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A review on techniques and modelling methodologies used for checking electromagnetic interference in integrated circuits

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ABSTRACT

The proper function of the integrated circuit (IC) in an inhibiting electromagnetic environment has always been a serious concern throughout the decades of revolution in the world of electronics, from disjunct devices to today's integrated circuit technology, where billions of transistors are combined on a single chip. The automotive industry and smart vehicles in particular, are confronting design issues such as being prone to electromagnetic interference (EMI). Electronic control devices calculate incorrect outputs because of EMI and sensors give misleading values which can prove fatal in case of automotives. In this paper, the authors have non exhaustively tried to review research work concerned with the investigation of EMI in ICs and prediction of this EMI using various modelling methodologies and measurement setups.

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1. INTRODUCTION

An integrated circuit (IC) is a small wafer, typically made of silicon, that can carry transistors, resistors, and capacitors anywhere from hundreds to millions [1]. Electromagnetic interference (EMI) is a disruption caused by an external source that will affect an electrical circuit through electromagnetic induction, radiation, conduction, or electrostatic coupling as shown in Figure 1 [2]. In the radio frequency spectrum, it is also known as radio frequency interference (RFI) [3]. Any device is electromagnetic compatible, if it functions without error and it also does not affect the operation of other devices in its intended electromagnetic environment [4].

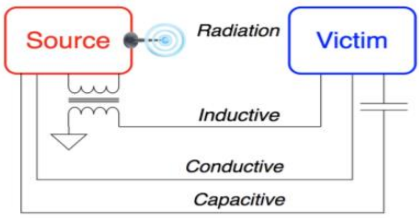

Figure 1. Path for EMI [2]

Electromagnetic compatibility (EMC) can be categorized in two directions: electromagnetic emission, which can disrupt the working of other systems and electromagnetic susceptibility, which basically describes how efficiently our system will work if it is subjected to disturbances from other systems [5]. The circuit's performance may be harmed or possibly shut down because of the disruption. EMC compliance is becoming more important as the number of ICs on electronic modules in the automotive industry grows [6]. Preventing EMI faults within a vehicle drives this EMC. Failure to do so could result in financial loss and, in the worst-case scenario, human life [7]. EMC therefore plays a major role in the design of automotive electronics, as shown by the broad body of work on this subject [8]-[14]. Research shows that the confidence level of first time passing an EMI test is easily raised from 35% to 80% if proper and upfront EMC design guidelines are followed [15]. Therefore, it becomes important to check the EMC from the IC level before the overall prototype is ready.

In this paper, main types of EMC issues encountered in ICs are briefly discussed in section 2 and an overview of most popular modelling techniques for ICs is presented in section 3. The standard EMC measurement methods have been explained briefly in section 4. Some most used EMI shielding techniques are discussed briely in section 5. Various modelling tools and experimental approaches used over the years for checking EMI in ICs have been reviewed and some of the strengths and weaknesses have been compared in section 6. Finally, in section 7, discussion is provided and conclusion is drawn.

2. EMC IN ICs

ICs play a critical role in an electronic system's EMC. Generally, ICs are both the ultimate source of interference-causing signals and the victim. The proper operation of an IC in an obstructive electromagnetic environment has always been a serious challenge. EMC problems in an IC can be generally classified into two types namely Intra chip EMC and Externally coupled EMC.

2.1. Intra chip EMC

When electromagnetic disruption from one portion of the IC interfere with the operation of other components of the same IC, this is referred to as intra chip EMC [16]. Intra chip interferences are commonly divided into two categories: Crosstalk and simultaneous switching noise, both of which constitute signal integrity (SI) concerns [17]. In electronics, Signal Integrity refers to the signal's ability to perform without being harmed [18]. The ratio of the accidental voltage emerging across the load in the victim circuit to the signal voltage in the source circuit is the general definition of crosstalk between two circuits. Simultaneous switching noise, on the other hand, is a usual impedance coupling difficulty that occurs when many circuits in an IC share the same power distribution bus [19].

2.2. Externally coupled EMC

Before devices are used in an actual product, intra-chip EMC issues are usually rectified. However, noise coupled in or out of the chip packaging can cause EMC difficulties in semiconductor devices that have no intra-chip concerns. Externally coupled EMC difficulties are developed when the ICs electromagnetic noise upsets off-chip devices or circuits, or when electromagnetic commotion from other devices disrupts the ICs operation. Conducted coupling, electric field coupling, magnetic field coupling, and radiated field coupling are all examples of externally coupled EMI [20], [21].

3. EMC MODELS

In electronic equipment, ICs are often the main source of disruption [22]. Several studies have been documented explaining the sensitivity of ICs to EMI, as these are usually the most sensitive too [23], [24]. Standards like the international special committee on radio interference (CISPR) 25 [25] for emissions and the International Organization for Standardisation (ISO) 11452 [26] for EMI susceptibility describe EMC test setups for the electronic systems used in automotive Industry. In recent years, electronic device designers have expressed a strong desire for easy and accurate measurement methods focusing on ICs.

The I/O buffer information specification (IBIS) working group made the first major contribution to standard EMC modelling by introducing a standard for defining the electrical efficiency of IC I/O structures. IBIS initially concentrated solely on signal integrity (SI) issues at the I/O level, with no knowledge about noise inside the IC core [27]. However, EMC was also considered for I/Os beginning with version 4.1.

In 1997, the "Union Technique de l'Electricite" (UTE), a French standardization committee, paid attention to component EMC modelling and created ICEM, a generic model for prediction of parasitic emissions in ICs [28]. ICEM debuted as a novel IEC proposal standard IEC 62014-3 [29] in 2002. Simultaneously, IEC 62404 [30] was adopted as the Japanese proposal known as I/O interface model for IC (IMIC). Table 1 summarises the most widely used EMC modelling techniques.

Table 1. Modelling techniques for ICs

Method	Simulation	Advantage	Drawback
IBIS [31]	Signal Integrity EMI	Not very Complex. Non confidential Data. Accurate I/O and package modelling.	Limited to 1 Ghz. Good Accuracy.
ICEM [32]	Conducted and Radiated Emissions	Not Complex. Non confidential Data.	Limited to 1 Ghz. Medium Accuracy.
IMIC [33]	Conducted and Radiated Emissions	Not Complex. Non confidential Data.	Limited to 1 Ghz. Medium Accuracy.

4. MEASUREMENT METHODS FOR EMC PREDICTION

The International Electro-Technical Commission has issued two standards: One for electromagnetic radiated and conducted emissions (IEC 61967) and the other for electromagnetic immunity (IEC 62132). The emission standard has 6 parts while the immunity standard has 5 parts as shown in the Table 2. TEM cell stands for transverse electromagnetic mode cell. GTEM or Gigahertz cell is the high frequency variant of TEM cell. Both are utilised to measure an ICs EME as well as its immunity to electromagnetic fields [34]. The surface scan method is another norm [35]. Using the surface scan technique, particular probes coupled to a receiver estimate the amplitude and phase of a particular section of the EM field generated by the IC.

IEC 61967-4 describes another method for measuring the conducted electromagnetic emission (EME) of ICs by using a 1Ω resistive probe to measure RF current and a 150Ω coupling network to measure RF voltage [36].The workbench faraday cage is another technique for conducting RF immunity and emission quantifications in a small space without the need for large anechoic chamber [37]. Magnetic probe method is another standard for emission measurement [38]. It specifies a procedure for measuring RF currents on the pins of an IC using a miniature magnetic probe and non-contact current calculation [39]. Bulk current injection (BCI) and direct power injection (DPI) are two popular immunity measurement methods. Bulk current injection's measurement theory is based on reproducing the induced current that EM fields coupled on a system's wires could produce in the real world [40]. On the other hand, DPI is a technique for determining how immune the IC is to conducted RF disturbances. Immunity measurements are guaranteed to be repeatable and correlated using this approach [41].

Table 2. Measurement standards of Electromagnetic immunity and emissions

S.NO	Emission		Immunity	
	Standard	Description	Standard	Description
1.	IEC 61967-1	Definitions	IEC 62132-1	Definitions
2.	IEC 61967-2	TEM/G-TEM cell [34]	IEC 62132-2	TEM cell [34]
3.	IEC 61967-3	Surface scan method [35]	IEC 62132-3	Bulk current injection (BCI) [36]
4.	IEC 61967-4	1Ω/150Ω method [37]	IEC 62132-4	Direct RF injection (DPI) [38]
5.	IEC 61967-5	Workbench faraday cage [39]	IEC 62132-5	Workbench faraday cage [39]
6.	IEC 61967-6	Magnetic probe method [40]	-	-

5. SOME COMMON WAYS TO REDUCE EMI

Aside from the EMI measurement techniques mentioned above, there are some of the most common structures used for electromagnetic shielding. A faraday cage was one of the earliest electromagnetic (EM) shields. The electrons in the walls of a faraday cage deploy in a way that neutralizes the electric field on the other side of the wall when an electric field is incident on them [37]. In addition to this, the space between each panel of a foldable shield can operate as a prow for EMI radiation in scenarios where foldable shields are used. In such circumstances, the joints and hinges should be tightly fastened to prevent any possible emission. To assure this, EMI shielding gaskets are used.

Differential mode (DM) and common mode (CM) noise make up most of the conducted emission noise. Filtering the generated CM and DM noises out of the system with EMI filters is a standard means of dealing with them. Because CM and DM noise signals require distinct filtering procedures, a noise separator is typically employed to differenciate these two undesired signals. Filters are added to the circuit once they have been separated. Electromagnetic absorbers are utilised in a variety of applications, including health monitoring, military, and radar cross section reduction, among others. These are also commonly employed in EMI/EMC technology. The reflection coefficient is the most significant metric to consider while developing and studying these absorbers. If a transmission line equivalent model is employed to examine the performance of an absorber, then the reflection coefficient R, is obtained by (1).

$$R = 20\log\frac{Z_i-1}{Z_i+1} \tag{1}$$

Where Z_i is the normalized input impedance [42].

6. REVIEW ON VARIOUS METHODOLOGIES USED IN RECENT WORKS TO PREDICT EMI

From the past few decades, a lot of work has been done in the field of EMC evaluation of ICs. Extraction of EMC models of ICs has been carried out extensively. Both modelling and experimental techniques have evolved and improvised over time. The EMC difficulties linked to direct and radiated emissions from high-speed ICs are discussed in [43]. Circuital and electromagnetic models are used to assess these emissions. Based on the integrated circuit emission model template (ICEM), an analogous circuit model is constructed to represent the IC and the influence of its loads. Figure 2 depicts the entire circuit as being formed of four primary subparts: the first is internal activity, IA which represents the core and I/O buffers, the second explains the package, and the third relates to the printed circuit board (PCB). The last subpart replicates a buffer that exchanges data with the IC via a generic load. In terms of radiated emission, an EM model formulated on the superposition of fields produced in the far field region by loop currents flowing towards the IC and package pins is proposed.

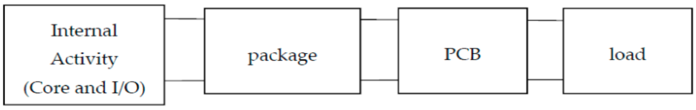

Figure 2. Circuit model conceptual diagram, based on [43]

A model-based simulation technique for characterization of immunity at system level at a premature design stage is presented which comprised of a hybrid 3D full wave, transmission line and circuit solver methodology and models for all components including ICs [44]. The bulk current injection (BCI) failure for a simple PCB comprised of a p-nitrophenol (PNP) transistor IC, namely 2SA1576 is predicted. An integrated circuit immunity model (ICIM) used for modelling the immunity of an IC is generated. Then this ICIM is used and a BCI simulation is performed. The BCI setup is simulated using method of moments (MOM). A the effects of various parameters like the number of winding turns, the width of coils on the S-Parameters of current injection probes are discussed [45]. The performance of a current injection probe is characterized with S-Parameters which could be measured using a vector network analyzer (VNA). It is reported that the insertion losses are found to decrease in low frequencies when the number of coils turns in the probe are increased showing the enhancement of the coupling effect of the probe. At high frequencies, the skin effect comes to play and insertion losses increase. To improve the probe bandwidth, it is suggested to reduce the number of turns of the coil winding.

The IC stripline technique is a new technique that could be utilized for calculating radiated emission falling in the sweep up to 3 GHz. The micro stripline approach is considered in [46] as well as its shortcomings in terms of characterisation of small package encapsulated ICs are highlighted. A novel EM guiding design that demonstrates an improved coupling with the Dalian University of Technology (DUT) in the 800 MHz-3 GHz frequency range is proposed to solve such problems. A test structure circuit model based on lumped elements that enables the use of SPICE-like simulators for circuit analysis is suggested. Contrasting the scattering parameters that were acquired from simulations with those resulting from measurements performed on a real test structure constructed and produced for this purpose, the model has been validated. A new way of modelling the DUT through EM simulations in the IC stripline has been proposed in [47]. The author has proposed the dimensions of an open version IC stripline and DUT as depicted in Figure 3.

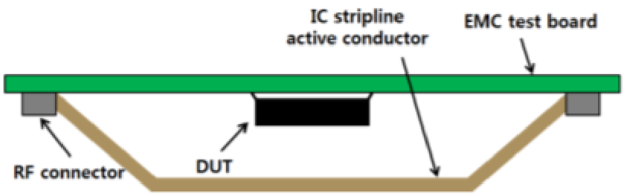

Figure 3. Simplified open version of IC stripline [47]

The S-Parameter results of 3D EM solver are looked at and an analogous lumped element circuit model is introduced and its exactitude is compared to 3D simulation. DUT is a quad flat package (QFP) with dimensions 10×10×2.1 mm. All the simulations as well as the IC stripline structure are simulated using 3D EM solver. Hwang *et al.* [47] has followed the methodology but improvised model proposed in [48] which was a single LCT model. The author has added a new parameter for modelling the capacitance between the middle active conductor and ground. Mutual inductance and coupling capacitance are used to model the EM coupling between active conductor and DUT. Compared to the previous model, more specific results could be obtained from the distributed lumped element model.

Heuvelman *et al.* [49] this concept is extended and applied to wire bonded ball grid array (BGA) IC and the modelling methodology is validated with test structures. The measurement set ups to calculate the radiated emission from reference antenna structures as well as from the real IC are used. For the simulation set up, first a representative of 3D model based on finite element method (FEM) utilizing the IC stripline dimensions is made. The DUT is then placed in the 3D model of the IC stripline. The S-Parameter model in addition with the transistor level circuit model of the I/O and load is used to configure the wire bonded BGA and IC stripline. The radiation emission spectrum is then determined using a commercially available simulation tool. Comparison between simulation and measurement results of various S-Parameters were made and found to be in excellent agreement.

The electromagnetic emissions (EME) are studied by a simulation method using a Gallium Nitride high electron mobility transistor power amplifier IC chip [50]. For simulation of 3-D IC layout, a simulation model has been suggested by introducing a high-frequency structure simulator with a Keysight advance design system (ADS). Experiments are used to verify the effects of the simulated EME. The EME for the IC chip is reduced using this simulation process, which uses a response surface methodology. In consequence, small improvements in the IC layout have been found to have a major impact on the EME.

The EMI susceptibility tests for ICs can be somewhat accurate based on the package size and shape. For example, an IC encapsulated in tiny package may show high immunity to EMI, whereas the same IC encapsulated in larger packages may show a lower immunity. The micro stripline method is studied and a new structure for coupling between the EM guiding structure and the IC terminal is proposed [51]. The DUT is organised on a test board which is used to provide the nominal signals to the DUT and collect a portion of EMI dispersed through the stripline. The preliminary design which is carried out as per the guideline has an aim to escalate the stripline to trace coupling in the range 0.7 to 4 GHz and when the DUT and its holder are put on the stripline, voltage standing wave ratio (VSWR) was observed to be below 1.25.

Novel disturbance generator models were developed to form part of a virtual EMC lab [52]. Current simulation models concentrate primarily on the IEC61000-4-2 discharged [53]-[54]. The scope varies and the primary focus is only to replicate the disturbance as defined in the specification. However, detailed and precise models over a wide range of load conditions have been implemented and tested in [52]. The study also highlights some of the inaccuracies of the standards, showing that different pass/fail EMC results can result from the use of different test equipment.

The EMI that an IC is subjected to when installed in real applications are not confined to be continuous wave (CW) or amplitude modulated. Strangely, this topic has not received as much attention as it deserves. However in [55], the author focuses on this aspect, addressing the problem from victim’s perspective (DUT) and covering all possible EMI induced failures by using a two-tone interference. An IC passing an immunity test such as the DPI could fail in practical applications with much lower levels of power than the ones it could withstand in the test. A solution of using two tone interferences which has a frequency deviation lower than the bandwidth of the circuit is put forward. A method to foretell and interpret the EMI spectrum from time-domain waveforms is suggested in [56]. The technique is built based on formulated operating principle of the spectrum analyzer and the specifications of EMI standards.

The current proficiency and power rating of power converters could greatly improve by the parallelization of silicon carbide (SiC) metal-oxide semiconductor field-effect transistors (MOSFETs). However, modelling EMI in a power module with parallel-connected SiC MOSFETs (PMPSM) is complicated by the the inductive coupling effect of parasitic inductance between the paralleled branches. First an EMI source generation mathematical modelling approach for PMPSM is proposed which identifies the coupling difference in multi switch in parallel conditions [57]. The inductive coupling of parallel-connected switches can also be used to compute the interference quantity. Following that, a common mode (CM) propagation mathematical modelling approach for PMPSM is proposed, which is based on the inductive coupling theory, which discovered the suppressed effect of parasitic inductances between parallel switches on high-frequency CM interference.

A unique CMOS miller operational amplifier (OpAmp) with excellent EMI immunity is proposed In [58]. The first-order quadratic mathematical model is used to build the proposed amplifier. The modelling equations in this study were constructed using typical mixed-mode CMOS technology. The goal of the suggested modelling in this paper is to create a first-order symbolic expression that incorporates the body effect and CLM for the output offset voltage. The suggested modelling is an important tool for comparing different architectures and gaining a better knowledge of the design aspects that affect the output offset voltage.

The effects of conducted emissions from ICs are studied and noise models are developed [59]. For noise-model building, both IBIS-based and measurement methods are investigated. The noise source model created for a test IC is used in system-level simulations, and the measured far field radiation is checked through measurements. The model's ability to characterise the conducted emissions from an IC I/O pin is demonstrated by the agreement between the simulated and measured performance. IBIS models have been used in [60] for noise extraction in ICs for conducted emission modelling. Total voltage is extracted from the IBIS model and correlated with a particular structural S-Parameter using this method. The IBIS model and the S-Parameter are used in ADS software to determine total voltage. The far field radiation is obtained after simulation. The simplicity of this method for both linear and nonlinear I/O buffer circuits is its biggest ascendancy.

IBIS models have also been used in [61] to perform Signal Integrity analysis of a high speed, low power analog to digital converter IC MAX11129 from maxim integrated. IC designers have always been concerned with signal integrity. It is responsible for several other silicon failures as well as IC redesign considerations [62]. Baba *et al.* [61] have carried out the signal integrity analysis of the IC by importing the IBIS model of the IC into ADS. The mismatch between the signals at the driver pin and the load pin has been checked. Some initial mismatch has been discovered, which has been linked to DUT signal integrity problems. To prevent reflections, it has been proposed that lines be properly terminated, and crosstalk between adjacent traces be reduced to a minimum.

Equivalent models of ICs can be used for the EMC analysis. Sufficient information about the IC is required for the construction of these models. For cases where this information is not available to the designers, a mathematical modelling technique has been proposed in [63]. The feature of the near and far electromagnetic fields coupling of the IC, as derived via near field scanning, are analyzed using a dipole moment model in [63]. In addition, the study shows an array of electric and magnetic dipole moments that were utilized to duplicate field distributions in the scanning plane above the IC. Table 3 presents a comparison of various methods used in the recent works.

Table 3. Comparison of different methods used in previous literature

Authors	Method Used	Strengths	Limits
[43]	Conducted emission modelling based on ICEM and radiated emission model based on superposition of fields.	Contribution of direct emission from ICs is highlighted which is usually hidden by indirect emissions coming from PCB.	The experimental setup for finding conducted and radiated emissions accounts for an uncertainty of around ±2.5 dB on the considered frequency range.
[44]	Bulk current injection and simulation using MOM.	BCI is popular for its simplicity and cost effectiveness	The performance of the injection probe and hence the results of the test are dependent on the bundle length and terminating impedance.
[45]	Using matching components to enhance performance of BCI probe.	High current injection and high coupling density of magnetic field lines.	Adding parallel resistances to improve frequency selection can cause more losses.
[47]	DUT has been modelled in an open version IC stripline.	The model presented can be used for rapid analysis for EMC of ICs.	Manufacture and measurement of IC stripline method is different for different types of ICs.
[49]	Modelling using IC stripline method has been extended and a representative model based on FEM is used.	Radiated emissions from DUT as well as from antenna structures are determined.	Coupling varies from case to case between the IC and the stripline. Therefore, 2 samples of the same IC encapsulated in 2 striplines can show different results.
[51]	Microstrip line technique is used and a new coupling structure has been proposed between IC and the guiding structure of EM.	Coupling structure that takes care of dependence of EMC of an IC on impedances seen at the PCB level loading and dependence of coupling on stripline has been proposed.	Maintaining regulated impedance through the design is extremely important when transmission lines are routed in a high-speed design.
[55]	Two tone interference effects are checked.	Methods of making IC withstand real environment interferences are proposed.	The setup is a bit complicated with the requirement of an additional RF source and a combiner.
[59]	IBIS model is used to extract noise sources from the IC.	IBIS model for ICs is readily available as compared to SPICE models.	The set up is only for conducted emissions and not for conducted immunity.

7. DISCUSSION AND CONCLUSION

EMI and EMC of ICs has been a hot topic of interest over the years. This research reviews a good number of recent publications made in this field. In this paper all the important aspects of IC EMI/EMC are briefly explained and recent work in this field is non-exhaustively summarised. Upon analysis, it can be realised that apart from the measurement methods avaible for EMI measurement, it can be extremely beneficial to use modelling methodologies if some knowledge about the IC is available. In addition, the measurement test setup for EMI detection is highly complex and costly with limited applications making modelling methodologies even more desirable. Early electrical simulators such as SPICE simulation tools, were created to simulate electronic system susceptibility to EMI. However, it is hampered by practical realities such as different simulators, undocumented simplifications, simulation speed, model availability, and vendor's reluctance to offer the SPICE model of I/O structure to the public. IBIS is the first significant development as far as IC modelling is considered. Initially IBIS was only concerned about SI analysis in an IC. However, EMC was also considered for I/Os beginning of version 4.1. The ICEM was developed to accurately account for the internal operation of ICs. The restrictions of this model as far as the overall operating frequencies are considered can be overcome by using a distributed model to account for the effects of the loads and transmission lines on the PCB. Thus, every approach has its own benefits and choosing a measurement, or a modelling approach based on the priorities of the designer is appropriate until a technique that can very accurately consider all the aspects of the DUT can be derived.

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