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Current mismatch reduction in charge pumps using regulated current stealing-injecting transistors for PLLs

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ABSTRACT

A charge pump for phase locked loops (PLL) with a novel current mismatch compensation technique is proposed. The proposed circuit uses a simple yet effective current stealing-injecting (CSI) technique and feedback to reduce mismatch between the negative-channel-metal-oxide (NMOS) and positive-channel-metal-oxide (PMOS) transistors. The current stealing transistor steals the current from a replica branch and mirrors it to the output where it is added to the output branch by the injecting transistor. A feedback mechanism is used to set the drain voltages of both branches to be equal and mitigate channel length modulation and ensure high accuracy. The proposed circuit was designed on Silterra 130nm technology and simulated using Cadence Spectre. The simulation results show that the proposed circuit yields a maximum of 0.107% and minimum of 0.00465% current mismatch while operating at a low supply voltage of 800mV for a range of 100mV to 700mV. The proposed design uses only one rail-to-rail op amp for compensating the mismatch and an addition of 4 transistors and utilizing 75% of the supply voltage for high voltage controlled oscillator (VCO) tuning range.

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1. INTRODUCTION

Recently, there has been an increasing demand for continuous supply of integrated circuits or better known as chips, for various purposes, the most recent and prevalent applications being 5G wireless chips and processors. One common block in these chips is the phase locked loops (PLL). The motivation of this work is to build one of the most important building blocks in a PLL system, namely, the charge pump. As mentioned earlier, the PLL has seen usage in chips, specifically serializes and deserializes (SERDES) protocols and radio frequency (RF) transceiver systems. In SERDES protocols, the PLL in the transmitter chain is responsible for the timing functionality [1]-[3]. Meanwhile, in RF transceivers, the PLL is used for the up-conversion and down-conversion of the signal through the mixer [4]-[6]. Apart from that, PLLs can also be used as frequency multipliers in microcontrollers, autonomous batteryless circuits [7] and as a clock generator in wireless sensor nodes (WSN) for health monitoring systems [8].

This work highlights the research problem with the charge pump in the PLL that can disrupt the PLL operation due to the current mismatch of the up current carried by the positive-channel-metal-oxide (PMOS) and down current carried by the negative-channel-metal-oxide (NMOS). Specifically, the current mismatch

causes reference spur and static phase offset in the PLL leading to PLL spectral impurity [9]-[12]. The implication of the spectral impurity in the PLL caused by current mismatch in the SERDES system is that the reference spur causes jitter in the PLL and degrades the timing capabilities on the transmitter side. Meanwhile, in the RF transceiver the implication of an impure spectral performance in the PLL manifests itself in the form of an overlap in the desired signal and the nearby adjacent signal when the mixer up-converts an RF signal. Therefore, it is imperative that the current mismatch problem be minimized in the PLL.

Consider a conventional current steering charge pump depicted in Figure 1. The current mismatch between the PMOS and NMOS exists due to the difference in the transistor electron mobility (μC_{ox}) and threshold voltage (V_{th}) values of the different transistors, leading to different current values carried by the NMOS and PMOS transistors at the output branch namely N1 and P1 respectively. On top of that, the channel length modulation causes the current through these transistors to vary largely due to variation in Vctrl. Since the Vctrl is supplied at the drain of both NMOS and PMOS transistors, the current will vary largely, hence degrading the accuracy. The problem is made even worse at lower voltage, since the current mirrors have limited headroom to operate in saturation, especially when the Vctrl is close to the upper and lower rails, these PMOS and NMOS, will be pushed to the triode region and hence degrade the current mirror performance. This translates to limited Vctrl range in which the charge pump can operate optimally and consequently affect the tuning range of the voltage controlled oscillator (VCO). Ideally, a VCO should have a wide tuning range to achieve a wide frequency range, which translates to high VCO gain and ease of PLL locking.

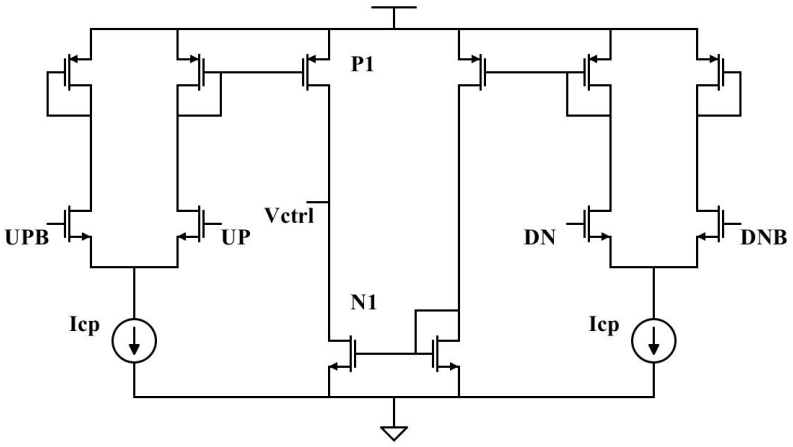


Figure 1. Conventional current-steering charge pump

This work attempts to minimize the current mismatch by using negative feedback technique to ensure the down current in the NMOS tracks the up current in the PMOS. The novelty of this work compared to other works in literature is the technique in which the feedback configuration is carried out, which is using a simple yet effective current stealing-injecting (CSI) technique and feedback to reduce mismatch between the NMOS and PMOS transistors. Other than that, this work is capable of operating down to a low supply voltage of 0.8V. Lastly, the amount of components used in the proposed charge pump design are far less compared to those reported in literature. Specifically, the proposed charge pump only uses one rail to rail op amp and an addition of 4 transistors.

2. RELATED WORKS IN CHARGE PUMP DESIGN

2.1. Advanced mismatch calibration techniques

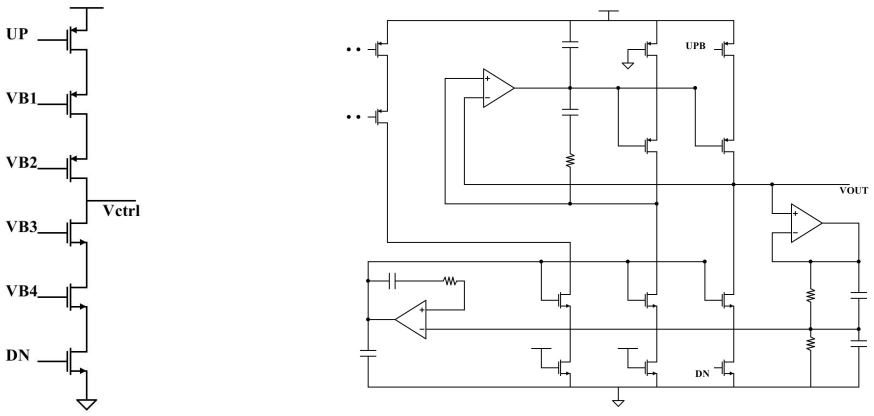
Lin *et al.* [13] proposed two techniques to overcome the charge pump mismatch, namely by using a dynamic charge pump with current-matching capabilities. Other than that, they proposed introducing a DC offset to the output of the charge pump in order to increase linearity and decrease spur in the PLL. A PLL employing the random pulsewidth matching (RPWM) and sub-sampling charge pump (SSCP) technique was demonstrated in [14]. This work attempts improve the spur performance using the mentioned techniques by averaging, randomizing and lastly reducing the ripples at the output of the charge pump which is fed into the

VCO. The works by [15]-[17] employ digital calibration techniques to calibrate the charge pump mismatch. The typical blocks involved include a lock detector (LD), some form of phase detector, a digitally-controlled charge pump and calibration circuitry. The calibration circuitry can be in the form of digital-to-analog converter (DAC), filter and digital logics, as is the case in [15] or even sucessive-approximate register (SAR) based logic [16]-[17] and controls the digitally-controlled charge pump calibration process. The idea is basically the same, that is, the LD functions to detect whether the PLL has been locked and signals the start of calibration. The phase detector, either bang bang phase detector (BBPD) [15]-[16] or high resolution phase detector (HRPD) [17], functions to detect the difference of phase between the reference frequency and the feedback frequency. HRPD is an improvement of the BBPD proposed by [17] and is superior in terms of accuracy.

2.2. Analog-centric techniques

Other more traditional approaches are more analog centric in the way that they employ negative feedback loops and replica bias techniques to handle the current mismatch [19]-[24]. Some of these techniques are viable only due to the abundance of voltage headroom while others are inherently complex in terms of design implementation, that is they require additional circuitry for current compensation. For example, Figure 2(a) shows the charge pump architecture by [18] in which a cascode structure was used. Since the transistors need to be in saturation region, the V_{DS} of each stacked transistor must be high, hence the output voltage, Vctrl is limited to a range of roughly $2V_{DSn}$ to $V_{DD} - 2V_{SDp}$. On top of that, this technique is only viable when there is ample headroom for the transistors to saturate and is not suitable for low voltage design.

With regards to complexity, while the mentioned works use the concept of negative feedback, the key here is to use as fewer components as possible for implementing the compensation schemes. As an example, Figure 2(b) shows the charge pump design proposed by [19] in which a lot of extra circuitry was added in order to compensate the current mismatch such as 3 op amps, capacitors and resistors. Other than that, the work by [20] uses 1 rail to rail op amp while also adding extra circuitry for current compensation and mismatch cancellation. Hwang *et al.* [21] use 2 op amps in a dual feedback loop to compensate the current mismatch. On the other hand, Lozada and Espinosa [23] designed a fully differential charge pump which requires double the normal circuitry to operate. A bulk-driven charge pump in triple well technology was proposed by [24] which uses 1 op amp with the addition of several transistors and also resistors.



(a) (b)

Figure 2. Examples of charge pump architectures; (a) A cascode charge pump design by [18], (b) A charge pump design by [19] utilizing 3 op amps as the compensation scheme

2.3. Low voltage techniques

The recent trend of CP design is moving towards low supply voltage architectures. Some of the recent CP circuit design techniques that have been employed for low voltage operation include gate switching CP [25]-[26], DTMOS transistors for leakage control [27], diode-connected MOS CP [28], non-cascode source-switch CP [29], clock-gated CP with tunable low pass filter (LPF) [30] and dual feedback loop CP [31].

From the literature survey, it can be concluded that there is room for improvement in terms of the complexity of the architecture used in order to compensate the current mismatch. It can be seen that previous

works, especially the advanced techniques use a lot of components or blocks in implementing the compensation such as SAR and DAC. This could potentially increase power consumption and area of the PLL. The analog-centric approach also has the advantage of simplicity and can be further exploited to operate at lower voltage. Similar to the advanced techniques, existing analog-centric architecture uses bulky compensation circuitry that can be further reduced to save area and power consumption. This work will focus on employing a current mismatch reduction technique that minimzes number of components used so as to reduce complexity while operating at low supply voltage. At the same time, the employed technique maximizes the utilization of the limited headroom at low supply voltage for high VCO tuning range.

3. RESEARCH METHOD

The proposed charge pump is shown in Figure 3. It consists of the current steering charge pump, a replica branch to replicate the output branch and a pair of current stealing-injecting transistors. The replica branch is added to the current steering charge pump to extract the current mismatch via a current stealing transistor and inject the current back to the output branch. The current stealing transistor MN7 steals some current from the replica branch and mirrors it to the transistor MN6 which then injects the current to the output branch. The op amp is used in negative feedback configuration to set nodes A and B to be equal and ensure that the transistors in both branches have the same V_{DS} and hence have the same residue current flowing into MN7 and out of MN6. This scheme reduces the mismatch as the current injected into output branch through MN6 is forced to track the residue current from the replica branch via MN7 using negative feedback. In order to ensure the feedback is functioning, the ratio of the current flowing through MN4 and MN3 to MN5 should not be equal to 1. This is because if the current flowing through MN6 and MN7 is too low, the feedback will fail to operate. In this work, the ratio of MN5 to MN4 is 2:1, that is the current flowing through MN4 and MN3 is half of that in MN5. Table 1 shows the device sizing of the proposed charge pump circuit.

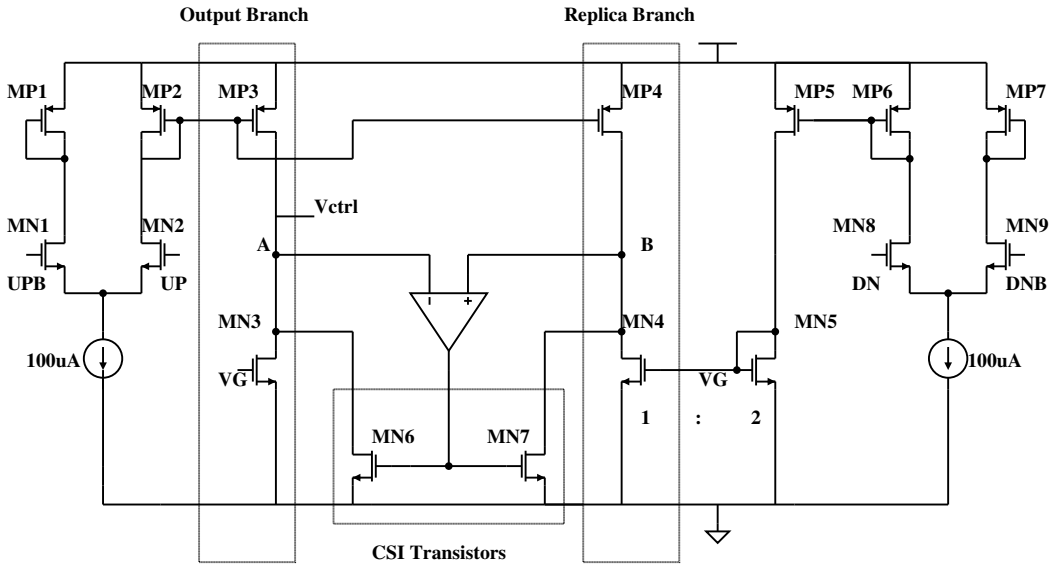


Figure 3. The proposed current-steering charge pump with current stealing-injecting (CSI) technique and feedback

The sourcing and sinking of current of the charge pump will be controlled by a block called the phase frequency detector (PFD) in the PLL. The PFD will output a high or low signal to the switches, namely transistors MN1, MN2, MN8 and MN9. For example, if the UP signal is high, while DN signal is low, the branch with MN2 will hog the current and MP2 will mirror the current to the output stage. Meanwhile, the branch containing MP7 and MN9 will hog all the current since the DN signal is low, leaving no current to flow from MP6 to MP5.

Table 1. Device sizing for the proposed charge pump design

Device	Size	Device	Size
MP1	30u/1u, m=2	MN2	4u/130n
MP2	30u/1u, m=2	MN3	20u/1u, m=4
MP3	30u/1u, m=2	MN4	20u/1u, m=4
MP4	30u/1u, m=2	MN5	20u/1u, m=8
MP5	30u/1u, m=2	MN6	10u/1u, m=4
MP6	30u/1u, m=2	MN7	10u/1u, m=4
MP7	30u/1u, m=2	MN8	4u/130n
MN1	4u/130n	MN9	4u/130n

The opposite happens when the UP signal is low and DN is high. In order to ensure wide compliance range of the charge pump, a rail to rail input op amp must be used. This work uses a rail-to-rail amp by [32] for constant-gm operation. The op amp used in this design uses a common drain input stage as a DC level shifter to shift the input voltages down and ensure constant-gm operation, followed by a common source stage. The input stage is followed by a current summing stage and a folded cascode load. A push-pull configuration was used for the output stage with miller compensation. The op amp design is depicted in Figure 4.

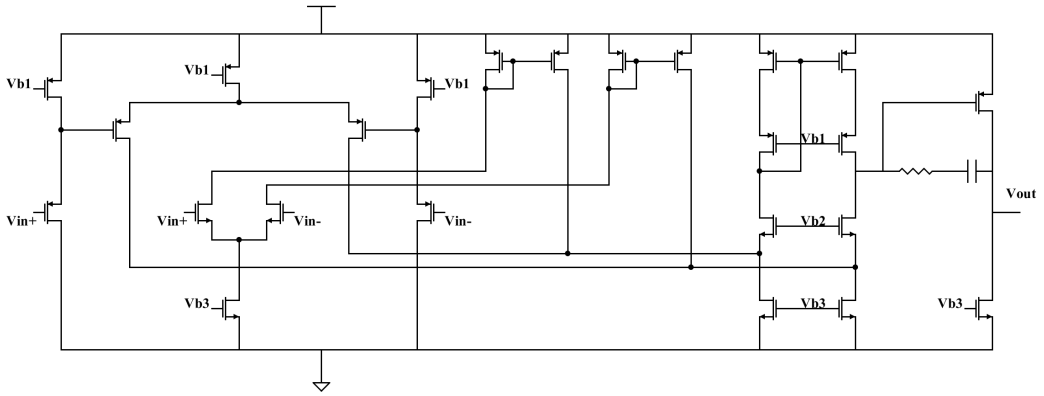
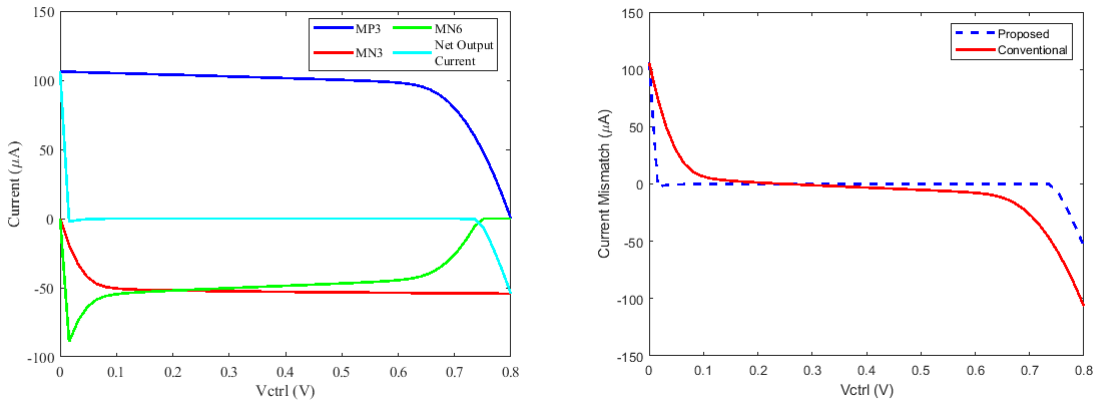


Figure 4. The rail-to-rail input op amp with common drain input stage as DC level shifter for constant-gm operation [32]

4. RESULT AND DISCUSSION

A pre-layout SPICE simulation was done using Cadence Spectre EDA tool to verify the effectiveness of the proposed technique in reducing the current mismatch in the charge pump. The simulation environment is under typical transistor conditions at a temperature of 27°. Figure 5(a) shows the drain current that is drawn by transistors at the output branch, namely MP3, MN3, MN6 and the net current. As explained previously, the drain current of MP3 carries 100μA, while MN3 carries 50μA. The drain current of MN6 is mirrored from MN7 and it tracks the difference of current between the MP4 and MN4, which ideally is 50μA. The drain current of MN6 is injected to the output node A to compensate for the mismatch. The net output current is given by the sum of the drain currents of MP3, MN3 and MN6. As depicted, it can be seen that the net output current is relatively constant in the 0μ regime, signifying that the output current mismatch is minimized.

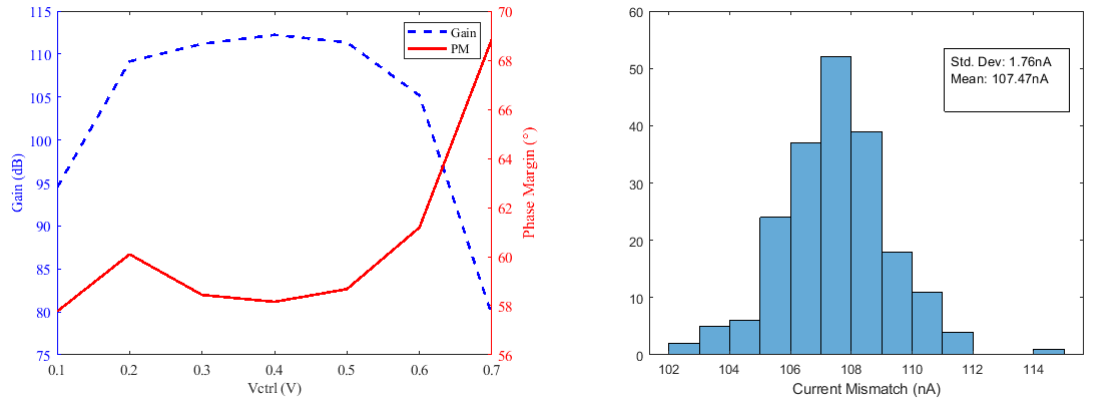
Figure 5(b) shows the comparison of current mismatch with and without the current stealing-injecting and feedback technique. For the conventional charge pump, it can be seen that the current mismatch varies greatly when the Vctrl is varied from 0V to 0.8V, achieving up to an absolute current mismatch of 26μA or 26% across the range of 100mV to 700mV. In contrast, the proposed charge pump circuit is relatively constant with an absolute maximum and minimum current mismatch of only 107 nA or 0.107% and 4.65 nA or 0.00465% respectively for the same range with 75% utilization of the headroom. The stark contrast between the current mismatch of the proposed and the conventional charge pump is a testament to the effectiveness in reducing the current mismatch in charge pumps. On top of that, the proposed circuit guarantees a mismatch of less than 1% from 31mV to 737mV which is 87.5% of the available headroom. From the Figure 5, it can also be noticed that when Vctrl approaches the upper and lower supply rails, the current mismatch deteriorates as the transistors MP3, MP4 and MN3 and MN4 will go into the linear region.



(a) (b)

Figure 5. The current mismatch simulation results; (a) Drain current of transistors at the output branch, (b) Current mismatch when Vctrl is varied from 0 to 0.8V

In order to ensure the proposed circuit is not oscillating, the stability of the negative feedback loop in the charge pump design is analyzed. Figure 5(a) shows the gain and phase margin of the proposed charge pump over the input Vctrl range of 100mV to 700mV. As can be seen, the achieved gain is from 79.58 dB to 112.23 dB. The phase margin range is from 57.8° to 68.9° indicating that the design is stable since it is within the vicinity of 60°. A Monte Carlo statistical simulation is carried out to verify under process variation, namely the (μC_{ox}) and (V_{th}). By running the Monte Carlo simulation, the extent of process variation on the current mismatch can be gauged. The Monte Carlo was run using Cadence Spectre tool with the confidential model files as the input given by the foundry, which cannot be disclosed. Figure 6(b) shows the Monte Carlo simulation of the proposed charge pump.



(a) (b)

Figure 6. Stability and Monte Carlo simulation results; (a) The gain and phase margin of the negative feedback loop in the proposed charge pump design, (b) Statistical Monte Carlo simulation for current mismatch with 200 runs

The design achieved an absolute maximum current mismatch with a mean of 107.4nA and standard deviation of 1.76nA, proving that it is a robust design over global and local variations. It can be seen that although subjected to process variation, the Monte Carlo simulation shows that the mismatch closely agrees with the pre-layout simulation under typical conditions. Table 2 summarizes the performance of the proposed CSI relative to previous works in charge pump design. From the table, it can be seen that the proposed design has the lowest current mismatch among all other works reported in literature. The calculation of the percentage of utilization is $(High\,boundary - Low\,boundary)/VDD * 100\%$ In the proposed design, the high boundary

is 700mV while the low boundary of the 100mV. The boundaries are taken at 100mV from the supply voltage (800mV) and ground (0V) to ensure the transistors at the output and replica branch have sufficient V_{DS} to operate in saturation. With a supply voltage (VDD) of 800mV, the proposed charge pump yields a percentage of utilization of 75%. On top of that, the design operates at a supply voltage of 800mV, which is the lowest among all the other works and still manage to achieve 75% utilization, on par with or better than other works. This superior current mismatch performance will enable it to minimize the effects of spur on the PLL and ensure spectral purity.

Table 2. Comparison of previous works in charge pump design

	This Work	[20]	[21]	[22]	[23]	[24]	[25]
Technology (nm)	130	180	65	130	65	180	180
Supply Voltage (V)	0.8	3	1.0	1.2	1.1	1.8	1.2
Vctrl Range (V)	0.1-0.7	0.2-2.7	0.1-0.85	0.2-1	0.1-0.92	0.3-1.5	0.2-1
Absolute Current Mismatch (%)	0.005-0.1	2.1	0.023-0.432	3.2	0.05	0.32	0.9
Up/Down Current (μA)	100	600	150	100	1000	100	140
Percentage of Utilization (%)	75	83.33	75	66.67	74.5	66.67	66.67
Standard Deviation (%)	<0.02	NA	<0.03	1.7	<2	<3.5	NA

5. CONCLUSION

A novel charge pump utilizing the CSI technique and feedback was designed to minimize the current mismatch which is important to reduce spur which will deteriorate the spectral purity of the PLL. The proposed charge pump uses only 1 rail to rail op amp in addition to 4 more transistors for the compensation scheme, which is low in complexity, resulting in high accuracy and minimal mismatch. Pre-layout SPICE simulation results using Cadence Spectre EDA tool show significant improvement over existing architectures in literature in terms of current mismatch, achieving a maximum and minimum mismatch of 0.107% and 0.00465% respectively at 800 mV supply voltage from a range of 100mV to 700mV. The design is also robust across process variations and is suitable for low voltage applications. In the future, the layout for the charge pump will be design for silicon fabrication. On top of that, the proposed charge pump design will be integrated at the top level with other blocks such as PFD, VCO, frequency divider and low pass filter for the system level PLL design. The practical applications of this includes RF wireless transceivers targeting applications such as WiFi, Bluetooth or 5G can have better PLL performance. Other than that, SERDES protocol chips that employ a PLL for timing purposes such as MIPI, SONET, USB, HDMI, PCI Express, Ethernet protocols can have accurate timing circuitry.

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