Magnetic Sensivity Modeling of DGMOSFET Transistor

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| **Article Info** |  | **ABSTRACT** |
| ***Article history:***  Receivedx xx, 2021  Revised x xx, 2021  Accepted x xx, 2021 |  | In this paper, the magnetic field effect on carrier transport phenomenon in Double Gate Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) has been investigated. This is done by exploring the Lorentz force and the behavior of a semiconductor subjected to a constant magnetic field. The magnetic field modulates the electrons position and density as well as the potential distribution in the case of silicon Tunnel FETs. This modulation impacts the device electricals characteristics such as ON current (*ION*), subthreshold leakage current (*IOF*), threshold voltage (*VTH*), the magneto-transconductance (*gmm*) and the output magneto-conductance (*gmDS*). In addition, a Hall voltage (*VH*) is induced and modulated by the magnetic field. It has been observed that this voltage influences the effective applied gate voltage. It has been observed that, the threshold voltage variations induced by the magnetic field is of paramount importance and affects the device switching properties both speed and power dissipation, noted that the threshold voltage VTH and (Ion / Iof) ratio are reduced by 10-3V and 102 for a magnetic field equal to ±6 and ±5,5 Tesla, respectively. We have simulated the different behavior in the channel mainly doping concentration, potential distribution, conduction and valence bands, total current density, total charge density, electric field, electron mobility and electron velocity. |
| ***Keywords:***  Magnetic field  Magneto Electronics  Hall Effect  Magnetic Short Channel Effects (MSCE)  Nano-Transistor  Silicon  DG MOSFET |
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| ***Corresponding Author:***  Arezki Benfdila,  Department of Electrical and Computer Engineering,  Mouloud Mammeri University,  Mouloud Mammeri University, Tizi-Ouzou -15000, Algeria.  Email: arezki.benfdila@ummto.dz | | |

1. **INTRODUCTION**

With the miniaturization of semiconductor technology, nanoscale integrated circuits have become very sensitive to the external magnetic field. Among the first measurements of the Hall Effect in silicon was made by Wick [1] on rather impure samples. Other studies were carried out by Pearson and Shockley [2] and by Putley and Mitchel [3], exploiting the Hall Effect on monocrystalline silicon with low impurities.

In the field of microelectronics technology reported parasitic effect on the external electrical characteristics in the Field Effect transistors MOSFETs [4,5], a few research has also motivated exploring the presence of magnetic field in the carrier transport phenomena in any substance carrying current, and thus also in the active region of a semiconductor devices especially in the technology of complementary Metal-Oxide-Semiconductor Field Effect Transistor (CMOS) [6,7].

The downscaling of dimensions of conventional MOSFETs at the nano-scale [8,9,10] is known to have a high magnetic sensitivity to the magnetic field [11,12] because of the low active channel area. This leads to complicate various Short Channel Effects (SCE) such as the effect of hot carriers effect, threshold voltage roll-off, substrate carrier effect, higher change in Hall voltage and drain source resistance (RDS) in the linear region [6,11,13,14].

Experimental of several case studies indicate that the magnetic field induced current deflection on the drain current voltage and changing the conductivity of the active region [15]**,** induces asymmetrical magneto tunneling conductance in MOSFETs resulting of non homogeneous space mechanical strain [16,17]. The magneto-transconductance of N-MOS Transistors exposed to the external magnetic field B=7T and 14T is reduced by 7% and 28% respectively due to the current reduction that comes from the deflection of the current lines inside the channel consequently of the Lorentz force acting to the current [12,18]. However, no research has been performed on the topic, certainly because of the applications of such a very high field limited.

The simulation of Hall Effect devices is relatively new, started in the 1980s [19,20,21] and has helped to analyze and understand the operation of Hall Effect in the complex devices such as integrated circuits.

The aim of this article is an analysis of advanced CMOS integrated circuits at the nanoscale and their sensitivity to the external magnetic field. Their performance can be seriously impaired and thus result from unforeseeable malfunctions. In the case of vehicles and machines controlled by these circuits, control is systematically lost.

To remedy this, control of the effects of the external magnetic field on the operation of these circuits must be controlled. This control involves the quantification of these noises, their analysis and their impact on the functioning of the circuits. For this, the DGMOSFET transistor was considered and modeled by the finite element method, while taking into account all the effects of carrier transport in semiconductors under an external magnetic field.The results show excellent accuracy comportment and good agreement compared with that obtained in the experimental study of MOSFETs technology.

1. **DIVICE STRUCTURE AND ANALYZES**

The structure of the device studied in our simulation is illustrated in Fig. 1. The applied magnetic field B= (0, By, 0) is consederated perpondicular to the current flowing between the two contacs drain and source oriented along the y-axis. The current density flowing through the silicon channel is along the z-axis. Two open circuit Hall1 and Hall2 rectangular contacts are provided for the detection of the Hall voltage VH, made on the DG MOSFET structure are placed perpendicular to the y-direction. The source (S), the drain (D) and the gate (G) as bias contacts. The length of the channel is L=30nm, it’s width is W=10nm. We assumed an enhancement n-type channel device. We shall denote the drain to source voltage by VD, the gate to source voltage by VG, and the threshold voltage by VTH.

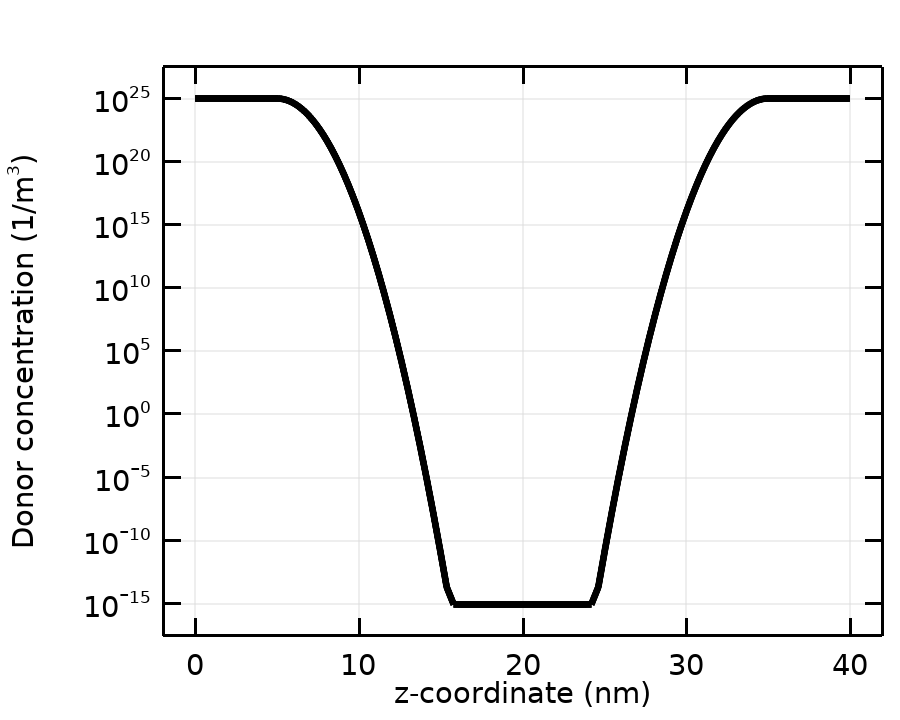
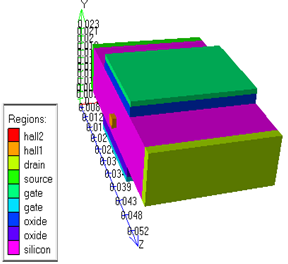


Figure 1. Schematic representation of the cross section of an n-channel DG MOSFET transistor. (Left image)

Figure 2. Logarithmic impurity doping profile distribution in the channel of Si DG MOSFETS.(Right image)

Figure 2.Illustrates the type of doping profile for the silicon DG MOSFET. Note that the electron concentration is highest in the source and drain extension contacts. The concentration is reduced past the limits of the source and the drain to the channel doped with acceptor impurity. The doping profile is a very important criterion in MOSFETs because it tells us about the desired drain current levels and the strength of the electric field in the device.

The details of device physical parameters used in the structure are shown in Table 1.

Table 1. Values of various parameters used in simulation.

|  |  |  |
| --- | --- | --- |
| *Symbols* | *Parameters* | Values |
| Na  Nd  tsi  LS ,LD  tox | Impurity doping in the channel  Impurity doping in source and drain  Silicon film thickness  Length of source and drainOxide thickness  Oxide thickness | 1014cm-3  1018cm-3  10nm  5nm  2nm |
| L | Channel length | 30nm |
| ε0 | Permittivity of vacuum | 8.8\*1012F/m |
| εsi | Permittivity of silicon | 11.85\* ε0 |
| εox | Permittivity of oxide | 3.9\* ε0 |
| T  ΦM | Absolute temperature in Kelvin  Metal work function | 300K  4.6eV |

If a constant magnetic field, B is applied along a perpendicular to the direction of drain current, the Lorentz equation will be used to describe the Hall Effect in silicon DG MOSFETs [11]

(1)

Here  is the cyclotron effective mass,  is the position, and the average (recombination) lifetime of the electron.  is the velocity at which electrons move through the Hall Effect.  is the electric field applied in a direction provided by the polarization contacts of the transistor.

Then the Hall field,  produced by the Hall Effect is given by [22],

(2)

In case of n-type channel MOSFET, the drian current  is entirely carried by majority carriers, electrons. Consequently,, thus equation (2) can be written, [15]

(3)

At very low drain voltage VD, in the linear region of operation of a MOSFET.

(4)

The area density of carriers in the channel is approximately constant over the channel. This charge density is given by

(5)

Where  denote the gate oxide capacitance per unit area. The drain current ID is given by

(6)

So, the  can be written as [23]

(7)

Where  is the channel conductance for. The channel conductance is given by,

(8)

Where  denotes the drift mobility of carriers in the channel,  is the magnitude of the inversion layer charge per unit area.

At higher drain voltage VD for

(9)

The carriers charge density in the channel continuously decreases with increasing distance from the source. The drain current is generally given by

(10)

Channel conductance  in saturation region is given by [24]

(11)

In long channel MOSFETs, therefore. So, effect of magnetic field on the short channel MOSFETs, thus very minor effect may be observed.

When the drain voltage reaches the value

(12)

The charge density at the drain boundary of the channel is practically reduced to zero, which corresponds to the pinch point. Beyond the pinch point, the drain current remains paratically constant. The drain saturation current is given by ( ) according to (10) and (12).

The Hall voltage of MOSFET is in the form [6]

(13)

Recalling that  given by (5), GH denotes the geometric correction factor and rH the Hall factor.

1. **SIMULATION AND RESULTSDISCUSSION**

**3.1. SIMULATION PROCESSOR**

In semiconductor physics, the classical model of carrier transport [30–31] is based on continuity equations. In order to have a complete description, we would also need to take into account the following partial differential equation:

 (14)

Where V: denotes the electrostatic potential, ε: is the electrical permittivity of the material, q: is the electronic charge and N = ND-NA is the fully ionized net impurity distribution. The solution of the Poisson equation in (14) is the electrostatic potential V. The discretization of the Poisson equation, the continuity equations of electrons and holes is necessary and a coupled method, which is a generalization of Newton's method, is used to calculate the initial proposed system by an numerical iterative method. And in order to express the impact of the magnetic field in the device, by solving and rewriting the usual Drift-Diffusion (D-D) model of carriers densities taking into account the terms depending on the magnetic field emitted by the effect of the Lorentz force on the carriers.

**3.2. RESULTS AND DISCUSSION**

Figure 3. Shows the variation of the Hall voltage VH induced on the surfaces of the Hall contacts as a function of the gate voltages VG applied to the gate (G) for three values of the applied magnetic field when existence (B = + 6 and -6 Tesla) and absence (B = 0 Tesla). We notice in the stationary state (Vg = 0), the Hall voltage is almost the same for the three values of the magnetic field. When the transistor has been biased, the Hall voltage increases or decreases gradually and asymmetrically with respect to the zero field (B = 0 Tesla) depending on the direction of applied magnetic field, and the hall voltage increases or decreases rapidly for higher values of gate voltage VG Until saturation, when the migration of electrons on the hall walls stops.

Figure4. Shows the variation of the Hall voltage VHas a function of the drain current ID flowing under the drain and the source contacts developed by the gate voltages VG applied to the gate contact (G) for three values of the applied magnetic field, B = + 6, B = -6 Tesla and B = 0 Tesla. We can see that in the quiescent state (Vg = 0), the Hall voltage is almost the same value for all three values of the magnetic field. As the gate voltage increases, the Hall voltage increases or decreases gradually and asymmetrically with respect to the zero field (B = 0 Tesla) depending on the direction of the applied magnetic field, and the hall voltage increases or decreases rapidly after just the threshold voltage VTH. For higher values of the bias voltage Vg, Hall voltage follows the same evolution until stability in the saturation region.

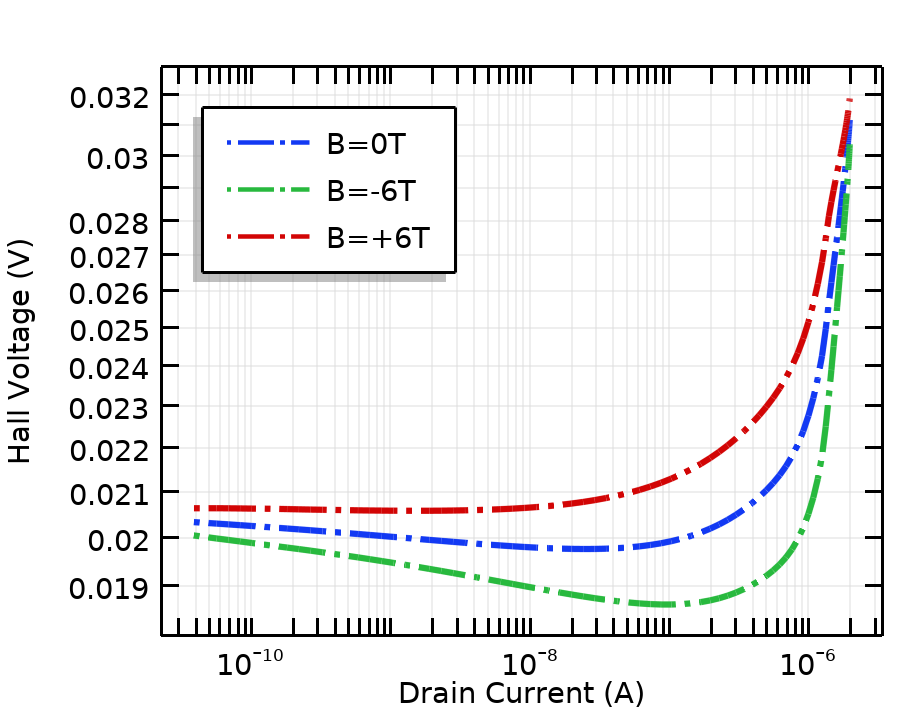
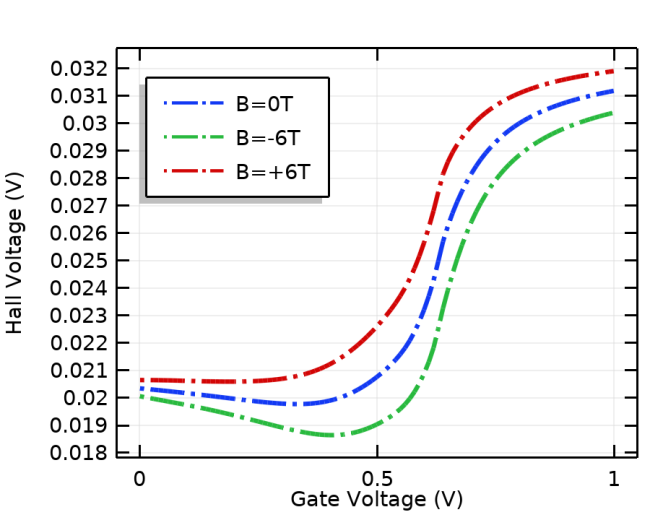


Figure 3. Hall voltage (VH) variation with gate voltage when B=+6, -6 Tesla and B=0 Tesla at VD =0.05V.(Left image)

Figure 4. Hall voltage VH variation with drain current ID for various gate voltage VG, when B=+6, -6 Tesla and B=0 Tesla at VD =0.05V.(Right image)

The hall voltage virsus drain voltage and hall voltage virsus drain current characteristics of the DG MOSFET surface recombination transistor are shown in Fig. 5. and Fig. 6. respectively, If the carriers are deflected towards the Hall2 recombination surface, their concentration in the transistor channel decreases, and the current also decrease. If the carriers are deflected towards the hall1 recombination surface, their concentration in the channel of the transistor increases, and the drain current also increases. this explains the difference in the hall voltage on the two surfaces of the hall1 and hall2 contacts. There fore, this magneto-transistor is sensitive to the sign of the applied magnetic field.

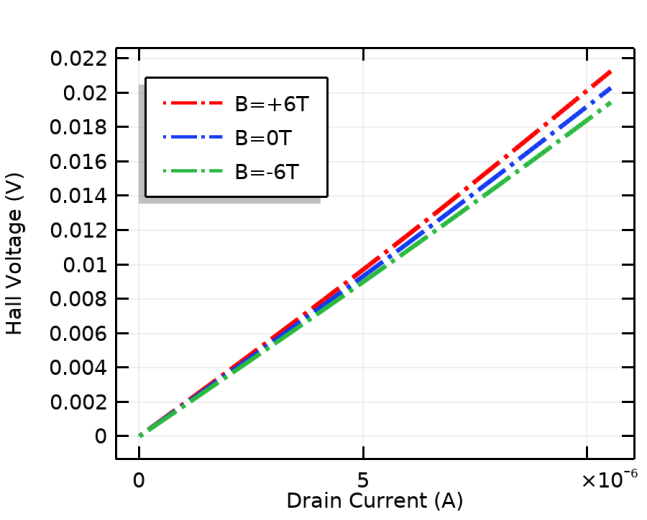
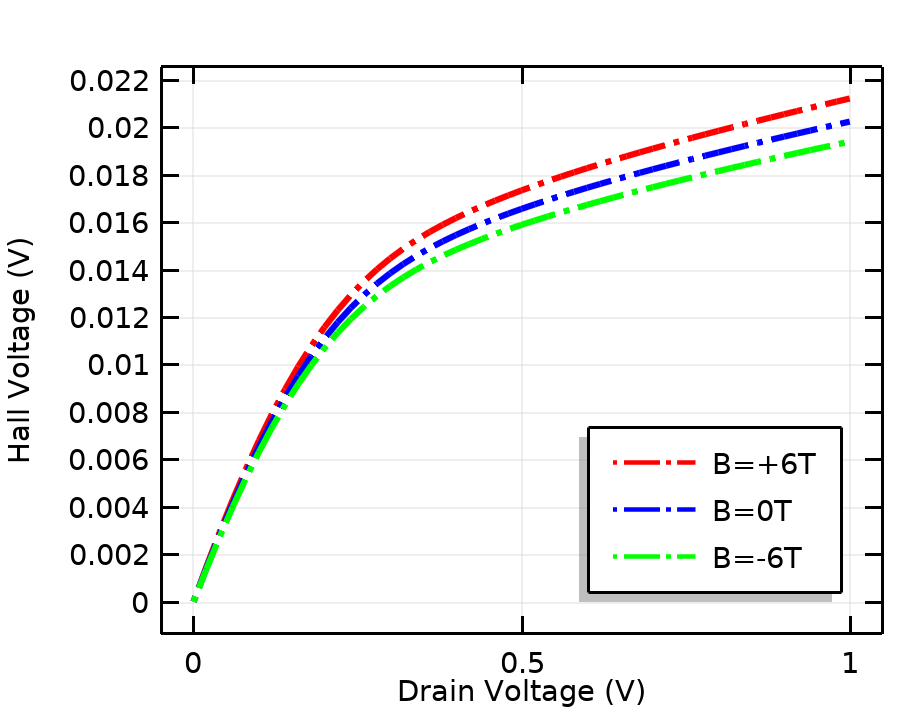


Figure 5. Hall voltage VH variation with drain voltage (VD) when B=+6, -6 Tesla and B=0 Tesla at VG=0.05V.(Left image)

Figure 6. Hall voltage VH variation with drain current ID for various drain voltage, when B=+6, -6 Tesla and B=0 Tesla at VG=0.05V. (Right image)

Figure 7. Illustrate the center potential in the x-direction for three values ​​of the magnetic field. The results considered when the device is in the on state and the gate voltage varies from 0 V to 1 V and the drain voltage is 0.05V, hence a large value of the current in the channel under gate voltage. When the drain source current emerged in a magnetic induction B perpendicular to the direction of this current, a Hall Effect appeared which gave rise to a potential difference between the two contact hall surfaces Fig.7, and a transverse electric field in the x-direction in the silicon channel Fig.8.

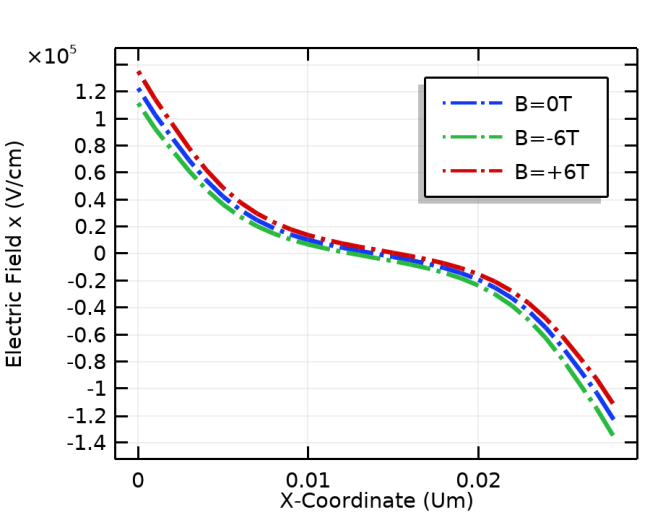
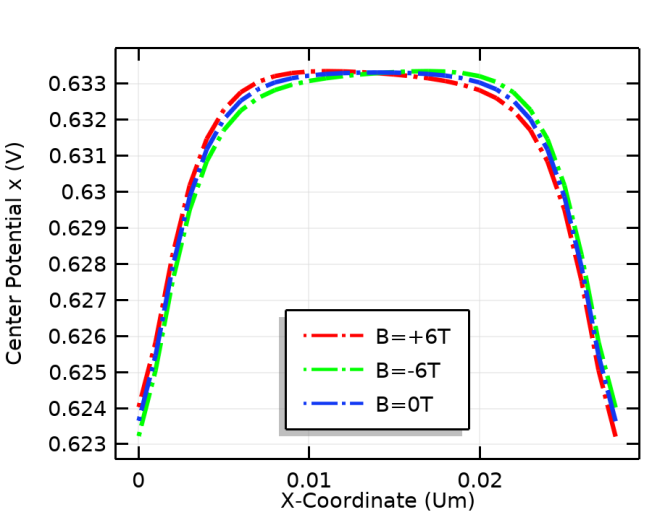


Figure 7. Center potential along the channel length in the x-direction for three values of magnetic field B=+6, -6 and B=0 Tesla at various gate to source voltage VG and VD =0.05V. (Left image)

Figure 8. Electric field along the channel length in the x-direction for three values of magnetic field B=+6, -6 and B=0 Tesla at various gate to source voltage VG and VD =0.05V. (Right image)

The electric field which compensates for the Lorentz force due to the charges which accumulate on the hal1 and hal2 faces, tends to modify the mobility and the velocity of the electrons Fig.9 and Fig.10,respectively, along the x-axis while respecting both orientation and the absence of a magnetic field.

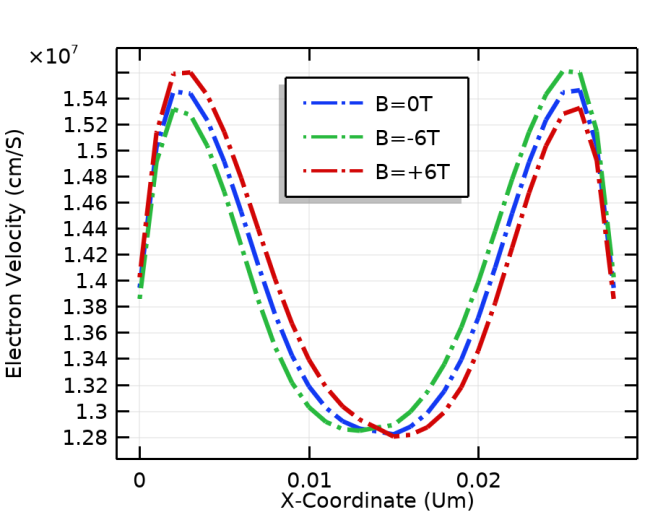
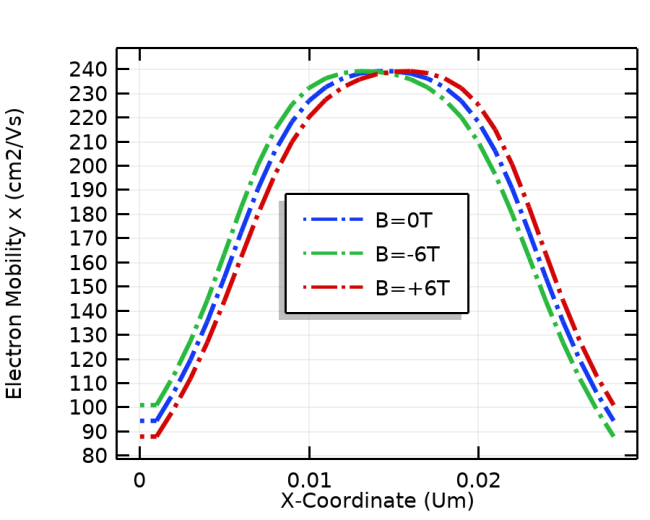


Figure 9. Electron mobility along the channel length in the x-direction for three values of magnetic field B=+6, -6 and B=0 Tesla at various gate to source voltage VG and VD =0.05V. (Left image)

Figure 10. Electron velocity along the channel length in the x-direction for three values of magnetic field B=+6, -6 and B=0 Tesla at various gate to source voltage VG and VD =0.05V. (Right image)

The electrons crossing the silicon channel in the direction opposite to that of the drain current undergo the Lorentz force, according to the direction of the magnetic field, accumulating there, thus creating new trajectories of the current lines along the x-axis, illustrated in Fig.11, and a differential charge density distribution shown in Fig.12.

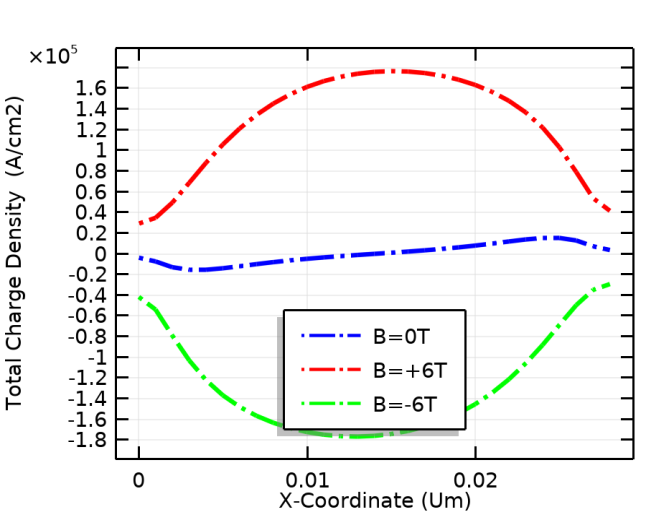
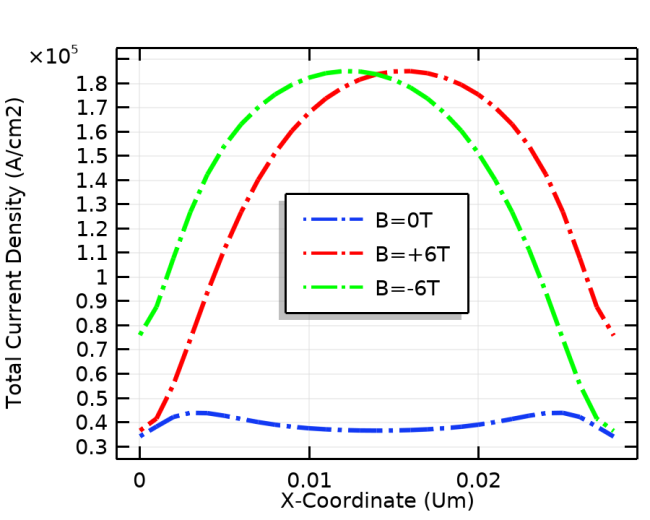


Figure 11. Total current density along the channel length in the x-direction for three values of magnetic field B=+6, -6 and B=0 Tesla at various gate to source voltage VG and VD =0.05V. (Left image)

Figure 12. Total charge density along the channel length in the x-direction for three values of magnetic field B=+6, -6 and B=0 Tesla at various gate to source voltage VG and VD =0.05V. (Right image)

Figure 13, and 14, illustrates the energy band diagram of DG MOSFET transistor. The band diagrams are along the channel in the x-direction following the hall-field direction. The two band diagrams show the position of the valence and conduction bands. The two band diagrams are considered when the device is on and the gate voltage varies from 0 V to 1 V and the drain voltage is 0.05V, Hence an increased value of the current in the channel under the gate region. Also, quasi-fermi level shifts of electrons and holes appeared caused by the action of an induction field in the current which modifies the distribution of the energy band levels.

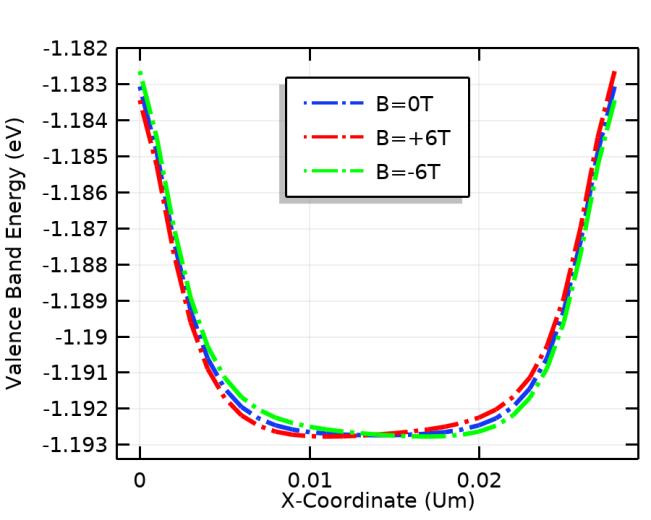
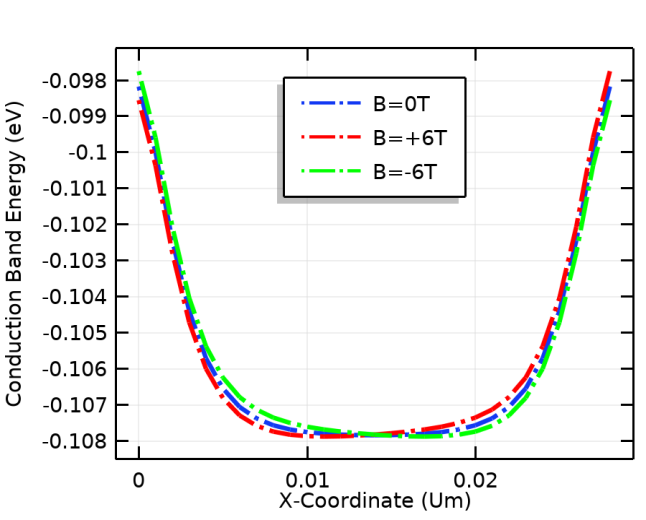


Figure 13. Conduction band energy along the channel length in the x-direction for three values of magnetic field B=+6, -6 and B=0 Tesla at various gate to source voltage VG and VD =0.05V.(Left image)

Figure 14. Valence band energy along the channel length in the x-direction for three values of magnetic field B=+6, -6 and B=0 Tesla at various gate to source voltage VG and VD =0.05V.(Right image)

The ID versus VD curve under constant magnetic flux density, B= 0 Tesla, 6 and -6 Tesla are shown in Fig. 15. It can be seen that in the linear region of the ID vs VD curve, the drain\_current ID remains the same with both directions of the applied magnetic field, but in the saturation region, ID increases or decreases depending on the direction of applied magnetic field. Due to the Hall effect, since electrons accumulate on the surface of the hall1 and hall2 contacts, the value of the amplitude of the charge of the inversion layer per unit area is effectively reduced, which reduces the magneto-conductance of the channel shown in Fig. 16.and therefore the drain current ID is reduced. If the constant magnetic field, B is applied along the reverse direction, along the negative y-direction, then the effect will be totally opposite. In this case, the magneto-conductance will be increased, causing the drain current ID to increase.

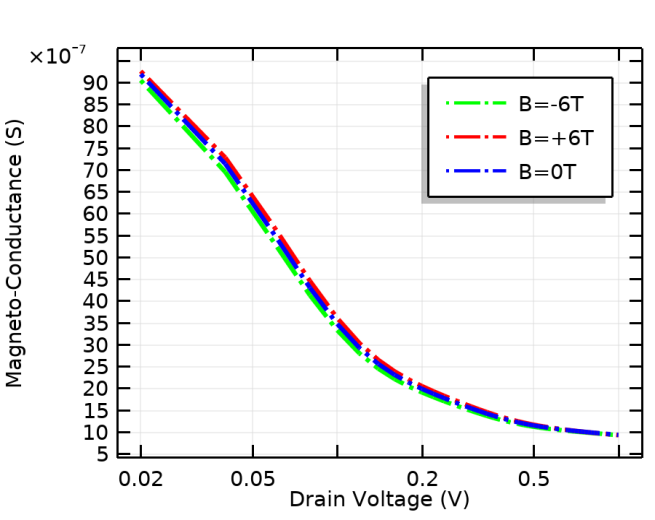
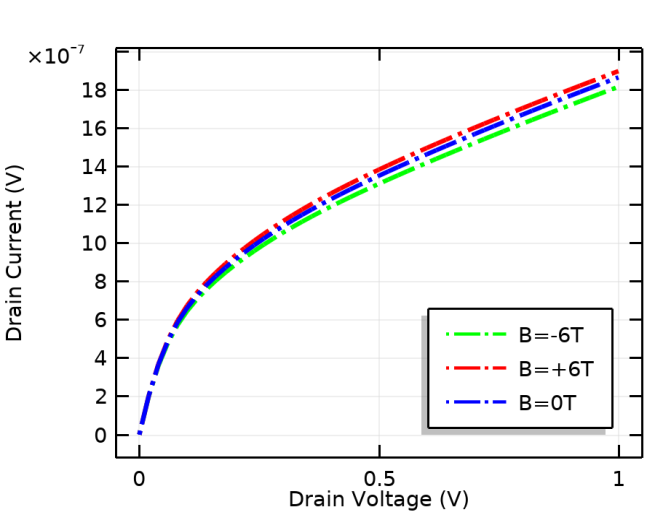


Figure15. Drain current (ID) against drain voltage (VD) when B=+6, -6 Tesla and B=0 Tesla at VG=0.5V [15-16]. (Left image)

Figure 16. Magneto-conductance (*gmDS*) against drain voltage (VD) when B=+6, -6 Tesla and B=0 Tesla at VG=0.5V [15]. (Right image)

Figure17. Shows a proportionality of an imbalance of the drain current ID as a function of the direction of applied magnetic field B, for the different values of the drain voltage VD=0.1V, VD=0.5 V and VD=1V. Note that there is a significant difference in sensitivity for the higher drain voltages which corresponds to the saturation region of the ID vs VD curve Fig 15. the difference is a little less in the region of the threshold voltage VTH=0.44072V at B=0Tesla0, but the difference is almost negligible is observed at the smallest drain voltages VD. The result is obtained by the experimental work of [15,25].

The sensitivity of the device for both channel has been evaluated and the results are shown in Fig. 18. Here Fig. 18. Illustrates a proportional sensitivity, between the difference of the Hall voltage as a function of the direction of applied magnetic field for the differents values of the gate voltage Vg=0.1V, Vg=0.5V, and Vg=1V obtained in Fig. 3. There is a significant difference in sensitivity for the different gate voltages, but the high difference is observed at gate voltages near the threshold voltage VTH=0.44072V at B=0Tesla.

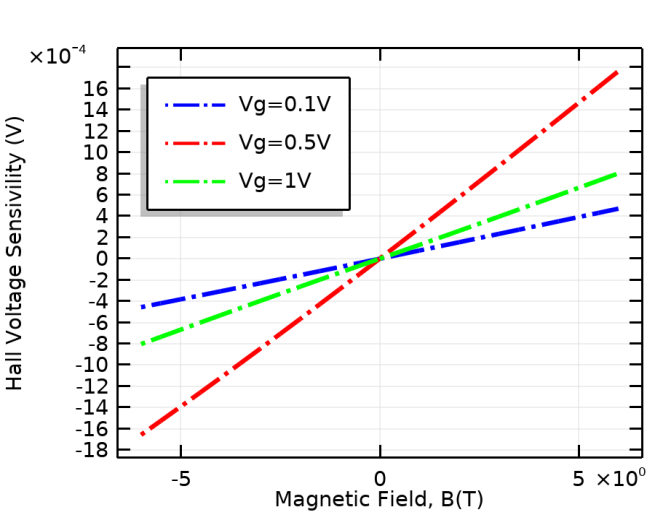
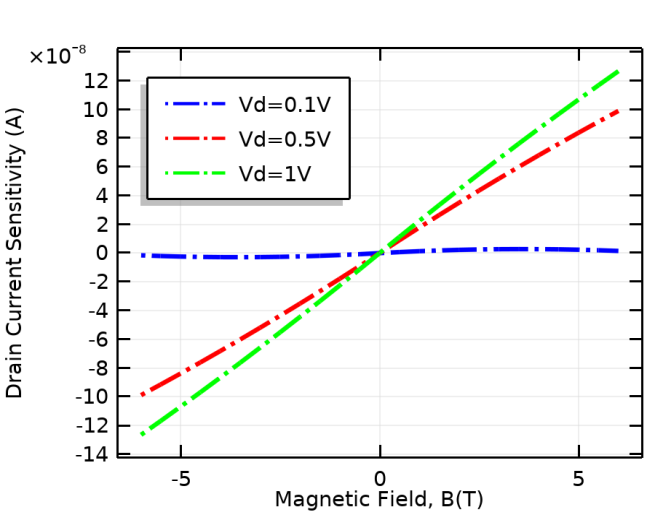


Figure 17. Drain current ID imbalance ΔID=ID1-ID2 against magnetics field.(Left image)

Figure 18. Hall voltage difference ΔVH=VH1-VH2 versus magnetics field.(Right image)

**3.3. DGMOSFET PERFORMANCE ANALYZES**

The performance of the MOSFET circuits was also analyzed and characterized in the sub-threshold region, where the source gate voltage VG was varied, while the source drain voltage VD was maintained at 50 mV. From these conditions, we calculate the different performance parameters of the DG MOSFET, the threshold voltage (VTH), ON current (ION), subthreshold leakage current (IOF), (ION / IOF) ratio, and the maximum of the magneto-transconductance (gmm). These parameters are very important for the operation of analog circuits since in this mode of operation the transistor consumes less energy [26,27].

In figure 19. The source drain current ID was evaluated for three magnetic field values, at B = 0T and within the magnetic field, B=+6T and B=-6T, was found to have the same behavior for both directions orientation of the magnetic field (positive and negative) so that the source drain current in the sub-threshold region and seems a little sensitive compared to the saturation region. The result shows that the source drain current ID is dependent on the field strength and independent of the direction of magneticfield orientation [11,18] in experimental studies. It is the same behavior for the maximum of the magneto-transconductance illustrated in fig. 20. This shows that the maximum of the magneto-transconductance decreases for the two orientation of magnetic field with respect to 0 teslas [18].

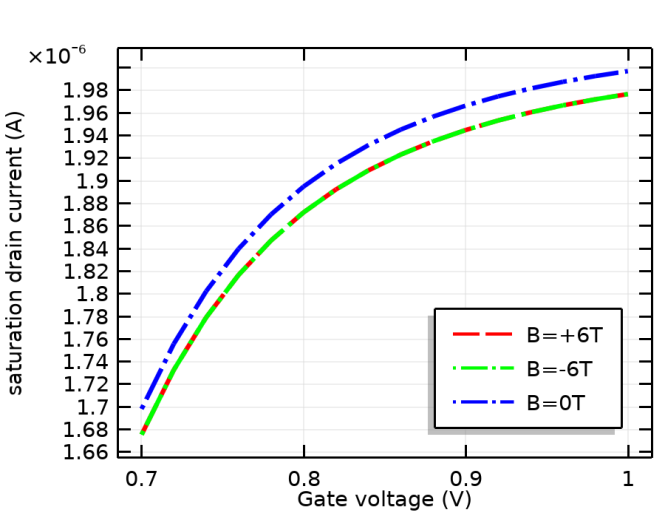
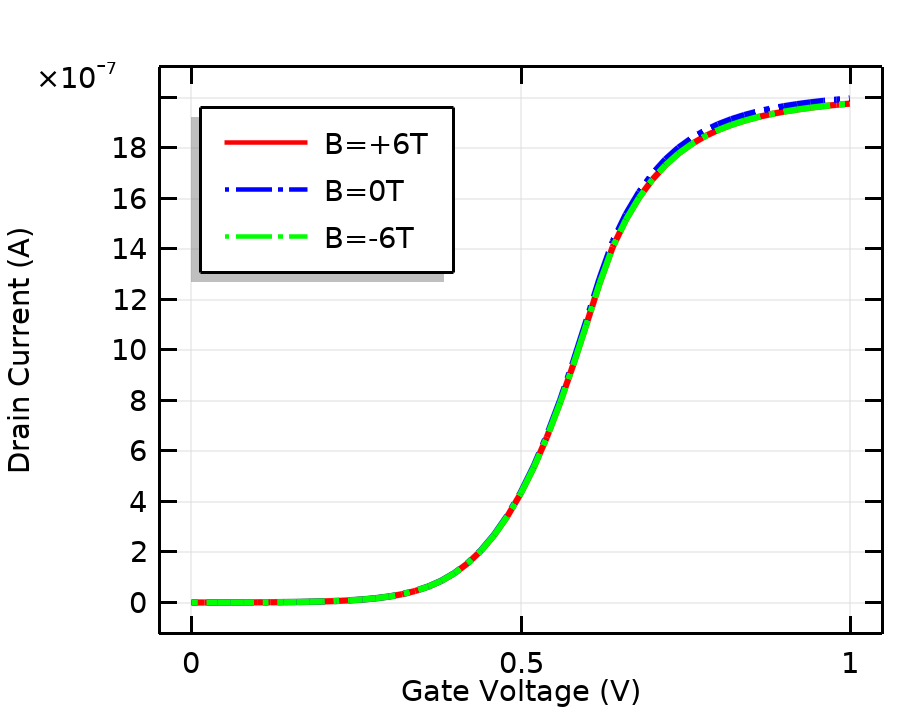


Figure 19a. Drain current ID against gate to source voltage (VG) when B=+6,-6 Tesla and B=0 Tesla at VD=0.05V [12-18-29].(Left image)

Figure 19b. Zoom in, on the Fig. 19a. of Saturation drain current ID against gate to source voltage VG when B=+6,-6 Tesla and B=0 Tesla at VD=0.05V [12-18-29].(Right image)

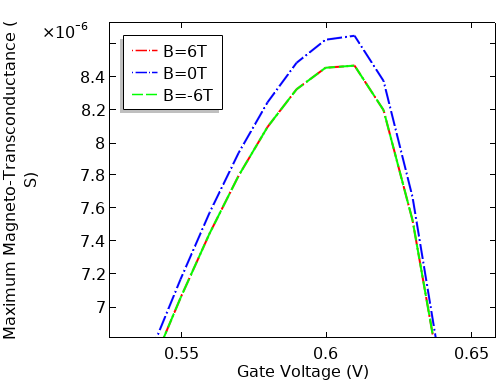
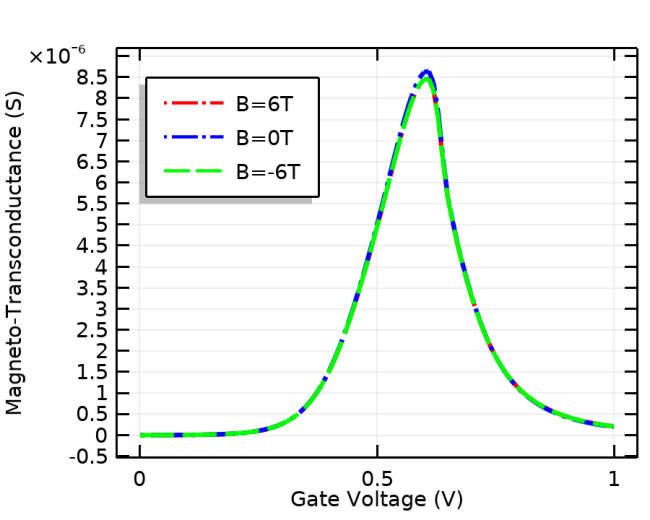


Figure 20a. Magneto-transconductance gmm against gate voltage VG, when B=+6, -6 and B=0 Tesla atVD=0.05V[12-18-29].(Left image)

Figure 20b. Zoom in, on the Fig. 20a. of Maximum of magneto-transconductance gmm against gate voltage VG, when B=+6, -6 and B=0 Tesla at VD=0.05V [12-18-29].(Right image)

The sensitivity of the two parameters, the drain current at the threshold voltage VTH and the maximum of the magneto-transconductance are evaluated as a function of the magnetic field B, are presented in Fig. 21. and Fig. 22. Respectively, the result illustrates a significant decrease in the two parameters studied. The reduction in drain current at the threshold voltage confirms the reduction of the threshold voltage as a function of the magnetic field shown in Fig.23.

The sensitivity of the threshold voltage VTH and the (Ion / Iof) ration considered as essential performance parameters of the MOSFET transistor is evaluated as a function of the magnetic field, and the results are shown in Fig. 23. Here, Fig. 23, shows that the threshold voltage VTH is reduced depending on the applied magnetic field, which will affect the applied switching gate voltages, noted that the threshold voltage is reduced by 10-3V for a magnetic field equal to ±6 Tesla. We also notice a significant disturbance of the ratio (Ion / Iof) shown on Fig. 24, knowing that for a magnetic field equivalent to ±5.5 Tesla, the ratio is reduced by 102, this reduction is considered as an adverse effect in CMOS technology.

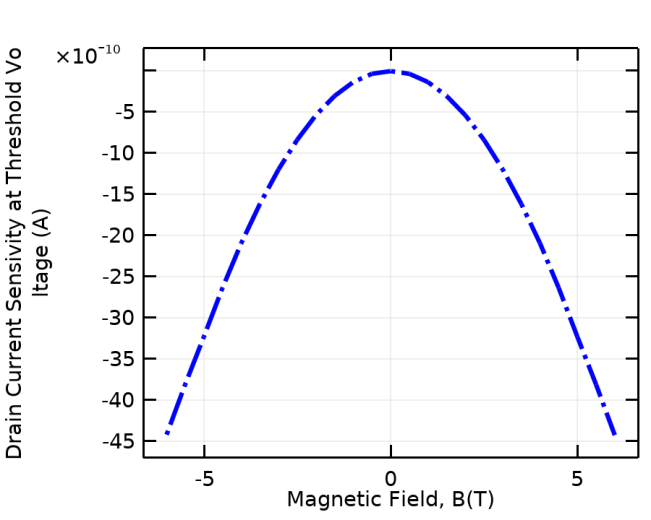
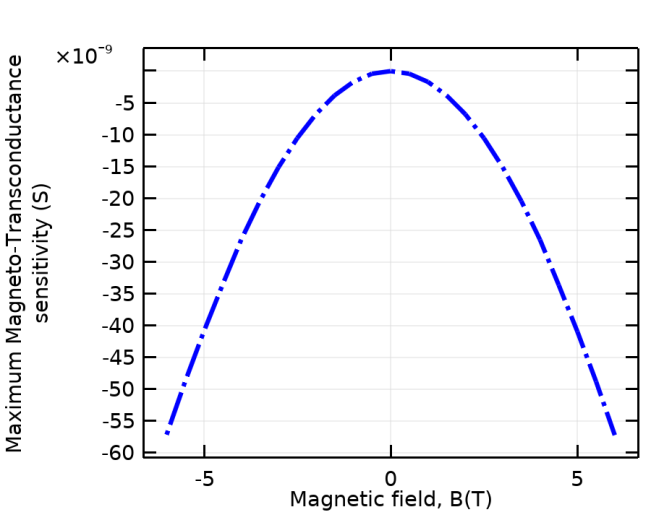


Figure 21. Maximum Magneto-transconductance difference Δgmm=gmm1-gmm2  against magnetic field B at VD=0.05V. (Left image)

Figure 22. Drain current difference at threshold voltage VTHagainst magnetic field B at VD=0.05V. (Right image)

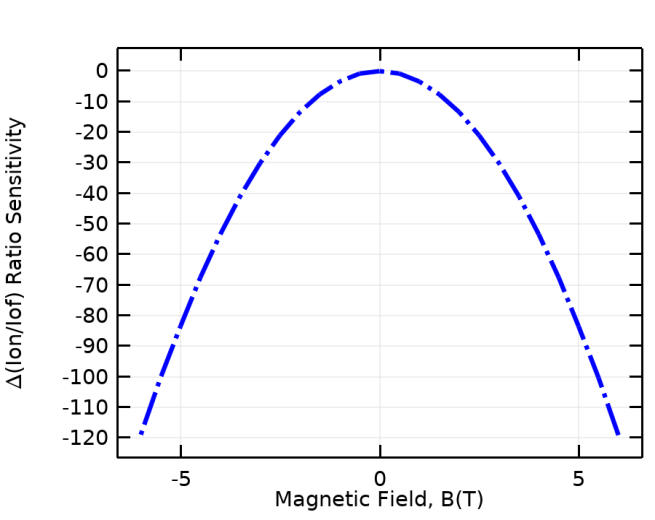
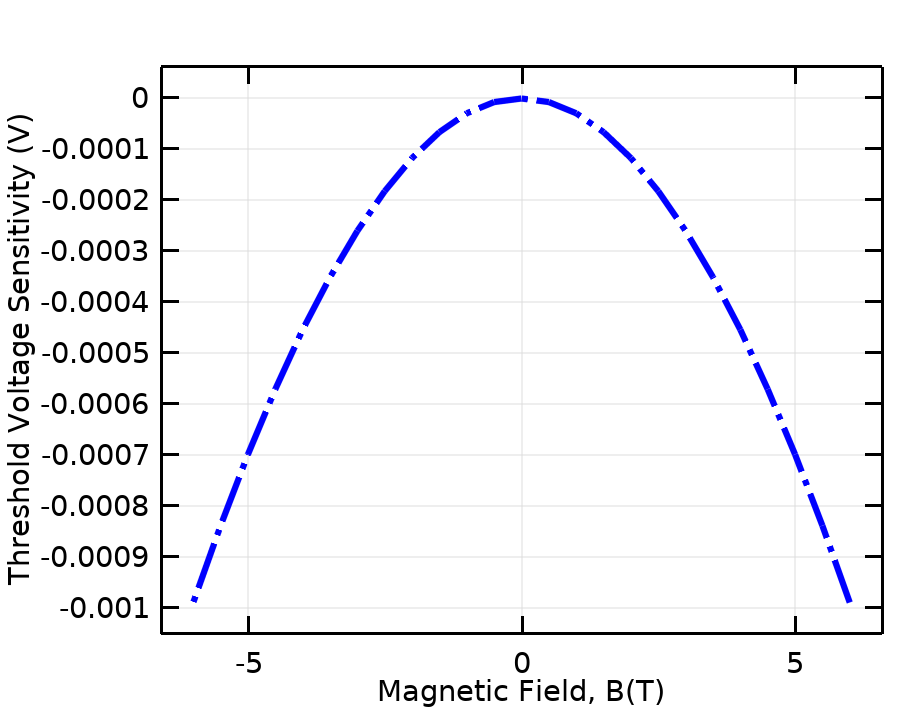


Figure 23. Threshold voltage (VTH) difference ΔVTH=VTH1-VTH2 against magnetic field (B) at VD=0.05V. (Left image)

Figure 24. (ION/IOF) ration difference Δ (ION/IOF) = (ION/IOF)1-(ION/IOF)2 against magnetic field B at VD=0.05V.(Right image)

1. **CONCLUSION**

This article presented our first numerical simulation of the effect of Hall field induced by a magnetic field on the electrical characteristics of the n-type channel DG MOSFET transistor.

It is shown that for short transistors, the Hall voltage VHpeaked for both directions of the magnetic field in the threshold region as expected in a shorter channel FET compared to the long channel FET, consistent with theory [28].

To mention again that the drain current (ID) for the variations of the drain voltage (VD) changes in both directions of the applied magnetic field perpendicular to the direction of flow of the drain current caused by the change in the amplitude of the layer charge inversion per unit area, which directly reflects the behavior of the magneto-conductance.

It is also shown that for short transistors, the drain current ID and the magneto-transconductance (gmm) for the variations of the gate voltage VG are reduced [18], and which are dependent on the intensity and independent to the direction of the magnetic field, Originates mainly by migration of electrons on the walls in hall surfaces and an imbalance of ionized charges fixed at the interface of the semiconductor oxide generated by the gate voltages which explains a decrease in the threshold voltage as a function of the magnetic field.

An undesirable effect observed concerns the reduction of the (Ion / Iof) ratio as a function of the applied magnetic field (B), which is one of today's requirements for CMOS technology.

As a perspective of this work, we began to study the different solutions to be developed to remedy its controlled parasites, quantified in order to reduce them (or even eliminate them).

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