Capacitance Study of Integrated Circuits Matrix Interconnects

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| **Article Info** |  | **ABSTRACT** |
| ***Article history:***  Received  Revised  Accepted |  | The evolution towards higher integration densities in integrated circuits with increasing operating frequencies reduced noise margin has led to multilayer integration technology. This results in many interconnection levels witch increase the parasitic capacitances between conductors.  The present work deals with the analysis of capacitance of multilayer conductor interconnect aiming for their possible exact extraction. We used three topologies of microstrip conductor interconnects and identified the potential distributor and then computed the capacitance and inductance matrix using a finite element method. The first analysis dealt with parallel microstrip conductors and the second with two levels (plan) of microstrip conductors The results are compared to those obtained by other methods and found quite encouraging. |
| ***Keywords:***  Interconnects  Multiconductor  Capacitance  Inductance  Integrated Circuits |
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1. **INTRODUCTION**

Metal interconnections are the main means of transporting signals in integrated circuits, which are currently constrained by the shrinking size and increasing frequency [1]. Studies show that the delay of the signal in an integrated circuit is related to its interconnections, limitations are imposed by the interconnection network to nanoscale technology to go far, the adverse effects that have been ignored by the integrated circuit designers cannot be ignored due to the complexity of the interconnection network and the increasing frequency of power supply, resulting in higher signal delay [2]. The radiation resistances, line inductances and capacitance of the interconnects continue to increase, Causing a significant increase in power supply noise [3]. So in order to ensure electromagnetic compatibility at the integrated circuit involves an effective reduction of noise sources and the sources of disturbances [4-5]. Electromagnetic modeling becomes necessary to ensure a predictive approach to all the risks of disturbances induced by electromagnetic interference [6-8]. This requires specific tools, models and knowledge in electromagnetic compatibility. The integrated circuit designer should take into account the capacitance and inductances that have not been considered previously, due to interconnection lengths and higher operating frequencies [9-11].

When designing and implementing integrated circuits, consideration should be given to the existence of parasitic capacitances between the interconnection lines and to providing methods for sufficiently reducing the influence of capacitive coupling either in led or radiated and improve their insensitivity to attacks from outside, in order to ensure reliable operation, in different use cases [12]. In order to ensure electromagnetic compatibility in the integrated circuit, an effective reduction of noise sources and the origin of disturbances are required[23-24]. Modeling of these facts becomes mandatory to ensure a predictive approach to the risks of disturbance induced by electromagnetic interference.

The modeling of all high-performance systems, such as the design of integrated circuits is based on numerical capacitance and inductance field calculation methods; capacitance calculation has drawn the attention of IC designers to the complexity of interconnection networks. The simulation tools must make it possible to define an overall specification of the system to be studied, but the difficulty lies in passing on the noise margins on the system [13].

The increase in integrated circuit integration density has led to considerable development of micro and nanoscale technologies. However, this evolution required a large number of interconnects and significant lengths of conductors used for this purpose in a superposition of microstrip planes[25]. In [14] starting from several reasonable approximations, a closed-form expression for the mutual impedance per unit length of coupled IC interconnects with silicon substrate have been proposed [15], the study of transmission lines and waveguides in quasi-TEM mode is done. We can mention, finite difference methods (FDM) [16], Variational method [17], the method of moment [18], the Green’s function approach [19], the Galerkin method [20], Finite Element Method [21].

In this work, we design two deferent geometry of line interconnects in two dielectric regions. The geometries of the studied model are designed in 2D, the finite element method is used for solving the propagation equation, and then a comparison of the results with galerkin and moment methods is carried out. This work aims at modeling electromagnetic phenomena and more specifically the parasitic effects between the lines of an interconnected network within an integrated circuit to predict possible electromagnetic compatibility (EMC) problems of integrated circuits. Our approach which is based on the finite element method is efficient and fast for the calculation of inductance and capacitance matrices for the type of non-homogeneous structures like the interconnects.

1. **MATHEMATICAL ANALYSIS**

The basic approach of the finite element method is to subdivide the field of study into finite numbers of subdomains called elements. For electromagnetic problems that are to be solved to evaluate the capacitance matrix of the parallel microstrip line, the general algorithm starts with a function that has the dimensions of system energy associated to the partial differential equation describing the two-dimensional distribution

|  |  |
| --- | --- |
|  | (1) |

To find the equation of electrical potential for the region between tracks, we will associate the conditions to the limits of types Dirichlet and Neumann, with the electrical permittivity ε(x, y) is a function of the position. The equation to be minimized in this situation is given by

|  |  |
| --- | --- |
|  | (2) |

The potential distribution is defined within each subdomain as a result

|  |  |
| --- | --- |
|  | (3) |

The per-unit length capacitance of each track can be writing

|  |  |
| --- | --- |
|  | (4) |

Where We are the energy given by

|  |  |
| --- | --- |
|  | (5) |

The capacitance coefficients for a system of parallel microstrip lines are defined as follows, it is convenient to write [22]:

|  |  |
| --- | --- |
|  | (6) |

Where *Vj* is the voltage of *j* th conductor with reference to the ground plane, Qi is the charge per unit length, Csij is the short circuit capacitance between *i* th and *j* th conductor. Short circuit equivalent capacities can be obtained as follows:

|  |  |
| --- | --- |
|  | (7) |

|  |  |
| --- | --- |
|  | (8) |

Where Cij is the capacitance per unit length between the *i* th conductor and the ground plane. The coupling capacitances are illustrated in Figure 1.

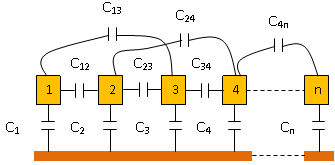


Figure 1. Per unit length capacitances of general n conductors<

The matrix [c] capacitance for n conductor is given by

|  |  |
| --- | --- |
|  | (9) |

|  |  |
| --- | --- |
|  | (10) |

Where,

[L] = Inductance matrix.

[C]-1 = the inverse matrix of the capacitance of the multiconductor transmission line when all dielectric constants are set equal to one.

μ0 = permeability of space or vacuum.

ε0 = permittivity of free space or vacuum.

The characteristic impedance and capacitance per unit length are related as follows:

|  |  |
| --- | --- |
|  | (11) |

The electrical parameters are:

Capacitance per unit length matrix ([C] in pF/m), inductance per unit length ([L] in nH/m), impedance ([Z] in Ω).

1. **RESULTS AND DISCUSSIONS**

To illustrate and validate the new proposed formulation, in the first section we consider a planar interconnects line including four strips In a two-layer dielectric medium we determine the capacitance and inductance matrix using the finite element method, Figure (2) shows the geometry of the model.

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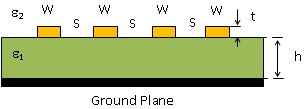
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Figure 2. Symmetric microstrip coupled interconnect

This microstrip coupled interconnects have the following geometrical parameters:

ω1= ω2 = ω3 = ω4 =20 μm, S=20 μm, h=40 μm, t= 5 μm, ε1=11.7, ε2=3.9

Figure (3) shows mesh by finite element, the basic approach of the finite element method is to subdivide the field of study into finite numbers of subdomains called elements. The approximation of the unknown is done in each element of the interpolation functions.

The interpolation function is also defined according to the geometry of the element that is chosen beforehand and coincides with the nodes of this element relative to the values ​​of the unknown.

The figure (4) shows the surface potential distribution we Note that the value of potential increases as it gets closer to the carbon nanotube track that is powered.

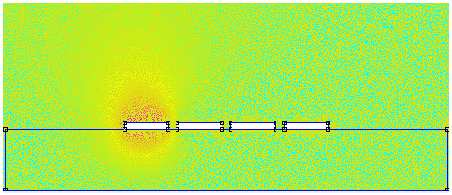
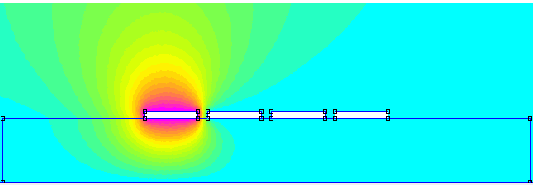
 

Figure 3. Mesh of four strip conductor system Figure 4. Surface potential distribution

The capacitance per unit length of the multistrip transmission lines are related as follows:



Table 1 shows the FEM results for the self-capacitance per unit length of the fourth conductor transmission lines interconnect with two dielectric layers. They are compared with the Galerkin method.

Table 1. Capacitance matrix of the model in figure 2

|  |  |  |
| --- | --- | --- |
| Capacitance (10-10F/m) | Galerkin method | Our work |
| C11 | 0.475 | 0.968 |
| C12 | -0.582 | -0.328 |
| C13  C14  C22 | -0.114  -0.062  0.289 | -0.08  -0.01  1.126 |

The inductance per unit length matrix is:



The impedance per unit length matrix is:



In the next section, we demonstrate our work with modeling as four two-level interconnect lines with two dielectric layers. Our calculation is fixed on the calculation of the inductance and capacity matrix, Figure (5) shows the geometry of the model.

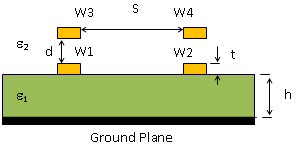


Figure 5. Symmetric Two-level microstrip coupled interconnect

This microstrip coupled interconnects have the following geometrical parameters:

* ω1= ω2 = ω3 = ω4 =20 μm, S=60 μm, h=40 μm, t= 5 μm, *d*=30 μm, ε1=11.7, ε2=3.9

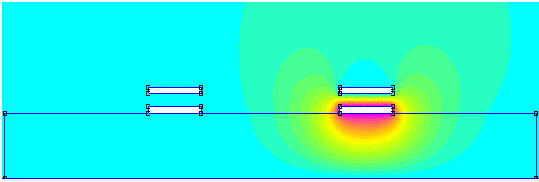
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Figure 6. Surface potential distribution of two strip two levels conductors lines

The capacitance per unit length of the multistrip transmission lines are related as follows:



Table 2 shows the FEM results for the self-capacitance per unit length of the fourth conductor transmission lines interconnect with two dielectric layers. They are compared with the Moment method.

Table 2. Capacitance matrix of the model in figure 5

|  |  |  |
| --- | --- | --- |
| Capacitance (10-10F/m) | MoM | Our work |
| C11 | 7.158 | 6.921 |
| C12 | -1.284 | -1.251 |
| C13  C14  C22  C33  C44 | -1.296  -2.224  8.732  13.39  14.11 | -1.312  -2.104  8.602  12.86  14.01 |

The inductance per unit length matrix is:



The impedance per unit length matrix is:



Capacity is found to be less important in the first case than in the second case

In this part, we have to demonstrate the effect of the geometry of the interconnection track on the values ​​of parasitic capacitance. We consider the same geometry for the figure (2) and figure (5). The calculation of the matrix [C] for the given cut is made by making various parameters.

The parameters studied are:

t, the thickness of the track varying from 5 to 10 μm.

h, the height of the oxide, ranging from 40 to 100 μm.

Table 3. Parameters values of five case were simulated

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Parameters  (μm) | 1 | 2 | Case  3 | 4 | 5 |
| W | 20 | 20 | 20 | 20 | 20 |
| S  t  h | 60  5  40 | 60  10  40 | 60  5  80 | 60  10  80 | 60  5  100 |

A general analysis makes it possible to notice that the capacitances towards the mass, C11 and C22 decrease with the increase of the distance h, concerning the plane of mass as show in figure (7). At the same time, the C12 and C13 capacities vary in phase, with the increase in h. on finding that the wider the track, the greater the parasitic coupling between the lines.



Figure 7. Capacitance per unit length vs of geometry track (of figure 2)

All abilities decrease with distance to the ground plane. This evolution can be explained by the fact that we combine the increase of the distance between the track, in order to locate an optimum layer thickness corresponds to the thickness for which the parasitic capacitance-to-capacitance ratio mass is the lowest as show in figure (8).



Figure 8. Capacitance per unit length vs geometry of track (of figure 5)

1. **CONCLUSION**

In this paper, we were able to model the four-conductor interconnects lines with two dielectric layers, we have identified the potential distribution of different geometries of the interconnection lines. The capacity matrix and the inductance for each of the geometries have been calculated. Some geometric parameters have also been varied to remedy the problems of parasitic capacitances. We have found that as the thickness of the dielectric layer increases, the parasitic capacities between the tracks increase with the levels of interconnection, and the higher the level of interconnection, the capacities towards the ground plane tend to become weak. The results obtained with the finite element method agree with those in the literature.

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