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Estimation of Power and Delay in CMOS Circuits using LCT

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Abstract

With a rapid growth in semiconductor Industry, complex applications are being implemented using small size chips, with the use of Complementary Metal Oxide Semi-Conductors (CMOS). With the introduction of new Integrated Circuit (IC) technology, the speed of the circuits has been increased by around 30%. But it was observed that for every two years, the power dissipation of a circuit doubles.The main reason for this power dissipation is leakage currents in the circuit. To reduce these leakage currents, we can reduce the width of the device. In addition to this, we can use lector techniques that use Leakage Control Transistors (LCT) and High Threshold Leakage Control Transistors (HTLCT).In this paper; we present a circuit technique that uses 130 nano-meter CMOS VLSI circuits that use two extra transistors to mitigate the leakage currents. The proposed technique overcomes the limitations posed by the existing methods for leakage reductions an average leakage reductions is 82.5%.The estimation of power and delay will be discussed using LCT's and HTLCT's.

***Keywords**: VLSI, CMOS, IC, Leakage Current, LCT, HTLCT, Power Dissipation, Time Delay.*

1. Introduction

As the impact of electronic systems on every walk of life is becoming more and more, the demand for very low cost, very small and very reliable systems is also increasing exponentially. The rapid development of the semiconductor technology is leading to very tiny systems that have the power of super-computers of the last decade. Designing such tiny systems is now being witnessed in every field mobile communications, industrial electronics and ubiquitouscomputing.Electronic circuits are characterized by reliability, low power dissipation, extremely low weight and volume and effective cost with a high degree of computations and complexities. The advancements in technology mainly contributed towards the miniature in transistor size, reduced power supply consumption and enhancement of services with reliability as a major factor.VLSI Technology has been the enabler for the advancement of the present electronics andcommunication age. Almost 90% of the electronic circuits fabricated worldwide are made of silicon using CMOS technology[1-2]. For relatively high performance and cost-effective[3] VLSI circuits, CMOS technology is used. It is the most popular technology because of its low power and less area requirement[4].Scaling of CMOS technology improved the speed however the leakage currents[5] are leftover as an adverse effect. These unsolicited leakage currents should be reduced for the smooth functioning of the circuits. LECTOR Technique[6-8] is the technique to reduce leakage power consumption[9] in CMOS circuits without affecting the dynamic power[10-11] of the circuit.In this paper, the performance of parallel adder-subtractor implemented with NAND gates using LECTOR technique is compared to the basic model and power dissipation and delay are compared.

/.Conventional Principles and Techniques

I. A NAND GATE

The fundamental building blocks of digital systems are logic gates. They are circuits in which the output depends upon the inputs according to the logic rules. The electronic circuits that operate on one or more input signals to produce an output signal are known as logic gates.

The NAND gate is called a Universal gate because it can perform all the three basic functions of AND, OR, NOT gates. The NAND gate is a AND gate followed by NOT gate. It is

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a NOT- AND operation. It may have two or more inputs but only one output. The logical symbol of NAND gate is given below:

The truth table of a NAND gate:

A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

It is clear from the truth table of two input NAND gate that the output is 1 when either A or B or when both the inputs are at logic '0'. For all input value combinations AND gate output is exactly opposite to the output of NAND gate. The logical expression for the output is givenby:

$$Q = \overline{AB} = \bar{A} + \bar{B}$$

The NAND gate can perform the OR function by inverting the inputs. The OR gate with inverted inputs is called bubbled OR gate or negative OR gate. The NAND gate is also called active low OR gate.

I. B EXCLUSIVE-OR GATE (XOR)

A basic XOR gate is a two-input single output logic gate, whose output is assumed to be HIGH only when one and only one of its inputs are HIGH. XOR can simply be defined as one or the other but not both.

Fig 1.1 Logical representation of XORgate

If input variables are represented by A and B then the logical expression for output is givenby

$$Q = A\bar{B} + \bar{A}B$$

XOR gate is known as an odd number of 1's detector in the input.

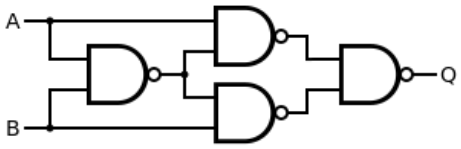


Fig 1.2 Realization of XOR Gate using NAND Gate

The truth table of XOR gate:

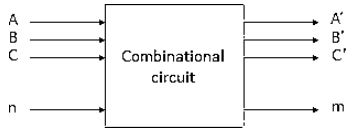
A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

The most important application of XOR gate is in parity generation and detection. It is also known as staircase switch. XOR gate acts as an inverter for control input of logic '1'.

I. C COMBINATIONAL LOGIC CIRCUITS

The circuit which consists of an interconnection of logic gates whose outputs at any instant of time are determined from a present combination of inputs only is defined as a combinational

logic circuit. The ‘n’ input binary variables come from external sources; the combinational logic circuit produces ‘m’ output variables by the internal logic connections and go to an external destination. Every input and output variables are contacts physically as an analog signal whose values are interpreted to be a binary signal that represents logic high and logic low



For ‘n’ input variables, there are 2^n possible combinations of binary inputs.

I.D FULL-ADDER

The combinational circuit that performs the arithmetic sum of three input bits is known as a Full-Adder. It consists of three input variables designated by augend, addend and the carry bit. The two output variables produce the SUM and CARRY.

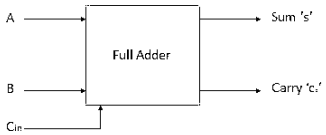


Fig 1.3 Block Diagram of Full Adder

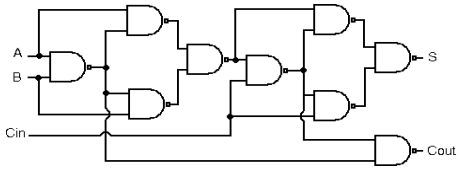


Fig 1.4 Full Adder realization using NAND gate

From the truth table given below, the logical expressions for Sum (S) and Carry (C_{out}) are:

$$S = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC = A \oplus B \oplus C$$
$$C_{out} = AB + BC + CA = AB + C\,(A \oplus B)$$

Input			Output	
A	B	C	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

I. E PARALLELADDER-SUBTRACTOR

A binary parallel adder-subtractor is a combinational digital circuit that adds two binary numbers in parallel form. It consists of full-adders connected in cascade with output carry from each full adder connected to the input carry of the next full adder. The mode bit ‘M’acts a control line i.e. depending on the value of M, the circuit acts as an adder or subtractor. The circuit shows Parallel Adder-Subtractor realized using Full Adders.

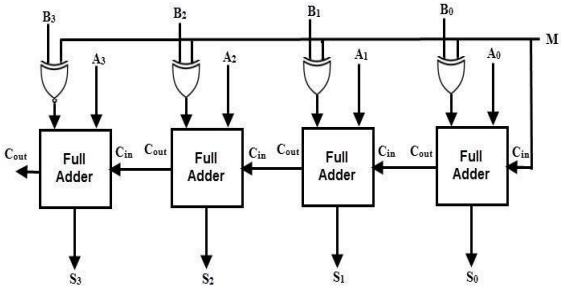


Fig.1.5. Four bit Parallel adder

When M is driven low (M=0) then one input to each and every XOR gate would be logic '0'. This results in un-altered XOR outputs. Also, Cin of the first full adder would be low. The cascaded circuit will act as a parallel adder. When M control line is pulled high (M=1) then one of the inputs to each XOR gate would be logic '1'. This results in complemented bits as XOR output which is fed as an input to each full adder circuit. Also, Cin of the first full adder would be logically high. As a result, the cascaded arrangement will act as a parallel subtractor.

I. F CMOS LOGIC FAMILY (NAND gate)

A CMOS (Complementary Metal Oxide Semi- Conductor FET) logic family is obtained by connecting a p-channel and an n-channel MOSFET in series to realize several advantages over the PMOS and NMOS families. In CMOS, p-channel and n-channel MOS devices are fabricated on the same chip. It makes the CMOS fabrication more complicated and reduces the package density. The important advantages are high speed and low power consumption. They can also be operated in high voltage resulting in improved noisemargin.To implement the CMOS NAND gates, the NMOS transistors are connected in series and the PMOS transistors are connected in parallel. For a given Silicon area, the 'ON' resistance for NMOS is less than that of the PMOS. CMOS NAND gate is generally faster than NOR gate. CMOS NAND gate and truth table are givenbelow.

When the inputs A and B are high, PMOS transistors are open circuited and NMOS transistors are short-circuited resulting in zero output. If any of the inputs is low, PMOS transistors are short- circuited and NMOS transistors are open circuited providing a high output. The truth table shows the possible operation of NAND gate usingCMOS.

Inputs		Outputs	
A	**B**	**Y**	**Logic**
0	0	Vdd	1
0	1	Vdd	1
1	0	Vdd	1
1	1	GND	0

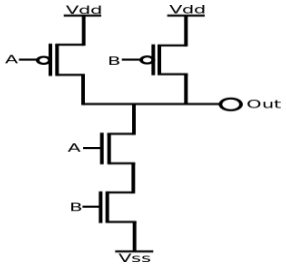


Fig1.6.CMOS NAND Gate

*II **Proposed LECTOR Technique***

In the design of CMOS VLSI circuits, power dissipation is one of the major considerations. The minimization of the threshold voltage due to voltage climb up leads to increase in sub-threshold leakage current and static power dissipation in CMOS circuits.

CMOS gates are designed using LEakage Control TransistOR (LECTOR) Technique which results in the reduction of the leakage current without any impact on dynamic power dissipation.In any supply to ground path, a state with more than one transistor OFF in a path from the source voltage to earth is far less leaky than a state with only one transistor OFF. Two leakage control transistors are introduced in every CMOS logic gate such that one of the LCT's is near its cut-off region of operation.

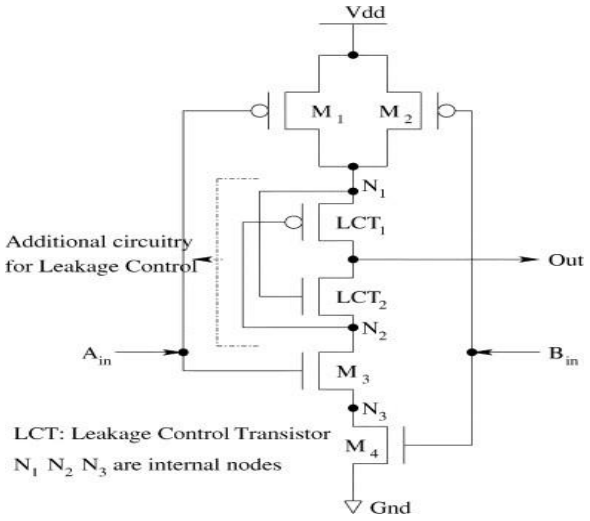


Fig.1.7. Two input LCT NAND gate. The leakage control transistors LCT1 and LCT2 are inserted between the nodes N1 and N2 and they act as self-controlled stacked transistors.

In this paper, we implement LECTOR Technique with NAND gate. A CMOS NAND gate with the addition of two leakage control transistors is shown in the Fig.1.7.Two leakage control transistors LCT1 (PMOS) and LCT2 (NMOS) are introduced between the nodes N1 and N2 of the pull-up and pull-down logic of the NAND gate. The drain terminals of the transistors LCT1 and LCT2 are wired together to form the output node of the NAND gate. The source terminals of the transistors are wired to nodes N1 and N2 of pull-up and pull-down logic respectively. The switching of the transistors LCT1 and LCT2 are controlled by the voltage potentials at nodes N2 and N1 respectively. This configuration ensures that one of the LCT's is always near its cut-off region irrespective of the input vector applied to the NAND gate [3]. LECTOR does not require any other additional control circuitry to monitor the states of the circuit. Self-biased transistors have their gate and their drain terminals wired together as a single node. Thus no external control circuitry isrequired.

III. ***Simulation Results and Discussion***

Basing on the schematic model of the parallel adder-subtractor, the conventional and LECTOR models are simulated in Mentor Graphics. The parallel adder-subtractor is realized using the NAND gates throughout the simulation. By varying the supply voltage, power dissipation and delay are observed for each voltage and adder-subtractor inputs. The values for both conventional and LECTOR models are recorded for further comparisons and observations.

The adder-subtractor inputs are considered as shown in the below tables. As discussed in section I.E, the model acts as an adder when Mode M =0 and as a subtractor for mode M=1.

Mode 0	**A1**	**B1**	**S1**	**C1**
	0	1	1	0
	1	0	1	0
	0	0	0	0
	A2	**B2**	**S2**	**C2**
	0	1	1	0
	1	1	0	1
	1	0	1	0
	A3	**B3**	**S3**	**C3**
	1	1	0	1
	0	1	0	1
	1	1	0	1
	A4	**B4**	**S4**	**C4**
	1	1	1	1
	1	1	1	1
	0	0	1	0

Let 010 and 100 be the inputs A1, B1 to the first full-adder in simulated Parallel Adder-Subtractor circuit. When the Mode input M is ‘0’, the circuit will act as an adder. The Carry input for the first full adder will be 0. The XOR gate takes B and Mode as inputs and gives B as its output as M=0. The Full-Adder will then add A, XOR output, Cin and gives S1 and C1 as its outputs. C1 will act as an input carry for the next full-adder. The operation will be carried out similarly through the remaining circuit till S4 and final Carry are obtained.Similarly, when the Mode input M is ‘1’, the circuit will act as a subtractor. The Carry input for the first full adder will be 1. The XOR gate takes B and Mode as inputs and gives complement of B as its output as M=1. The Full-Adder will then add A, XOR output, Cin and gives S1 and C1 as its outputs. C1 will act as an input carry for the next full-adder. The operation will be carried out similarly through the remaining circuit till S4 and final Carry areobtained.

Mode 1	**A1**	**B1**	**S1**	**C1**
	0	1	1	0
	1	0	1	1
	0	0	0	1
	A2	**B2**	**S2**	**C2**
	0	1	0	0
	1	1	0	1
	1	0	1	1
	A3	**B3**	**S3**	**C3**
	1	1	1	0
	0	1	1	0
	1	1	0	1
	A4	**B4**	**S4**	**C4**
	1	1	1	0
	1	1	1	0
	0	0	0	1

The outputs of a basic parallel adder-subtractor and LCT parallel adder-subtractor are plotted for the considered inputs as described in table IV.

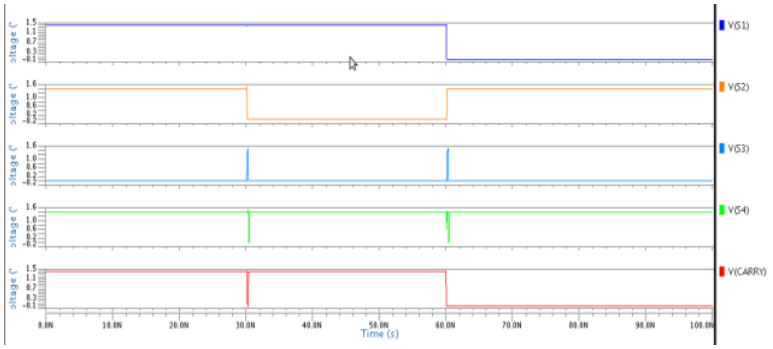


Fig.1.8.Basic Parallel Adder

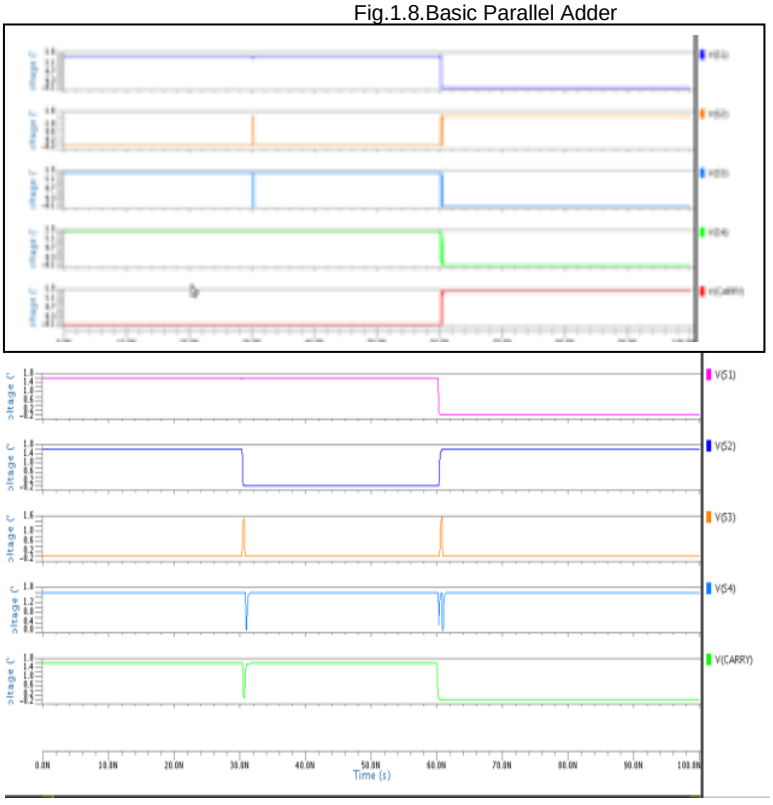


Fig.1.9.LCT Adder

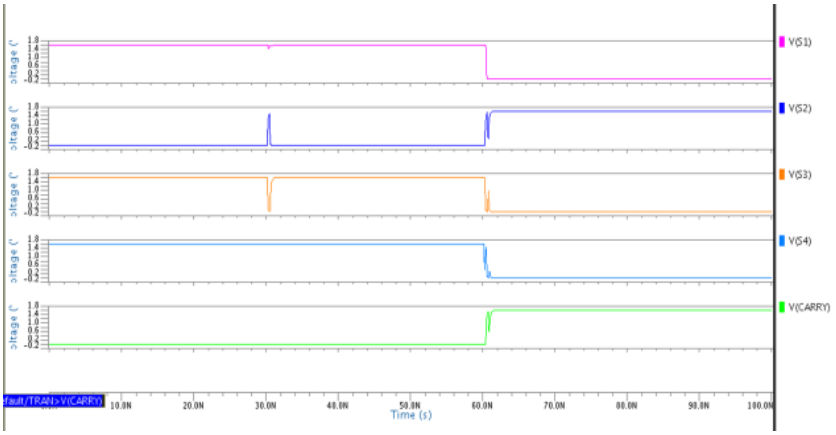


Fig.1.10.LCT Subtractor

	Voltage	Power Dissipation(nW)	Delay(ps)				
			S1	S2	S3	S4	C4
Mode 0	1	49.4405	178.85	268.08	503.65	564.79	103.79
	1.2	55.5687	137.76	209.94	391.95	436.61	79.439
	1.4	72.2754	114.95	176.23	329.13	363.61	65.995
	1.6	92.0056	100.60	156.13	283.50	318.49	57.405
	1.8	115.3078	90.891	141.53	262.87	287.68	51.622

Table-I: Power Dissipation and Delay of a Basic Parallel Adder-Subtractor in Adder Mode (M=0)

	Voltage	Power Dissipation(nW)	Delay(ps)				
			S1	S2`	S3	S4	C4
Mode 1	1	37.0195	336.11	479.73	458.25	177.75	613.07
	1.2	49.5823	259.72	370.37	355.16	137.74	471.71
	1.4	64.4102	216.97	309.73	297.78	124.46	392.69
	1.6	81.8852	190.22	271.77	262.03	120.38	343.64
	1.8	102.4766	172.14	245.95	237.44	100.35	310.42

Table-II: Power Dissipation and Delay of a Basic Parallel Adder-Subtractor in Subtractor Mode (M=1)

	Voltage	Power Dissipation(nW)	Delay(ps)				
			S1	S2	S3	S4	C4
Mode 0	1	39.0280	664.75	994.99	1721	723.68	376
	1.2	51.6831	427.66	637.52	1119	459.24	237.52
	1.4	66.5318	319.56	482.33	850.34	379.85	175.21
	1.6	83.8677	261.97	397.90	704.96	338.96	140.44
	1.8	104.0790	225.61	345.99	614.11	307.68	119.39

Table-III: Power Dissipation and Delay of an LCT Parallel Adder-Subtractor in Adder Mode (M=0)

	Voltage	Power Dissipation(nW)	Delay(ps)				
			S1	S2`	S3	S4	C4
Mode 1	1	35.2997	1338.2	1381.45	683.32	682.16	1282.30
	1.2	45.2043	840.63	892.71	432.42	432.16	817.06
	1.4	59.6495	624.35	671.72	322.84	322.40	617.12
	1.6	76.9218	509.01	559.55	263.48	263.15	508.87
	1.8	94.4894	438.75	493.38	226.90	196.48	443.06

Table-IV: Power Dissipation and Delay of an LCT Parallel Adder-Subtractor in Subtractor Mode (M=1)

The power dissipation and delay are the most important factors to measure the performance of the circuits. Actual power delivered by the circuit is measured as the power dissipated by the circuit. The time taken to propagate the input signal from the gate to the output of the gate is considered as adelay.When the speed of operation is important, each circuit must have a short propagation delay. As the number of logic levels decreases, delay decreases.The power dissipation and delay of a basic parallel adder-subtractor model acting as an adderi.e. when M=0 is given in the Table- I and as a subtractor when M=1 is given in Table-II. Voltage is varied and delay and dissipation are recorded for each varied input.Similarly, the power dissipation and delay of an LCT parallel adder-subtractor model acting as an adder i.e. when M=0 is given in the Table- III and as a subtractor i.e M=1 is given in Table-IV. Voltage is varied and delay and dissipation are recorded for each variedinputs.The proposed Techinque is overcomes the inhibitations of abshed by the another related methods leakage current dimnishments and efficiency measurements comparision are shown in below table V

S.No	Topologies	Efficiency (%)
1	Reference[6]	79.40
2	Reference[7]	79.85
3	Proposed Technique	82.50

Table-V: Efficiency analysis for LCT leakage current

IV CONCLUSION

Power dissipation and delay are the major parameters that affect the performance of the circuit. The performance of a simulated basic parallel adder-subtractor model and the LCT parallel adder-subtractor simulated model is compared. The parallel adder-subtractor with LCTs offer a reduction in leakage power as the LCT is in near cut-off region always. However, the increase in a number of logic levels increases the delay as the delay is considered by taking the average of delays at the gates of each logic level. The proposed technique overcomes the limitations posed by the existing methods for leakage reductions an average leakage reductions is 82.5%.When the speed of operation is needed, the reduction in a number of logic levels will improve the performance of the circuit decreasing the delays.

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