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Study of Different Parametric Variations of MOSFET Pressure Sensor

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ABSTRACT

There is a growing demand of miniaturization of the electronics world. A brief discussion for simulating and fabrication of the MOSFET based pressure sensor in nanoscale is being reviewed in this paper. Aim of this paper is to collect all the scaling challenges and their solutions together to make understanding the facts of the MOSFET based sensor. As the MOSFET move from micro scale to nanoscale the functioning changes dramatically. The Silicon oxide material fails when scale down to nano region. However, many issues such as electrical quality, thermodynamic stability, Kinetic stability, gate compatibility and process compatibility were being solved in the process of integration and implementation.

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1. INTRODUCTION

Micro electronics have a great importance and has infiltrated in our life since last decades, from radio to television to the handy cellular phone in our hand which can collect any information by connecting to internet. The growing up demand of miniaturizing the device and faster operation is the reason for boosting up the technology to move beyond its limits. Microelectronic need low cost and high performance to go ahead. The most effective way to improve performance and reduce costs is to shrinkage or scaling down of the device. But by thinning of the silica (SiO_2) gate oxide beyond 2nm the channel length gets reduces and this nearness in the source and drain looses the control over MOSFET operation through gate terminal. This instability in device structure by reduction in channel thickness of MOSFET is mainly due to the short channel effect (SCEs) like threshold voltage roll-off, gate leakage current, drain induced barrier lowering (DIBL), hot electron effects (HECs). SCEs results in increasing the leaking current between the drain and source and reduces ON to OFF state ratio current [11].

The concept of integrating MEMs structures with microelectronics on a single chip is widely being used for the development of smart sensors for health care and biomedical applications [15]. The implementation of these sensors requires a sensing technique that is fully compatible with the standard CMOS circuitry for extracting the sensor's output signal. Pressure sensors based on MOSFET sensing have been proposed and developed by different researchers [13], [14]. In this project we are going to study the MOSFET behaviour for the various channel thickness in nanometre range for making a "MOSFET based pressure sensor". Piezoresistive pressure micro sensor is one kind of the most widely used pressure sensors for automotive, aerospace, biomedicine and many other applications, but these are having certain limitations like sensitivity, e.g. it cannot sense the presence of a very low weighing molecule having a weight of few nanogram [1]. This issue of high sensitivity can be solved by using a MOSFET pressure sensor. This pressure sensor is having a diaphragm along with two MOSFETs and two resistors arranged in a form of wheatstone

bridge as mentioned by zhan0g et al [5]. In this paper we have presented the increasing sensitivity of MOSFET pressure sensor with reduction in thickness of channel.

1.1. Background

Computing power has increased dramatically over the decades, enabled by significant advances in silicon integrated circuit (IC) technology led by the continued miniaturization of the MOS transistor. Circuit performance and functionality together with reduced manufacturing costs are the driving force for the rapid growth in semiconductor industry. Since the 1960s, MOS transistor dimensions have been shrinking 30% every 3 years, as predicted by Moore's law [5]. The bulk-silicon MOSFET has been the backbone of the semiconductor trade over the last forty years. However, the scaling of bulk MOSFETs becomes progressively troublesome for gate lengths below ~20nm (sub-45 nm half-pitch technology node) expected by the year 2009, because the gate length is reduced, the electrical phenomenon coupling of the channel potential to the supply and drain will increase relative to the gate, resulting in considerably degraded short-channel effects (SCE). This manifests itself as a) exaggerated off-state discharge, b) threshold voltage (VTH) roll-off, i.e. smaller VTH at shorter gate lengths, and c) reduction of VTH with increasing drain bias owing to a modulation of the source-channel potential barrier by the drain voltage, additionally referred to as drain-induced barrier lowering (DIBL). to take care of the comparatively sturdy gate management of the channel potential in bulk devices, varied technological enhancements like ultra-thin gate dielectrics, ultra shallow source/drain junctions, halo implants and advance channel doping profile engineering techniques like super-steep retrograde wells are necessary. Every of those technologies is currently approaching basic physical limitations which can, in turn, limit any scaling of device dimensions.

1.2. The Problem

Now the problem arises when we go for miniaturization of size of MOSFET. If we try to reduce the thickness below 2 nm in silicon oxide MOSFET there will be a free flow of drain current through the channel as reported by saeed et al [1]. The solution to this problem is also suggested by saeed et al [7] in the same literature that for obtaining a proper flow of drain current through channel we need to replace silica with a material having high k Value (or high Di-electric constant). While exchange the oxide with a high di-electric material some factors has got to be thought of, these factors are:

a. Material ought to be able to continue scaling to lower equivalent compound thickness.
b. stop the gate threshold voltage instabilities caused by the high defect densities
c. Limit the loss of carrier quality within the Si channel once mistreatment High-κ oxides
d. Warrant dependability of the gate material.

1.3. The Proposed Solution

paper summarized the challenges and problems faced on scaling down the channel width of the MOSFET or ultimately scaling down the MOSFET size. Thus, they have suggested various insulating material for MOSFET having high dielectric constants which can be a replacement for the standard oxide layer along with their theoretical calculation. Some materials like group IIIA metal oxides such as aluminium oxide (Al2O3), group IVB Metal Oxides and silicates such as titanium oxide (TiO2), zirconium oxide (ZrO2), zirconium silicate (ZrSiO4), Hafnium oxide (HfO2), hafnium silicate (HfSixOy) etc are replacement of silicon.

2. LITERATURE SURVEY

Saeed Mohsenifar, M.H. Sharokhabadi, "Gate stack high-K materials for Si-based MOsfets Past, Present, and future", Microelectronics and solid state Electronics 2015, DOI:10.5923/j.msse.20150401.03 [1]. In this paper authors have discussed the challenges and problems faced on scaling down the channel width of the MOSFET or ultimately scaling down the MOSFET size. As from the paper it's been clear that Silicon material fail in standard CMOS technology (for nanoscale), due to the short channel effect and tunneling effect shown by silicon material. The working of the MOSFET changes when we move towards the nanoscale regime. In order to continue scaling the planar MOSFET without harmful SCE's, the effective channel length needs to be 40times the dielectric thickness so the dielectric thickness must be decreased along with the physical dimension of the device.

S.Suthram, J.C Zeiegert, T.Nishida, "Piezeoresistance coefficient of (100)Silicon nMOSFET measured at low and high (1.5GPa)channel stress", IEEE electron devices letters, Vol.28, NO.1, January 2007[2]This paper gives a brief idea about the modeling of the highly stressed channel of the silicon MOSFET. In their experimental setup they have designed an unaxial channel stress; the wafer is allowed to

bend in a flexure based four point bending setup.The stress-altered drain current versus total unaxial longitudinal stress for long and short devices has been shown.

Y.L.Yang, Anthony G.O'Neill, Barry J.Gallacher, Sarah H.Olsen, "Using Piezeoresistance model with C-R conversion for modelling of strain-Induced mobility", IEEE electron device letters, vol.29. no.9, September 2008[3]. The piezeoresistance model have been commonly been used to describe mobility enhancement for low levels of process induced strain in CMOS technology. In this paper, a conversion between the change in conductivity and resistivity is developed such that a piezeoresistance model can be applied correctly to calculate the strain-induced mobility changes. They concluded that the linear piezeoresistance concept fails when the applied stress exceed the linear limit where nonlinear piezeoresistance effect occurs and showed that the correction to this i.e. the C-R conversion dramatically improves the accuracy over the commonly used formulation of piezeoresistance concept while maintaining its simplicity.

Jhong-Sheng Wang, William Po-Nien Chen, Chun-Hsing Shish,Chenhsin Lein,PinSu, "Mobility modeling and its extraction techniques for manufacturing starined-Si MOSFETs", IEEE electron letters, vol. 28, NO. 11 November 2007 [4]. In this letter, for a MOSFET channel thickness from 32nm to 73nm, a practical extraction method is integrated and proposed to decouple the parasitic parameters and to evaluate the mobility of short channel strained-Si devices. The extraction of parasitic source/drain resistance follows the improved Berkeley short channel IGFET model method to get an accurate drain current without parasitic drain resistance degradation for the current device. They concluded that, at a relatively high field, by assuming that a constant bulk piezeoresistance coefficient is applied for stress devices, their model can properly predict the mobility enhancement for the various strained-Si technologies and device dimensions by including the coulomb scattering corrections. A better description of tensile-stress mobility is achieved for nanoscale short channel devices.

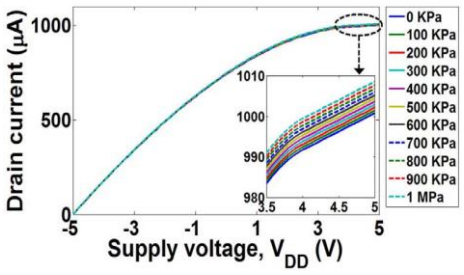


Figure 1 ID vs.VDD Characteristics of Active MOSFET for Various pressures [9].

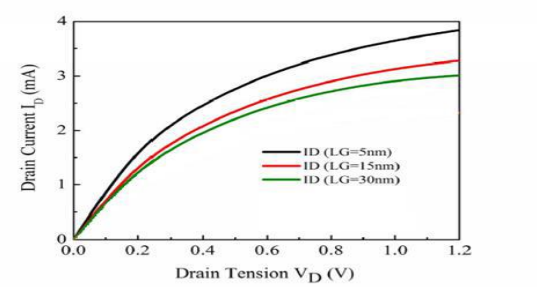


Figure2 ID vs.VDD Characteristics of Active MOSFET for Various Thickness of Oxide Layer [11].

3. METHODOLOGY

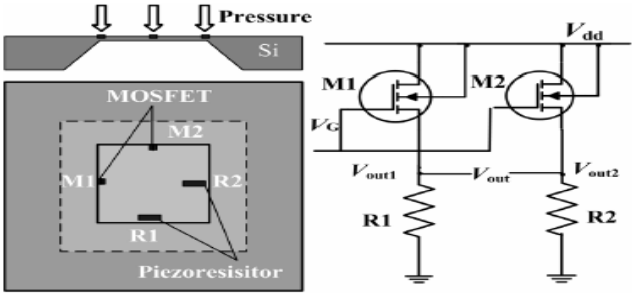
The question arises here is that how the thickness of channel will affect the sensitivity of MOSFET pressure sensor. There are many literatures in which it is reported that with the decrease in the channel width the drain current increases, which therefore increases the sensitivity of the device [9]. In this section we will discuss about the dependency of sensitivity of device with channel thickness and also the various literatures which reported about the same problem.

Various parameters used to design and simulate MOSFET embedded pressure sensor

a. Diaphragm shape, size and material-Square, 100μm x 100 μm x 5 μm, Silicon
b. using 5 μm CMOS technology for n-MOSFET piezoresistor
c. Dimension of n- MOSFET = 1.5 μm x 1.25 μm x1 μm
d. Drain current ID(sat) = 2 μA
e. Source to drain voltage= .5V
f. Output resistance = VSD/ ID(sat) = .25MΩ
g. Resistance of n-MOSFET equivalent piezoresitor= R= ro = 2MΩ
h. Resistivity of n-MOSFET piezoresistor=, ρ= 25 Ωm
i. Reference Temperature To = 300 K

Operating principle of the MOSFET pressure sensor is presented by zhao hua zhang et al [5]. Based on the stress sensitive effect of MOSFET, a new MOSFET-bridge-circuit structure is designed, as shown in Figure 1. Two PMOSFET's and two piezoresistors are connected to form a Wheatstone bridge. To obtain the

maximum sensitivity, these components are placed near the four sides of the silicon diaphragm, which are the high stress regions. The MOSFET's has the same structure parameter W/L, same threshold voltage VT and gate-source voltage VGS (equal to VG-Vdd). They are designed to work in the saturation region. The piezoresistors also have the same resistance R0.



(a) (b)

Figure 1. (a) Schematic of Novel MOSFET Pressure Sensor Including Two MOSFET and Two Resistors on the Membrane to Form a Wheatstone Bridge, (b) The MOSFET-Based Bridge Circuit, the Output Voltage is Vout=Vout1-Vout2, the Voltage Source is VDD

When there is no forced pressure, the bridge is in balance. The balanced output V0 of each arm is calculated by [6]

$$V0 = .5\ R0\ \mu P0\ COX\ (W/L)\ (VGS - VT) \quad (1)$$

As a result, the sensor output signal Vout is zero. When a pressure is forced on the membrane, the current and piezo-resistance in each bridge arm are changed. The variation of the PMOSFET current is proportional to the change of channel mobility Δμp, computed as [6]:

$$\Delta IDS / IDS = \Delta\mu / \mu o = \pi l .\sigma l + \pi t .\sigma t \quad (2)$$

Where, σ1 and σ2 are the parallel and vertical stress in the channel; π1 and π2 are the parallel and vertical channel piezoresistive coefficient, respectively. The change of piezoresistance is also proportional to the resistor mobility change ΔμR, which can be expressed using a similar formula, as:

$$\Delta R/ RO = \Delta \mu R / \mu RO = \pi l .\sigma l + \pi t .\sigma t \quad (3)$$

Where, σ1 and σ2 are the parallel and vertical stress in the resistor bar, π1 and π2 are the parallel and vertical piezoresistive coefficient, respectively.

According to the different current direction placing, the bridge becomes unbalance. The μP of M1 and the μR of R2 get increased with the stress, in opposition, the μP of M2 and the μR of R1 are decreased. Then the two arms outputs become as [6]:

$$Vout\ 1,2 = (1/2)\ (Ro + \Delta R).\ (\mu po + \Delta\mu p)\ COX\ (W/L)\ (VGS - VT)2 \quad (4)$$

Therefore, the sensor output is obtained as [6]:

$$Vout = 2\ (\Delta\mu p / \mu po + \Delta\mu R/ \mu RO\ )2\ Vo \quad (5)$$

Formula (5) shows that, Vout is proportional to the stress as well as the forced pressure. This is the operating principle of the novel MOSFET-bridge-circuit pressure micro sensor.

Several literatures has been reported the sensitivity of this pressure sensor to be increasing upto 100 micrometer of channel thickness concluded that the sensitivity of the MOSFET sensor will also increase with reduction in channel thickness with the increase in drain current [4], [5].

There are also some literatures has reported that the drain current of MOSFET increases with reduction in thickness of channel [9]. With above formulas and the literature mentioned above we can conclude that the sensitivity of the MOSFET pressure sensor should increase if we go below 130 nm thickness of channel. In this paper we will present the comparison of sensitivity of MOSFET pressure sensor having thickness from 130 nm to 20 nm.

4. RESULT AND DISCUSSION

After simulating MOSFET for various thicknesses and applying a force of 2 bar we have obtained the I-V curve i.e. the drain current and drain voltage curve (Figure 1) and plotted the thickness versus resistance curve.

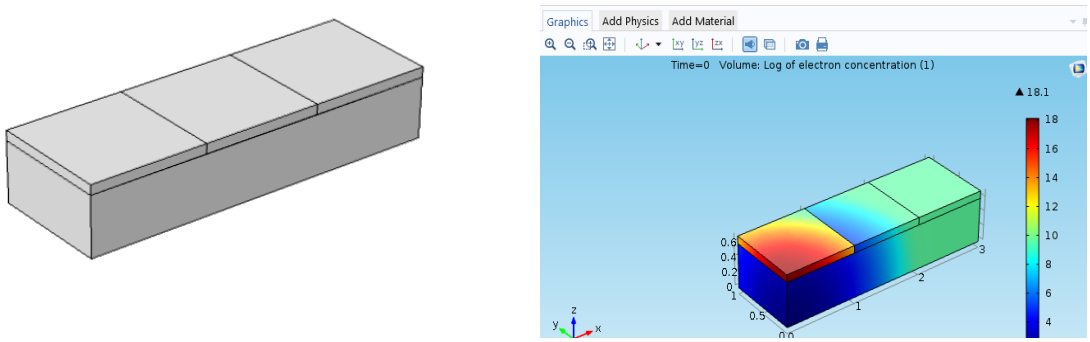


Figure 2. 3-D Model & Plot of Electron Concentration in the Model at Time=0 of p-channel MOSFET with Silicon Material

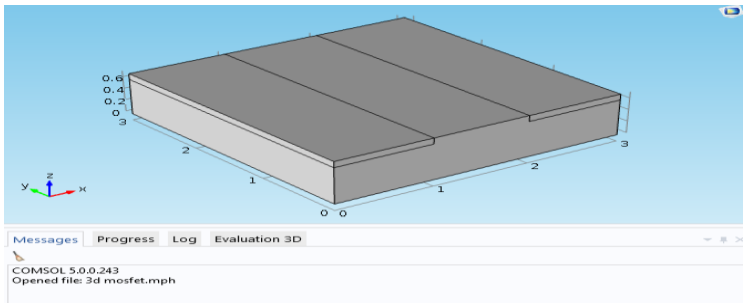


Figure 3. 3-Dimensional p Channel MOSFET of 3x3x.7 nm, Doped n-Region of Area1x3nm Each Side with a p-channel Width of 1nm

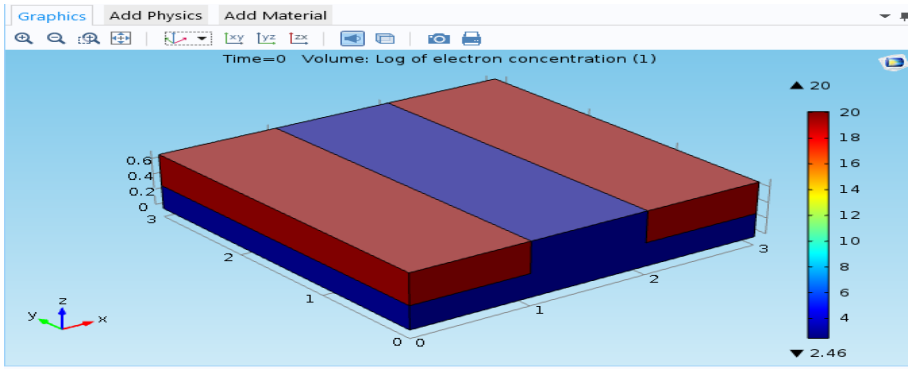


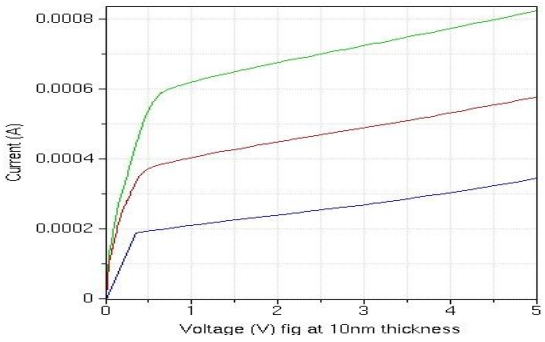
Figure 4. Electron Density of Model 3

The theoretical calculation for increasing the sensitivity of the sensor we can relate the sensitivity of the sensor to the resistance, lower the resistance in the channel greater the mobility of the carrier and hence the sensitivity increases as the variation in the current will be sensible. Thus the equation below defines the resistance of the channel

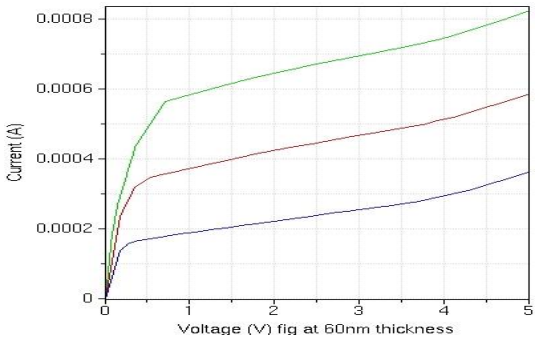
$$R = (VDD - VGS) / IG \quad (6)$$

Where, VDD is drain voltage, VGS is gate to source voltage, IG is gate current.

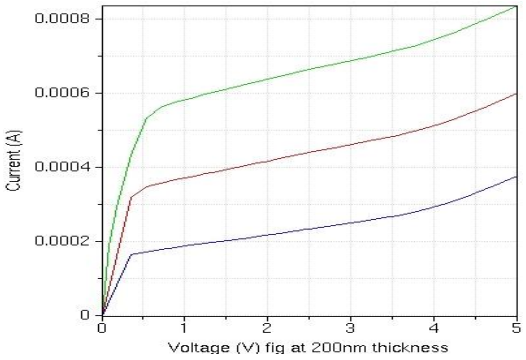
After simulating MOSFET in 2 Dimensional structure for various thicknesses obtained the I-V curve i.e the drain current and drain voltage curve (Figure.20) and plotted the thickness versus resistance curve (Figure 3).



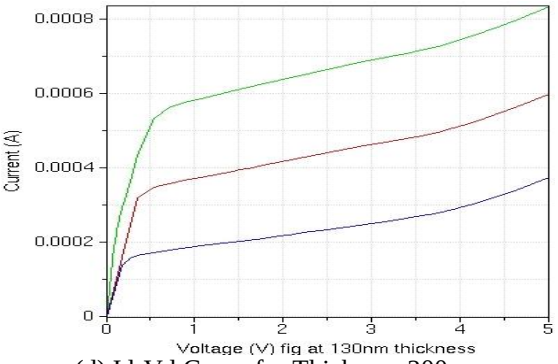
(a)Id-Vd Curve for Channel Thickness10nm



(b)Id-Vd Curve for Channel Thickness of 60nm



(c) Id-Vd Curve for Thickness 130nm



(d) Id-Vd Curve for Thickness 200nm

Figure 3. The Id-Vd Curve for Different Channel Thicknesses with vg Constant at .5, .75 and 1 volt for Oxide Thickness of 10nm, 60nm, 160nm and 200nm

Thus from figure it's been visible that when we move from 200nm towards 10nm the resistance initially increases till 130nm but below it the resistivity decreases hence the sensitivity increases for the channel thickness of MOSFET below 130nm to 10nm for the conventional silicon material.

5. COMPARATIVE ANALYSIS

Curve below 2nm has been plotted for the three different materials that is for Zirconium Oxide (Zr_2O_3), Lanthanum Oxide (La_2O_3) and Hafnium Oxide (HfO_2). In order to compare these materials in this section a comparative I-V curves has been drawn below 2nm for analysis of the best material among the respective three.

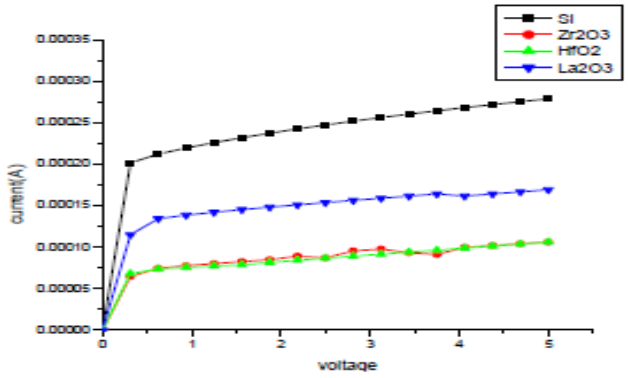


Figure 5. Id -Vd Curve at 2nm for Different Material

Different materials I-V characteristics curves have been compared for silicon, Hafnium Oxide, Lanthanum Oxide and Zirconium Oxide at 2nm channel thickness of MOSFET structure. From the Figure. 5 it can be observed that, Lanthanum Oxide materials performance or current is high as compared to the other High dielectric constant materials. The lanthanum oxide material draws greater current among other materials.

Table 1. Id -Vd Curve at 2nm for Different Material

voltage	Current (mA)			
	Silicon	Zirconium Oxide	Hafnium Oxide	Lanthanum Oxide
0	-2.17892	-8.023	-8.02311	-1.2426
0.3125	0.20	0.648	0.0685547	0.115
0.625	0.21	0.7885	0.0738	0.1345
0.9375	0.219	0.0778	0.075	0.1388
1.25	0.226	0.0806	0.07749	0.1423
1.5625	0.232	0.8285	0.07902	0.145
1.875	0.2377	0.8509	0.08183	0.1484
2.1875	0.243	0.8944	0.08445	0.1512
2.5	0.247	0.08729	0.08697	0.1540
2.8125	0.252	0.0958	0.089	0.156
3.125	0.256	0.0979	0.0918	0.159
3.4375	0.261	0.0936	0.0942	0.1618
3.75	0.264	0.0915	0.0967	0.1644
4.0625	0.268	0.1000	0.0991	0.1618
4.375	0.272	0.1022	0.1015	0.1644
4.6875	0.275	0.1043	0.1040	0.1675
5	0.279	0.1065	0.1065	0.1695

It can be observed that a small amount of Current is drawn from the circuit about few milli Amperes

6. CONCLUSION

Thus, after studying all the views from the various authors the MOSFET based pressure sensors sensor have been studied for its optimised performance and enhancing the sensitivity of the sensors while decreasing the size of them. The materials with higher k value can be used to overcome all the challenges in scaling down the MOSFET. These MOSFET based sensors which are smaller enough can be used in various applications in the field of medical science and technology according to the need and availability.

The sensitivity of the MOSFET pressure sensor is found to be increasing as the thickness of channel is reducing, this result occurs due to high drain current at lower thickness. Further it is reported in some literature that further reduction in the thickness of channel will allow the free flow of electron through the MOSFET. So it is suggested to use the material having high dielectric constant such as HfO2, if more size miniaturisation is required.

REFERENCES:

[1] W Gajendra Shekhawat Et Al, Soo-Hyun Tark, Vinayak P. Dravid, "MOSFET-Embedded Microcantilevers For Measuring Deflectionin Biomolecular Sensors", *Science 311*, 1592(2006) DOI:10.1126/Science.1122588.

[2] S.Suthram, J.C Zeiegert, T.Nishida, "Piezoresistance Coefficient Of (100)Silicon Nmosfet Measured At Low And High (1.5gpa) Channel Stress", *IEEE Electron Devices Letters*, VOL.28,NO.1, January 2007

[3] Y.L.Yang, Anthony G.O'Neill, Barry J.Gallacher, Sarah H.Olsen, "Using Piezeoresistance Model With C-R Conversion For Modelling Of Strain-Induced Mobility", *IEEE Electron Device Letters*, Vol.29. No.9, September 2008

[4] Jhong-Sheng Wang, William Po-Nien Chen, Chun-Hsing Shish, Chenhsin Lein, Pinsu, "Mobility Modelling and Its Extraction Techniques for Manufacturing Strained-Si Mosfets", *IEEE Electron Letters*, Vol.28, NO. 11 November 2007

[5] Zhao-Hua Zhang, Yan-Hong Zhang, Li-Tian Liu, Tian-Ling Ren, "A Novel MEMS Pressure Sensor with MOSFER on Chip", *IEEE Sensors Conference*, 2008.

[6] Zhang Zhao-Hua, Ren Tian-Ling, Zhang Yan-Hong, Han Rui-Rui, Liu Li-Tian, "Low Power and High Sensitivity MOSFET-Based Pressure Sensor", *chin. Phys. Lett.* Vol. 29, No. 8 (2012) 088501

[7] Xiaofeng Zhao, Dianzhong Wen, Gang Li, "Fabrication and Characterisation Of An Nc-Si/C-Si Heterojunction Mosfets Pressure Sensor", *Sensors 2012*, ISSN1424-8220, DOI: 10.3390/S120506369.

[8] Pradeep Kumar Rathore , Brishbhan Singh Panwar, *"CMOS-MEMS Integrated MOSFET Embedded Bridge Structure Based Pressure Sensor"*, Annual IEEE India Conference (INDICON) , 2013

[9] Pradeep Kumar Rathor, Brishbhan Singh Panwar, *"Design And Optimization Of A CMOS_MEMS Integrated Current Mirror Sensing Based MOSFET Embedded Pressure Sensor"*, IEEE International Conference On Control Application(CCA), August 28, 2013

[10] K N Bhat, Ajay AP, Navakanta Bhat, SM Kulkarni, "Novel MOSFET Based Pressure Sensors That Uses Combined Channel Piezoresistance And Gate Capacitance Effects", *Stm Journel, Recent Trend In Sensor Research & Technology*, ISSN: 2395-8765, Volume 2, Issue 2.

[11] Harsh Vardhan, *"Effect Of Gate Length And Oxide Thickness On DG MOSFET",* International Conference Of Engineering And Technology, Volume:2, Issue :8 L 2015, E-ISSN: 2395-0056

[12] Saeed Mohsenifar, M.H. Sharokhabadi, "Gate Stack High-K Materials For Si-Based Mosfets Past,Present, And Future",*Microelectronics An Solidstate Electronics* 2015, DOI:10.5923/J.Msse.20150401.03

[13] Olivier Sagazan, Emmanuel Jacques, Tayeb Mohammed-Brahim, "MOSFET on Thin Si Diaphragm As Pressure Sensor", *ECS Transaction*, 2011.

[14] M.F. Bolanos, N. Abele, V. Pott, D. Bouvet, G.A. Racine, J.M. Quero, And A.M. Lonescu, "Polyimide Sacrificial Layer For Sol SG-MOSFET Pressure Sensor", *Microelectronic Engineering*, Vol. 83, Pp. 1 1 85-1 188, 2006.

[15] Ananthasuresh GK, Vinoy KJ, Gopalakrishnan S. Et Al., "Micro and Smart Systems Technology and Modeling", Wiley NY, 2012.