Indonesian Journal of Electrical Engineering and Computer Science
Vol. 9, No. 3, March 2018, pp. 711~721
ISSN: 2502-4752, DOI: 10.11591/ijeecs.v9.i3.pp711-721

A Simplified PWM Technique for Reduced Switch Count Multilevel Inverter

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Article Info

Article history:

Received Sep 19, 2017
Revised Dec 30, 2017
Accepted Jan 17, 2018

Keywords:

Multilevel Inverter
Pulse Width Modulation
Renewable Energy Sources
Total Harmonic Distortion

ABSTRACT

Penetration of multilevel inverters (MLI) in to high power and medium voltage application has been increasing because of its advantages. A conventional two level inverter has high harmonic distortion which gives poor power quality. Lot of topologies has been developed to overcome the drawbacks of two level inverter. These topologies include more number of switching devices which increases the design complexity and cost. The optimum design of inverter requires less number of switches with better quality in waveform. In this paper, a symmetrical five level and seven level inverter configuration with simplified pulse width modulation technique is proposed. This proposed inverter requires less switches, less protection circuits along with low cost and size. The analysis of the inverter circuits is done by using Matlab/Simulink software. The synthesized staircase wave form is shown and total harmonic distortion (THD) is also measured.

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1. INTRODUCTION

In recent years, the industries have started to operate at higher power rating machines. And for some medium voltage drives and applications, they need medium voltage and high power level. For this purpose, multilevel inverter [1]-[3] concept has been developed for high power and medium voltage applications. These inverters are not only used for high power applications, but also used for interfacing the renewable energy sources (RES) [4]-[6] to the utility grid. The renewable energy sources like solar, wind and fuel cell could be easily connected to the grid using multilevel inverters. The multilevel inverter concept has been introduced since 1975. It has started with a three level inverter and consequently lot of inverter topologies has been introduced.

However, the major objective of the multilevel inverter is to get high power using power semiconductor switches with number of low voltage dc sources. The characteristics of less total harmonic distortion (THD) [7-8], reduced dv/dt and low common mode voltage are the reasons for getting popularity for the multi-level inverters in medium voltage and high power applications. The advantages of multilevel inverter are given below.

a. Reduces the electromagnetic compatibility problems because of low dv/dt stress and less harmonic distortion.
b. The common mode voltage of a multilevel inverter is small. Therefore, if a multilevel inverter is connected to drive the stresson the bearing will be reduced.
c. The current drawn by the multilevel inverter has low distortion.
d. Multilevel inverters can able to operate at fundamental as well as high switching frequency.

However, more number of switching devices in the inverter causes to decrease the efficiency and reliability of the drive [9]-[10]. Therefore, it is necessary to improve the reliability and efficiency by reducing

the number of switches. In this paper, a reduced switch count multilevel inverter for five and seven level is proposed. A simplified pulse width modulation technique is implemented for control strategy [11]. A five level inverter is proposed with five switches and a 7 level inverter is proposed with six switches. These circuits are implemented using Matlab/Simulink software. The total harmonic distortion for voltage wave form is measured by fast Fourier transform analysis.

2. FIVE SWITCH FIVE LEVEL INVERTER

The proposed 5 switch five level multilevel inverter is shown in figure 1. This topology consists of four switches of IGBT and one ideal switch. The source voltage is divided in to two equal parts as V_{dc}/2each. The configuration of the circuit with R load is shown.

The required five level output voltage levels 0, V_{dc}/2, V_{dc}, -$V_{dc/2}$ and –V_{dc} are obtained by operating these five switches in proportional manner. The diagrams for each level are illustrated in following figures.

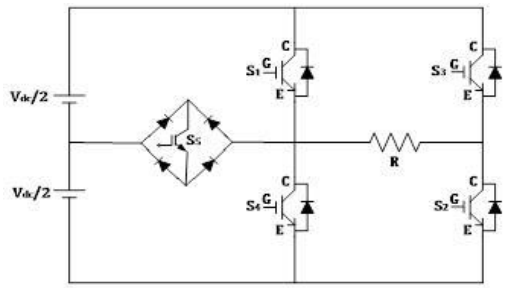

Figure 1. Proposed five level inverter

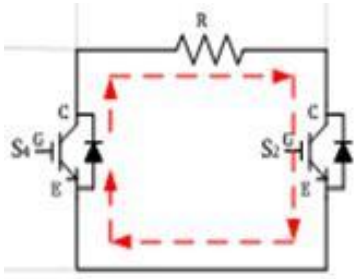

Figure 2. Operational diagram for 0 voltage level

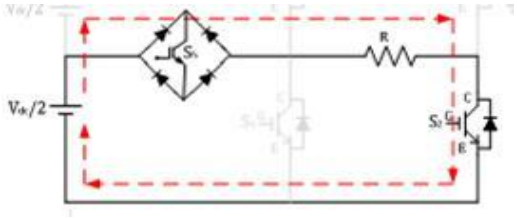

Figure 3. Operational diagram for V_{dc}/2 voltage level

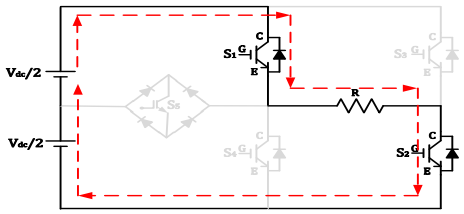

Figure 4. Operational diagram for V_{dc} voltage level

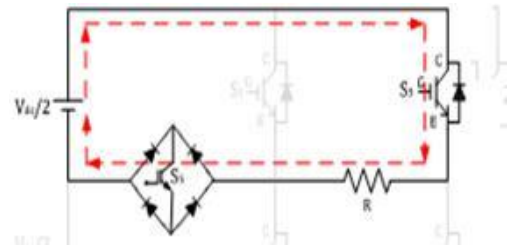

Figure 5. Operational diagram for -$V_{dc/2}$ voltage level

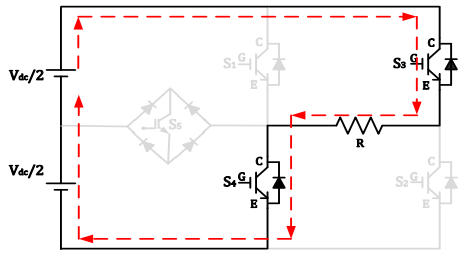

Figure 6. Operational diagram for -Vdc voltage level

Level - 0

To get zero voltage level, the switches S2 and S4 should be turned on. The load becomes short circuit and the voltage across it is zero. The operational diagram is shown in Figure 2.

Level - $V_{dc/2}$

The voltage level of Vdc/2 is produced by switching ON the switches S2 and S5.In this case only bottom source is connected to the load and the voltage $V_{dc/2}$ appears across the load. The operational diagram is shown in figure 3.

Level – V_{dc}

By switching ON switches S1 and S2 we can get the voltage level of V_{dc}. In this case both the voltage sources appear across the load. The operational diagram is shown in Figure 4.

Level - $-V_{dc/2}$

The $-V_{dc/2}$ voltage level is obtained by closing the switches S3 and S5. In this case the upper voltage source is connected to the load. The operational diagram is shown in Figure 5.

Level – $-V_{dc}$

The voltage level $-V_{dc}$ could be obtained by operating the switches S3 and s4. Both the voltage sources are connected to load with negative polarity. The operational diagram is shown in Figure 6.

Table 1. Switching Sequence for Five Level Five Switch Multilevel Inverter

Voltage levels	Switching Sequence				
	S_1	S_2	S_3	S_4	S_5
0	OFF	ON	OFF	ON	OFF
$V_{dc/2}$	OFF	ON	OFF	OFF	ON
V_{dc}	ON	ON	OFF	OFF	OFF
$-V_{dc/2}$	OFF	OFF	ON	OFF	ON
$-V_{dc}$	OFF	OFF	ON	ON	OFF

The Table 1 shows the switching pattern for five switch five level inverter.

3. SIX SWITCH SEVEN LEVEL INVERTER

The proposed 6 switch seven level multilevel inverter is shown in Figure 7. This topology consists of four switches of IGBT and two ideal switches. The source voltage is divided in to three equal parts as Vdc/3each. The configuration of the circuit with R load is shown.

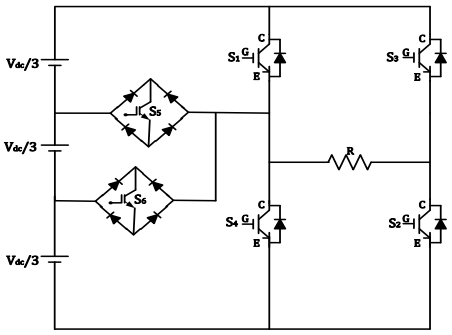

Figure 7. Proposed seven level inverter

The required seven level output voltage levels 0, $V_{dc/3}$, $2V_{dc/3}$, V_{dc}, $-V_{dc/3}$, $-2V_{dc/3}$ and $-V_{dc}$ are obtained by operating these six switches in proportional manner. The diagrams for each level are illustrated in following figures.

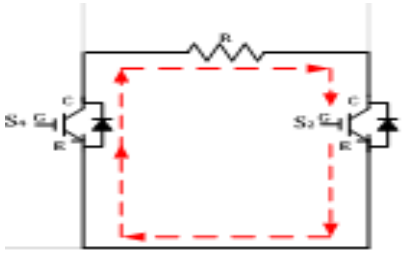

Figure 8. Operational diagram for level zero

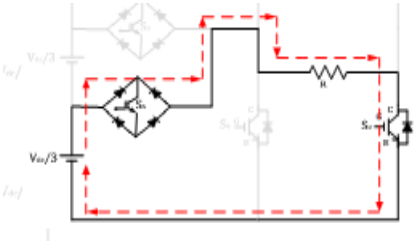

Figure 9. Operational diagram for level $V_{dc/3}$

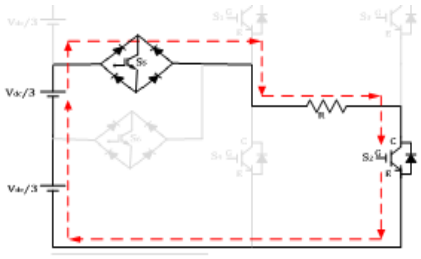

Figure 10. Operational diagram for level $2V_{dc/3}$

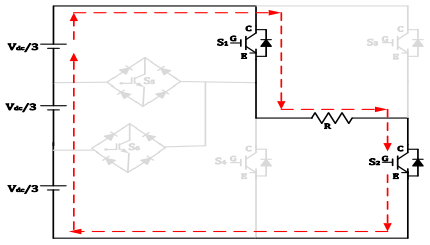

Figure 11 Operational diagram for level V_{dc}

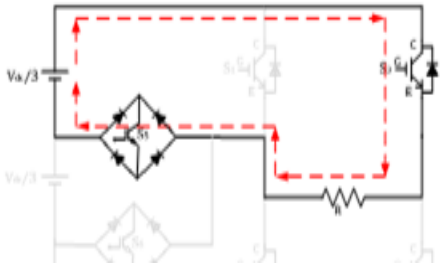

Figure 12 Operational diagram for level $–V_{dc/3}$

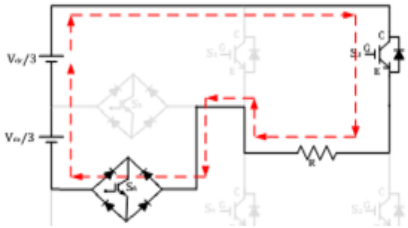

Figure 13 Operational diagram for level $–2V_{dc/3}$

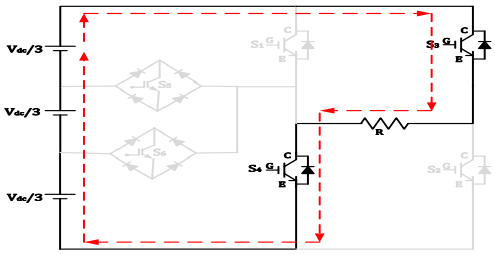

Figure 14. Operational diagram for level $–V_{dc}$

Level - 0

To get zero voltage level, the switches S2 and S4 should be turned on. The load becomes short circuit and the voltage across it is zero. The operational diagram is shown in Figure 8.

Level - $V_{dc/3}$

The voltage level of Vdc/3 is produced by switching ON the switches S2 and S6.In this case only bottom source is connected to the load and the voltage $V_{dc/3}$ appears across the load. The operational diagram is shown in Figure 9.

Level - $2V_{dc/3}$

The voltage level of 2Vdc/3 is produced by switching ON the switches S2 and S5.In this case bottom two sources are connected to the load and the voltage $2V_{dc/3}$ appears across the load. The operational diagram is shown in Figure 10.

Level – V_{dc}

By switching ON switches S1 and S2 we can get the voltage level of V_{dc}. In this case all the voltage sources appear across the load. The operational diagram is shown in Figure 11.

Level - $-V_{dc/3}$

The voltage level of $-V_{dc/3}$ is produced by switching ON the switches S3 and S5.In this case only upper source is connected to the load and the voltage $-V_{dc/3}$ appears across the load. The operational diagram is shown in Figure 12.

Level - $-2V_{dc/3}$

The voltage level of $2V_{dc/3}$ is produced by switching ON the switches S3 and S6.In this case top two sources are connected to the load and the voltage $-2V_{dc/3}$ appears across the load. The operational diagram is shown in Figure 13.

Level – $-V_{dc}$

By switching ON switches S3 and S4 we can get the voltage level of $-V_{dc}$. In this case all the voltage sources appear across the load. The operational diagram is shown in Figure 14.

4. SIMPLIFIED PWM TECHNIQUE

4.1. For Five Switch Five Level

In multilevel inverters the output voltage is controlled by using different modulation strategies. In PWM control, there are three techniques like fundamental switching frequency PWM, PWM technique based on carrier and space vector PWM technique. Among these, the carrier based PWM technique is frequently used because; it has less complexity even when output voltage levels are more. In this paper, a multi-carrier based SPWM (sinusoidal pulse width modulation) technique has been implemented. It contains a reference signal which is compared with the two high frequency carrier signals to generate switching states A, B and C (Figure 15). The two carriers have a small difference in its magnitude which are disposed vertically. By combining these switching states, the gating pulses are generated for the switches using following logical notation.

$$S_1 = A \cdot C$$
$$S_2 = C + \bar{B}\bar{C}$$
$$S_3 = B \cdot \bar{C}$$
$$S_4 = \bar{B}C + \bar{B}\bar{C} + A\bar{C}$$
$$S_5 = B\bar{C}$$

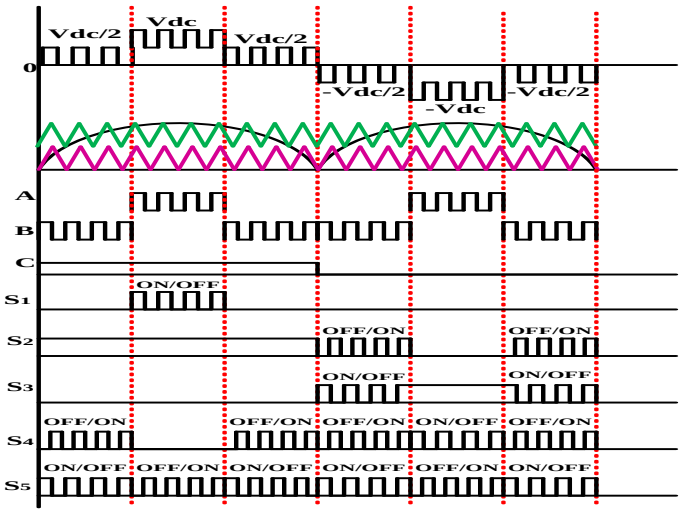

Figure 15. PWM technique for five level

4.2. For Six Switch Seven Level

In this control three carrier waveforms are used to generate the four switching states. The logical combination of four switching states A, B, C and D gives us the pulses for switches S1 through S6. The PWM technique and switching logic is given.

By combining these switching states, the gating pulses are generated for the switches using following logical notation.

$$S_1 = C \cdot D$$
$$S_2 = D + \bar{A}\bar{D}$$
$$S_3 = A \cdot \bar{D}$$
$$S_4 = \bar{A}D + \bar{A}\bar{D} + C\bar{D}$$
$$S_5 = B\bar{C}D + A\bar{B}\bar{D}$$
$$S_6 = A\bar{B}D + B\bar{C}\bar{D}$$

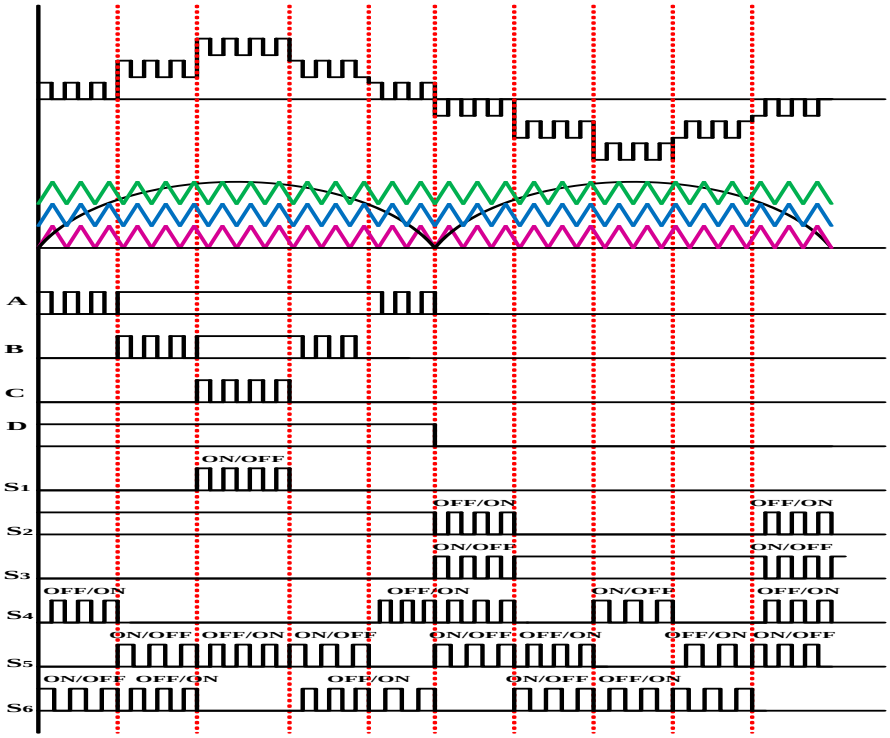

Figure 16. PWM technique for seven level

5. SIMULATION RESULTS

5.1. Five switch Five level inverter

Case 1: R-load

Figure 17. Shows the output voltage of the five switch five level inverter.

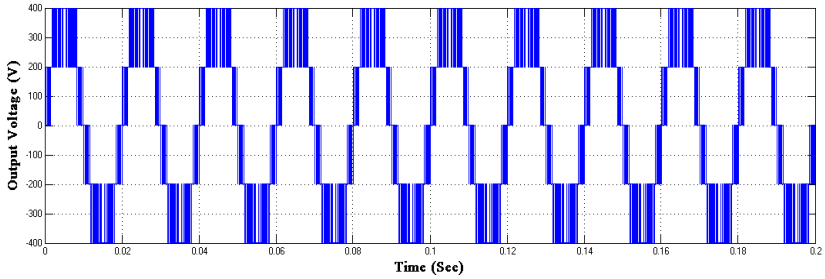

Figure 17. Output voltage

The output current wave form is shown in Figure 18

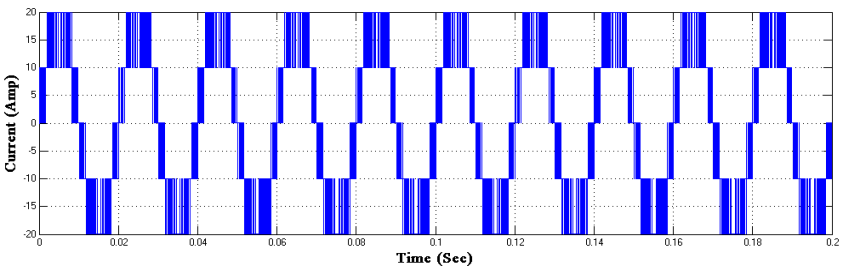

Figure 18. Output current

The PWM waveforms and switching pulses are shown in Figure 19 and 20 respectively.

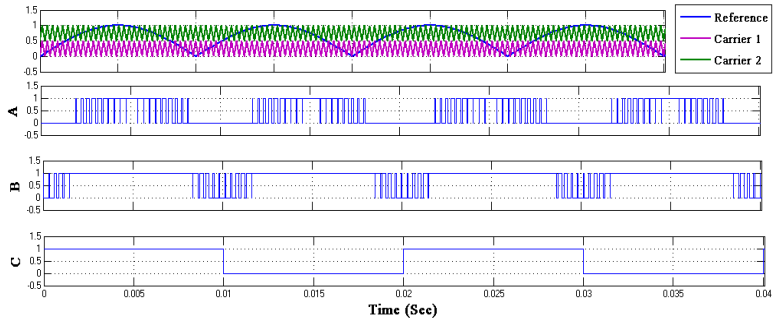

Figure 19. PWM wave forms

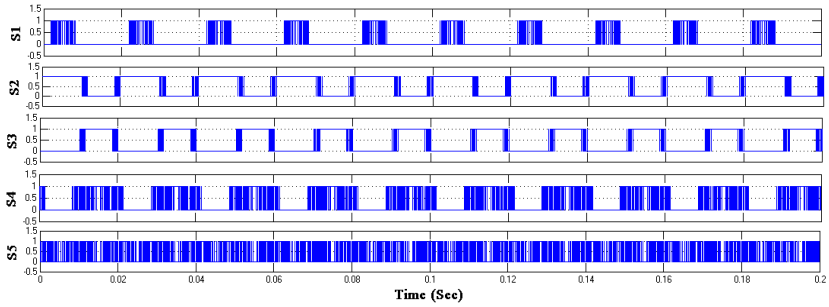

Figure 20. Switching pulses

Case 2: RL-Load

The output voltage waveform is shown in Figure 21.

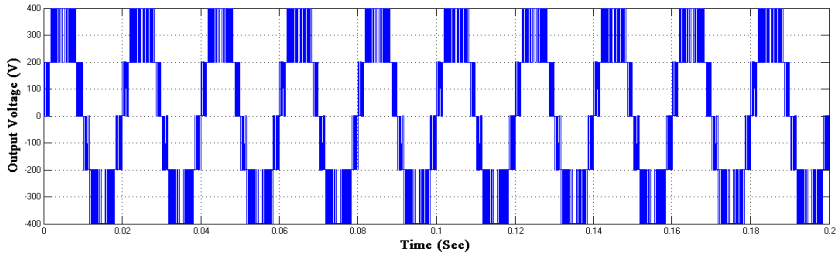

Figure 21. Output voltage

Figure 22 shows the output current wave form.

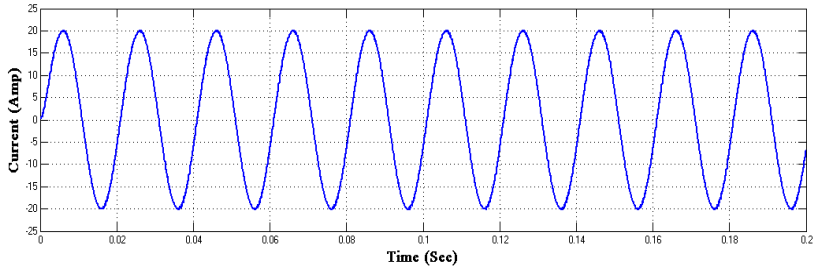

Figure 22. Output current

PWM wave forms and switching pulses are shown in Figure 23 and 24 respectively.

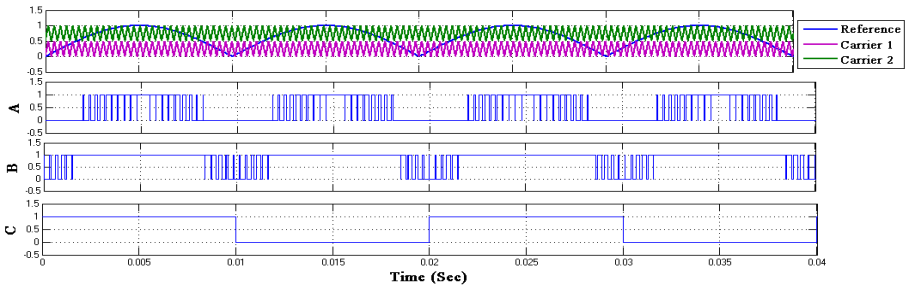

Figure 23. PWM wave forms

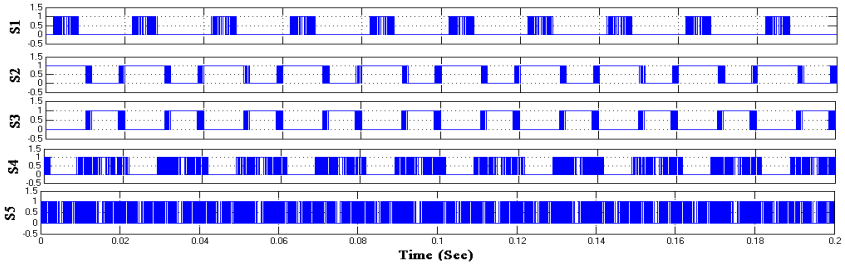

Figure 24. switching pulses

The total harmonic distortion for voltage wave form is given in figure 25 and the THD measured is 26.87%.

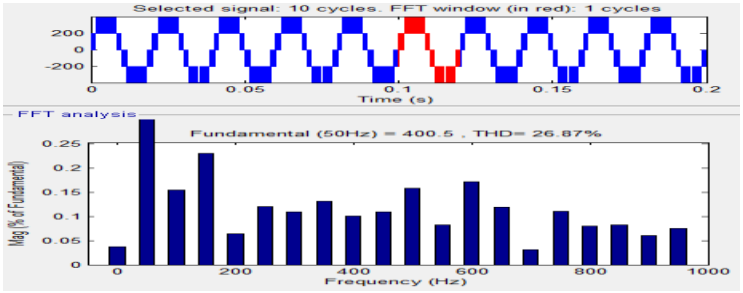

Figure 25. THD Graph

5.2. Six Switch Seven Level Inverter

Case 1: R-load

The output voltage of six switch seven level is shown in Figure 26.

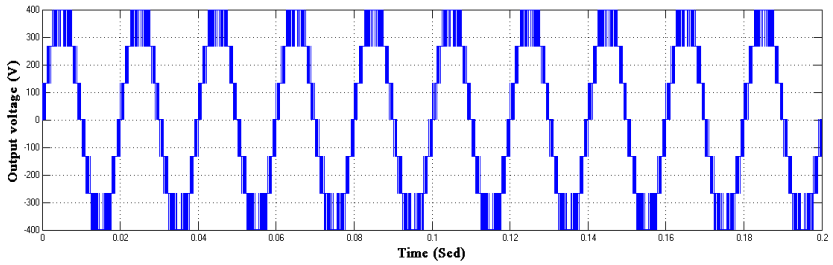

Figure 26. Output voltage

Figure 27 shows the output current.

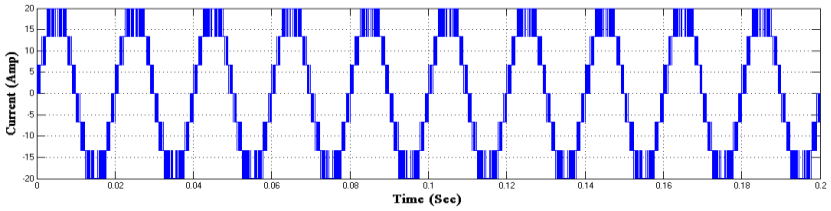

Figure 27. Output current

The PWM waveforms and switching pulses are shown in Figure 28 and 29 respectively.

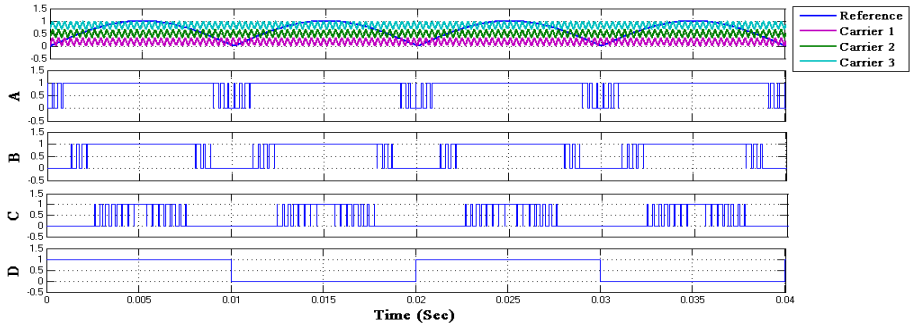

Figure 28 PWM waveform

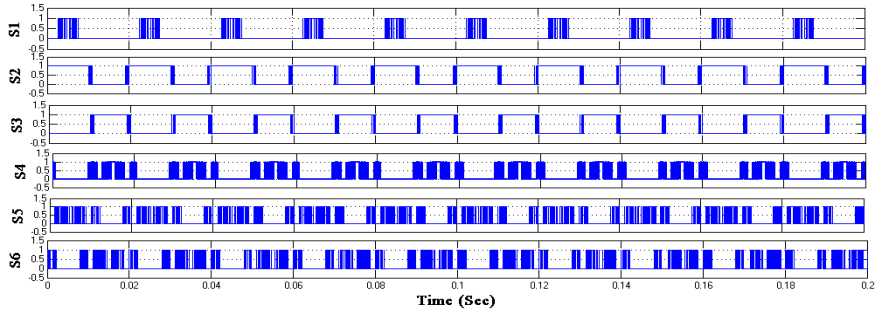

Figure 29. Switching pulses

Case 2: RL-load

Figure 30 shows the output voltage wave form.

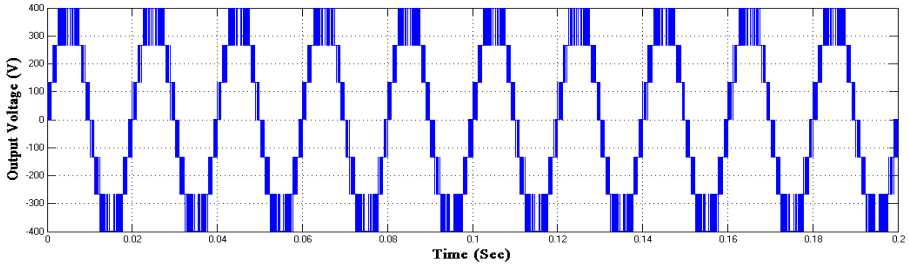

Figure 30. Output voltage

Output current waveform is shown in Figure 31.

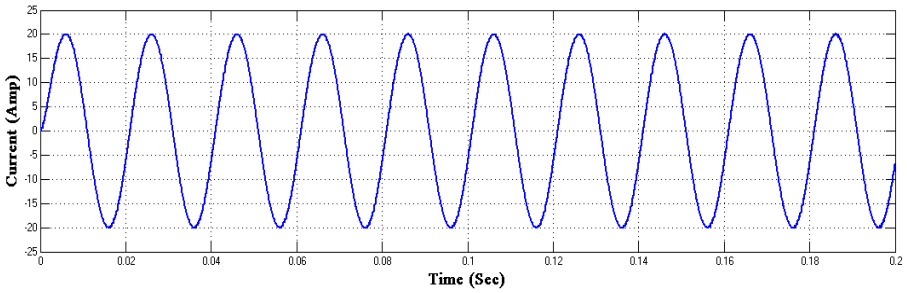

Figure 31. Output current

Figure 32 and 33 shows the PWM waveform and switching pulses respectively.

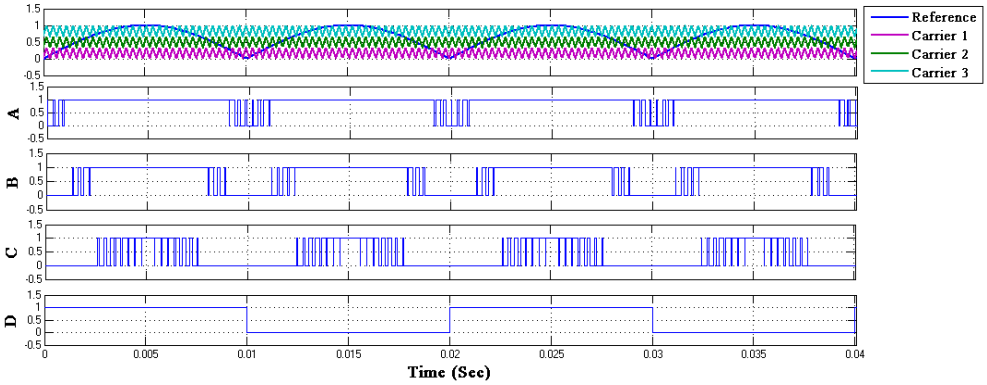

Figure 32. PWM wave form

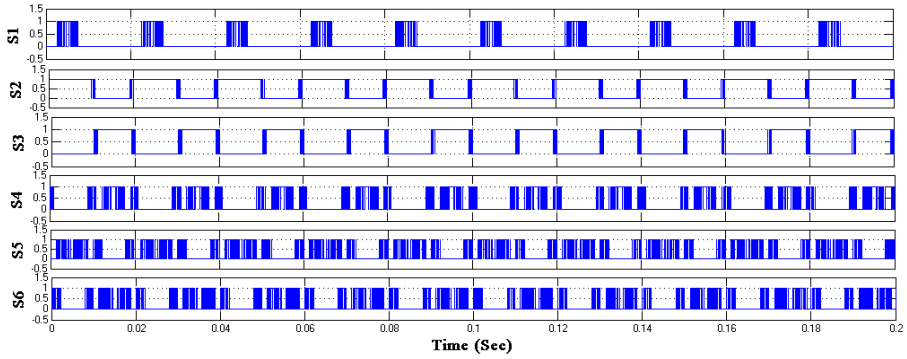

Figure 33. Switching pulses

The total harmonic distortion is shown in Figure 34 and measured 18.18%.

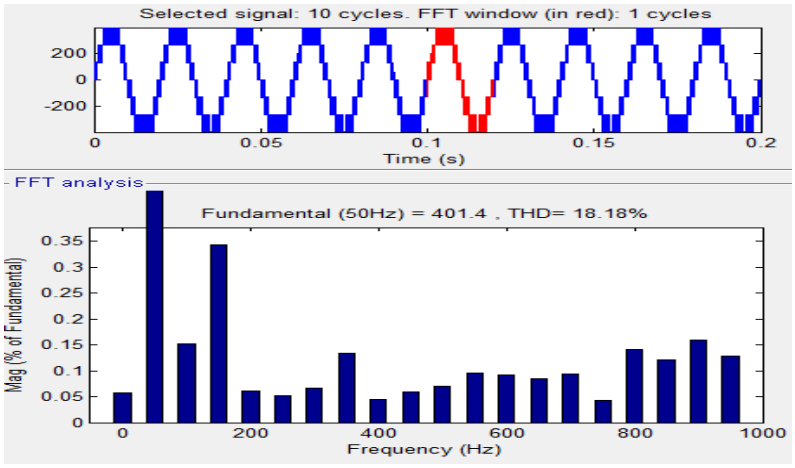

Figure 34. THD

6. CONCLUSION

In this paper, the five switch five level and a six switch seven level multilevel inverter is proposed. A simplified pulse width modulation technique also has been implemented for proposed inverters. Based on the PWM wave forms a digital switching logic has been developed and implemented to the control logic. The five level and seven level inverters are analyzed with R and RL load and the results are presented. The total harmonic distortion is also measure for both the levels. The THD for five level is 26.87% and for seven level is 18.18%.

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