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Comparative Analysis of Carrier Based Techniques for Single phase Diode Clamped MLI and Hybrid Inverter with Reduced Components

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Abstract

The multilevel inverters have highly desirable characteristics in high power high voltage applications. The multilevel inverter was started first with diode clamped multilevel inverter. Later, various configurations have been came into existence for many applications. However the multilevel inverters have some demerits such as requiring higher number of components, PWM control method is complex and capacitor voltage balancing problem. The hybrid multilevel inverter presented in this paper has superior characteristics over conventional multilevel inverters. The hybrid multilevel inverter employs fewer components and less carrier signals when compared to conventional multilevel inverters. It consists of level generation and polarity generation stages which involves high frequency and low frequency switches. The complexity and overall cost for higher output voltage levels are greatly reduced. Implementation of single phase 7-level, 9-level and 11-level diode clamped multilevel inverter and hybrid multilevel inverter has been performed using sinusoidal pulse width modulation (SPWM) strategies i.e., phase disposition (PD), alternate phase opposition disposition (APOD). Also these techniques are compared in terms of total harmonic distortion (THD) for various modulation indices and observed to be greatly improved in case of hybrid inverter when compared to diode clamped inverter. The comparative study of performance for single phase diode clamped multilevel inverter and hybrid inverter is analyzed with different loads. Simulation is performed using MATLAB/ SIMULINK.

Keywords: Diode clamped multilevel inverter, Alternate phase opposition disposition, Hybrid inverter, Phase disposition, Total harmonic distortion

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1. Introduction

The concept of power conversion in multilevel inverters (MLI) is to synthesize a staircase voltage waveform from several lower voltage DC sources which approaches the sinusoidal wave with reduced harmonic distortion has got several advantages and have drawn tremendous interest in high power high voltage applications [1-4]. In case of multilevel inverters the semiconductors are wired to form series type connection so that the operation at higher voltages is possible. The switching losses and the switching frequency can be reduced by staggering the switching because the switches are not truly series connected. Conventional multilevel inverters include neutral point clamped (diode-clamped) inverter, flying capacitor (capacitor clamped) inverter and cascaded H-bridge inverter. The major drawback of multilevel inverters is the higher number of power semiconductor switches needed that complicates the overall system [5-8]. Using lower rated switches in the multilevel inverter can reduce the cost of active semiconductors compared to two level inverters. Associated gate drive circuits are required for each active semiconductor which increases the complexity. In [9], the symmetrical topology which is called as reversing voltage topology is implemented for single phase seven level inverter. This multilevel inverter topology requires less number of components when compared to conventional multilevel inverters. A multilevel inverter with reversing voltage component has many advantages as the levels increase when compared to conventional multilevel inverters. The hybrid topology eliminates the diodes and capacitors that are used in diode clamped inverters, capacitors used in flying capacitor inverters and also reduces the switches and carrier signals required than in cascaded inverters, diode clamped, and flying

capacitors inverters. An approach of utilizing high-power devices with low-switching-frequency reduces voltage distortion of output but has got current harmonics which is a major drawback [10-13]. There are asymmetrical methods of using different values of voltage source which requires more number of power switches and diodes with different rating. Some topologies suffer from the capacitor balancing problems. Whereas in case of hybrid multilevel inverter, the voltage sources used have equal values and has many advantages compared with the methods discussed above. It uses less number of switches and carrier waves and also operates the switching devices at line frequency which results in more efficiency. Various carrier-based PWM techniques are reported to minimize total harmonic distortion(THD). Advanced multilevel inverter topologies have been proposed recently such as hybrid multilevel inverter, soft switching inverter and generalized multilevel inverter. The multilevel inverters have been extensively used in applications like FACTS, tractions and industrial drives [14-16]. In this paper, phase disposition (PD), alternate phase opposition disposition (APOD) sinusoidal pulse width modulation(SPWM) techniques are utilized to drive the single phase diode clamped multilevel inverter (DCMLI) and hybrid inverter for different output levels. The structure of general multilevel inverter for different levels can be seen in in Figure 1.



Figure 1. Multilevel inverter structure for two, three and n-levelss

2. Multilevel Inverters

The analysis of diode clamped multilevel inverter and hybrid inverter are discussed based on sinusoidal pulse width modulation techniques.

2.1. Diode Clamped Multilevel Inverter

In order to produce seven levels by sinusoidal pulse width modulation, six saw-tooth waveforms for carrier and a sinusoidal reference signal for modulator are required in diode clamped multilevel inverter. Figure 2 and Figure 3 shows the carrier arrangement for APOD and PD techniques.



Figure 2. APOD pulse width modulation technique for single phase seven level DCMLI



Figure 3. PD pulse width modulation technique for single phase seven level DCMLI

2.2. Hybrid Multilevel Inverter

The hybrid multilevel inverter is a combination of two stages. One stage is level generation and other stage is polarity generation. First stage consists of high-frequency switches which produces the required positive levels. Whereas the other stage has low frequency switches which gives output polarity. Mainly the hybrid inverter eliminates higher number switches that are required to produce output levels. The single phase seven level diode clamped multilevel inverter using sinusoidal pulse width modulation requires six carriers, but three carriers are sufficient for hybrid multilevel inverter. The seven level hybrid inverter requires only three carrier waveforms and a sinusoidal reference signal. The carrier arrangement using alternate phase opposition disposition and phase disposition sinusoidal pulse width modulation methods are shown in Figure 4 and Figure 5.



Figure 4. APOD pulse width modulation technique for single phase seven level hybrid inverter





3. Simulation of DCMLI and Hybrid Inverter

The simulation models for producing gating signals in a single phase seven level diode camped multilevel inverter using alternate phase opposition disposition and phase disposition sinusoidal pulse width modulation methods are represented in Figure 6 and Figure 7.







Figure 7. Gating signals of seven level diode clamped inverter for PD PWM

The simulation model for producing gating signals in level generation stage of seven level hybrid inverter is represented in Figure 8 using alternate phase opposition disposition pulse width modulation method.



Figure 8. Simulation model for gating signals of level generation part

Figure 9 presents the simulation model for producing gating signals in polarity generation stage of seven level hybrid inverter.



Figure 9. Simulation model for gating signals of polarity generation part

4. Results and Discussion

The waveforms obtained for diode clamped and hybrid multilevel inverters are discussed in this section for R and R-L loads. The results obtained using LC filter are also presented. The results are shown for alternate phase opposition disposition method for modulation index (m_a)=0.9.

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4.1. Single Phase Diode Clamped Inverter

The results of diode clamped multilevel inverter for different loads are presented below for various levels. Figure10 to Figure 12 shows the results of seven level diode clamped multilevel inverter.





Figure 10. Voltage and current waveforms of seven level DCMLI for R load

Figure 11. Voltage and current waveforms of seven level DCMLI for R load using LC filter



Figure 12. Voltage and current waveforms of seven level DCMLI for R-L load

The results of nine level diode clamped multilevel inverter are shown from Figure13 to Figure 15. The waveforms obtained for eleven level diode clamped multilevel inverter are shown from Figure 16 to Figure 18.



Figure 13. Voltage and current waveforms of nine level DCMLI for R load



Figure 14. Voltage and current waveforms of nine level DCMLI for R load using LC filter



Figure 15. Voltage and current waveforms of nine level DCMLI for R-L load



eleven level DCMLI for R load



Figure 17. Voltage and current waveforms of eleven level DCMLI for R load using LC filter



Figure 18. Voltage and current waveforms of eleven level DCMLI for R-L load

4.2 Hybrid Multilevel Inverter

The results of hybrid multilevel inverter for different loads are presented in this section for various levels. The results obtained for single phase seven level hybrid multilevel inverter are shown from Figure 19 to Figure 21.



Figure 19. Voltage and current waveforms of seven level hybrid inverter for R load



Figure 20. Voltage and current waveforms of seven level hybrid inverter for R load using filter

Figure 21. Voltage and current waveforms of seven level inverter for R-L load

Figure 22 to Figure 24 represents the results for single phase nine level hybrid multilevel inverter.



Figure 22. Voltage and current waveforms of nine level inverter for R load



Figure 23. Voltage and current waveforms of nine level inverter for R load using LC filter

The waveforms of single phase eleven level hybrid multilevel inverter are shown from Figure 25 to Figure 27.



Figure 24. Voltage and current waveforms of nine level inverter for R-L load



Figure 25. Voltage and current waveforms of eleven level inverter for R load



Figure 26. Voltage and current waveforms of eleven level inverter for R load using LC filter



Figure 27. Voltage and current waveforms of eleven level inverter for R-L load

4.3. Comparative Analysis of Diode clamped and Hybrid Multilevel Inverters

FFT analysis is carried out for single phase diode clamped multilevel inverter and hybrid multilevel inverter at different levels at various modulation indices using phase disposition and alternate phase opposition disposition sinusoidal pulse width modulation techniques and are summarized from Table 2 to Table 5.

Table 1. Comparison of THD (%) with R-Load using PD method							
Output Level	Modulation index	Witho	ut Filter	With Filter			
		Diode clamped inverter	Hybrid multilevel inverter	Diode clamped inverter	Hybrid multilevel inverter		
Seven level	0.85	18.67	12.29	3.97	1.13		
	0.9	17.52	11.48	3.83	1.05		
	0.95	15.77	11.08	3.53	1		
	1	13.97	9.84	3.28	0.92		
	0.85	13.19	9.05	3.55	0.88		
Nine level	0.9	12.81	8.47	3.42	0.87		
	0.95	11.97	8.4	3.18	0.85		
	1	10.48	7.38	3.24	0.8		
Eleven level	0.85	10.02	7.15	2.5	0.79		
	0.9	10.11	6.8	2.84	0.8		
	0.95	9.54	6.65	2.57	0.83		
	1	8.25	6.05	3.12	0.77		

Table 2. Comparison of THD (%) with R-Load using APOD method

Output	Modulation	Witho	ut Filter	With Filter			
Level	index	Diode clamped inverter	Hybrid multilevel inverter	Diode clamped inverter	Hybrid multilevel inverter		
Seven level	0.85	18.5	12.21	3.18	1.1		
	0.9	17.58	11.56	3.01	1.02		
	0.95	15.74	11.12	2.93	0.99		
	1	13.86	9.7	2.79	0.86		
	0.85	13.01	8.96	2.85	0.81		
Nino Iovol	0.9	12.88	8.53	2.7	0.8		
Nine level	0.95	12.02	8.37	2.78	0.73		
	1	10.46	7.44	2.82	0.69		
Eleven level	0.85	9.77	7.34	2.54	0.72		
	0.9	10.22	6.93	2.96	0.71		
	0.95	9.75	6.52	2.61	0.70		
	1	8.38	6.02	2.84	0.66		

Table 3. Comparison of inverters in terms of current THD (%) using R-L load

PD method 7-Level 9-Level			11-Level 7-Level		APOD method 9-Level		11-Level				
DCMLI	Hybrid inverter	DCMLI	Hybrid inverter	DCMLI	Hybrid inverter	DCMLI	Hybrid inverter	DCMLI	Hybrid inverter	DCMLI	Hybrid inverter
4.81	4.8	4.81	4.79	4.75	4.77	4.83	1.79	4.81	4.82	4.79	4.79
4.81	4.83	4.79	4.81	4.77	4.75	4.81	4.79	4.82	4.82	4.78	4.79
4.79	4.79	4.79	4.81	4.74	4.75	4.81	4.81	4.82	4.83	4.8	4.8
4.79	4.77	4.8	4.79	4.76	4.79	4.81	4.71	4.81	4.83	4.78	4.78

5. Conclusion

The phase disposition and alternate phase opposition disposition SPWM control methods are implemented in this paper to drive the single phase diode clamped inverter and hybrid multilevel inverter for different levels at various modulation indices. The hybrid inverter requires less number of high frequency switches when compared to diode clamped multilevel inverter. It is observed that the hybrid inverter has superior features compared to conventional multilevel inverters in terms of the required switches, control requirements, cost, reliability and efficiency. The components required for different voltage levels for single phase hybrid inverter

are lower compared to conventional multilevel inverters. The hybrid inverter is a good potential for FACTS, STATCOM and HVDC applications. As the hybrid inverter requires low rated dc sources, the fuel cells, photovoltaic arrays can also be used as dc sources.

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References

- [1] A Nabae, I Takahashi, A Akagi. A new neutral-point clamped PWM inverter. *IEEE Trans. Ind. Appl.* 1981; 19: 518–523.
- [2] G Mondal, K Gopakumar, P N Tekwani, E Levi. A reduced switch-count five-level inverter with common-mode voltage elimination for an open-end winding induction motor drive. *IEEE Trans. Ind. Electron.* 2007; 54 (4): 2344–2351.
- [3] P M Bhagwat, V R Stefanovic. Generalized structure of a multilevel PWM inverter. *IEEE Trans. Industry Applications.1983; 19* (6): 1057-1069.
- [4] A Rufer. An aid in the teaching of multilevel inverters for high power applications. Proc. Rec. IEEE PESC'95. 1995; 347–352.
- [5] B Ravikumar, P Satish Kumar "Performance Analysis of Modified SVPWM Strategies for Three Phase Cascaded Multi-level Inverter fed Induction Motor Drive", *International Journal of Power electronics drives (IJPEDS)*, 2017; 8 (2): 835-843.
- [6] N Susheela, P Satish Kumar, C H Reddy. Performance Analysis of Four Level NPC and NNPC Inverters using Capacitor Voltage Balancing Method. IEEE Uttar Pradesh Section International Conference on Electrical, Computer and Electronics Engineering. Varanasi. 2016; 212-217.
- [7] G Carrara, S Gardella, M Marchesoni, R Salutari, G Sciutto. A new multilevel PWM method: a theoretical analysis. *IEEE Trans. Power Electronics*. 1992; 7 (3): 497–505.
- [8] J Rodriguez, J S Lai, F Z Peng. Multilevel inverters: A survey of topologies, controls, and applications. *IEEE Trans. Ind. Electron. 2002;* 49 (4): 724–738.
- [9] E Najafi, A H M Yatim, A S Samosir. A new topology-Reversing Voltage (RV)-for multilevel inverters. *IEEE* 2nd International Power and Energy Conference (PECon 08). 2008; 604 608.
- [10] S A Gonzalez, M I Valla, C F Christiansen. Analysis of a cascade asymmetric topology for multilevel converters. Proc. IEEE ISIE. 2007; 1027–1032.
- [11] N Susheela, P Satish Kumar, B Sirisha, "Hybrid Topologies of Multilevel Converter for Current Waveform Improvement", *International Journal of Inventive Engineering and Sciences 2013*;1 (4): 29-37.
- [12] E Beser, B Arifoglu, S Camur, E K Beser. Design and application of a single phase multilevel inverter suitable for using as a voltage harmonic source. *J. Power Electron.* 2010; 10 (2): 138–145.
- [13] G M Martins, J A Pomilio, S Buso, G Spiazzi. Three-phase low frequency commutation inverter for renewable energy systems. *IEEE Trans. Ind. Electron.2006;* 53 (5): 1522–1528.
- [14] Ehsan Najafi, Abdul Halim Mohamed Yatim. Design and Implementation of a New Multilevel Inverter Topology. *IEEE Transactions on Industrial Electronics.* 2012; 59 (11):4148-4154.
- [15] R Stala. Application of balancing circuit for dc-link voltages balance in a single-phase diodeclamped inverter with two three-level legs. *IEEE Trans. Ind. Electron.2011;* 58 (9): 4185–4195.
- [16] B Sirisha, N Susheela, P Satish kumar "Three Phase Two Leg Neutral Point Clamped Converter with output DC Voltage Regulation and Input Power Factor Correction" International Journal of Power Electronics and Drive System (IJPEDS), 2012; 2 (2): 138 -150.