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Modeling, Analysis and Comparative of Down Sampling based Clamping SV PWM for Cascaded and Diode Clamped Multilevel Inverter fed Induction Motor Drive

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Abstract

This paper presents investigation and performance analysis of novel down sampling based clamping SV PWM technique for diode and cascaded Multi-level Invereter fed to Induction motor drive. A novel down sampling based clamping SVPWM has developed by adding triangular off set to sinusoidal fundamental waveform is modified by down sampling the reference wave by order of 10 so this technique is called clamping space vector pulse width modulation techniques such as PD, POD and APOD. so as to shift the lower order harmonics to higher order side. This novel carrier is compared with the offset injected space vector reference waveform to generate the required PWM pulses to the inverter. To analyze the performance of the proposed PWM technique it is implemented on seven level diode and cascaded Multi-level Inverter using Matlab/Simulink software tool for output line, phase voltage, currents, speed, torque and Total harmonic distortion analysis.

Keywords*: Seven-level cascaded and diode clamped multi-level inverter, CSV PDSPWM, CSV PODSPWM, CSV APODSPWM, THD*

1. Introduction

Multi-level diode clamped voltage fed inverters are recently becoming very popular for multi-megawatt power applications. The main advantage of such an inverter topology is voltage division, i.e., the output voltage is produced through small steps of voltage, and therefore the individual switches are submitted only to these small voltages steps. The other advantages are low harmonic distortion at output, low *dv/dt* and extended range of under modulation. But it has the disadvantages like the increased number of switching devices and the complex control algorithm [1, 2].

At present, multilevel inverters (MLI) have emerged as attractive solution for medium-voltage and high power applications due to numerous advantages over two level inverters. The most poular multilevel topologies are diode-clamped (or) neutral-point-clamped (NPC), capacitor-clamped (or) flying capacitor (FC) and cascaded H-bridge (CHB) multilevel inverter [3, 4]. In literature, several modulation schemes have been developed for MLI applications. The classical sinusoidal PWM has been extended MLIs by using multiple carriers with either phase-shift (PS-PWM) or level-shift (LS-PWM) [5]. In addition PWM based hybrid modulation method has been suggested for CHB topologies with unequal dc sources in order to reduces the switching losses and improve of number of levels [5, 6].

New modulation technique such as Clamping Space vector Pulse width modulation technique is have been investigated in this paper. Which is generally simple implementation compared to other multi carrier based PWM techniques. This technique applied to seven level cascaded H-bridge multilevel inverter. The paper mainly deals with the computation and the comparison of the motor harmonic losses of proposed CSV PWM solutions and with the selection of the solutions providing the best results. Finally, the drive harmonic losses will be compared for each levels. Finally, simulation results verify the each level of the inverter.

2. Cascaded H-bridge Multilevel Inverter

The cascaded inverter uses number of single-phase full-bridge inverters connected in series to get multilevel in a phase. The resultant phase voltage is produced by the addition of the voltages generated by the individual cell. Three voltages at the output: +Vdc, 0, and -Vdc are produced by each single-phase full-bridge inverter. The main advantage of this topology is that the modulation, control, and protection of each bridge are modular, each inverter acts as a module with identical circuit topology, control structure, and modulation. Therefore, in case of failure in any one of the modules, replacement is easy. But, individual inverter requires its own dc supply. This drawback has generally confined the cascaded inverters to the high-power range where more levels of output voltage are required. The cascaded inverter can reach medium output voltage levels with the use of standard low-voltage semiconductor devices. Due to its modularity, control strategy and low harmonic distortion, these inverters have been used in very high power applications (over 4 kV and several MW). These inverters have been mainly used in the areas of static VAR compensators (SVCs), power line conditioner, voltage stabilizer and so on. The AC outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs [7, 8]. The levels in phase voltage are 2N+1, here N is 1-ϕ inverter cells present in a phase and the number of levels in line voltage are 2M-1, where M is the number of level in phase voltage shown in Figure 1.
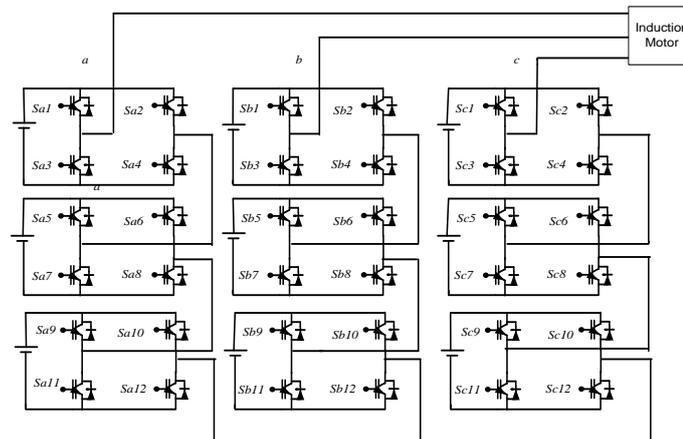
Figure 1. Seven level cascaded inverter
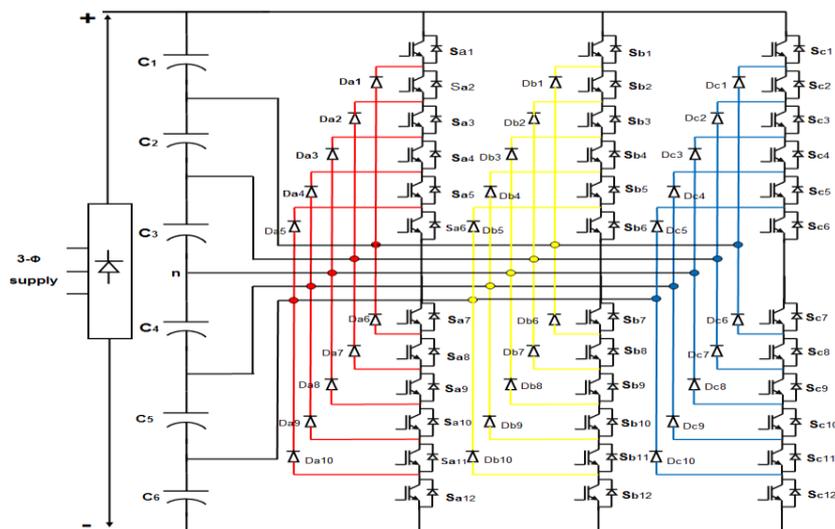
Figure 2. Seven level diode clamped inverter

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The structure and basic operating principle consists of series connected capacitors that divide dc bus voltage into a set of capacitor voltages. A DCMI with 'n' number of levels typically comprises (n-1) capacitors on the dc bus. Voltage across each capacitor is $V_{dc}/$ (n -1). The three-phase seven-level diode-clamped inverter is shown in Figure 2. Each of the three phases of the inverter shares a common dc bus, which has been sub divided by six capacitors into seven levels. The voltage across each capacitor is Vdc and the voltage stress across each switching device is limited to Vdc through the clamping diodes. The output voltage levels possible for one phase of the inverter with the negative dc rail voltage V_0 as a reference. State condition 1 means the switch is on, and 0 means the switch is off. Each phase has six complementary switch pairs such that turning on one of the switches of the pair require that the other complementary switch be turned off. The complementary switch pairs for phase leg 'a' are (Sa1, Sa7$_1$), (Sa2, Sa8), (Sa3 Sa9), (Sa4 Sa10), (Sa5 Sa11) and (Sa6, Sa12). Also shows that in a diode-clamped inverter, the switches that are ON for particular phase legs are always adjacent and in series. For a seven-level inverter, a set of six switches is ON at any given time [9, 10].

3. Generalized Down sampling based Space Vector Pulse Width Modulation Techniques for Multilevel Inverter

The control principle of the SPWM is to use several triangular carrier signals keeping only one modulating sinusoidal signal. For a m-level inverter, (m-1) triangular carriers are needed. The carriers have the same frequency (fc) and the same peak to peak amplitude AC. The modulating signal is a sinusoid of frequency (fm) and amplitude (Am). At every instant, each carrier is compared with the modulating signal. Each comparison switches the switch "on" if the modulating signal is greater than the triangular carrier assigned to that switch [11]. The main parameters of the modulation process are:
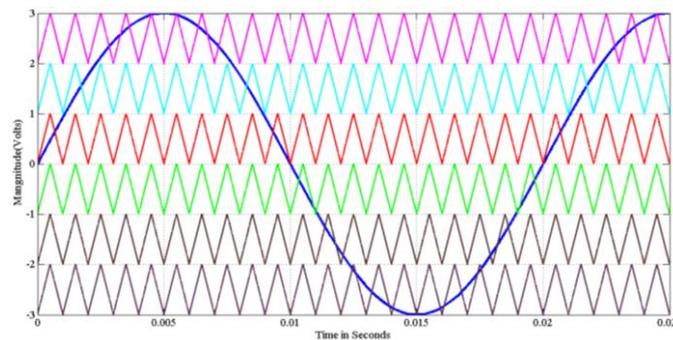
Figure 3. PDSPWM

3.1 Modulation Index

The modulation index is the ratio of peak magnitudes of the modulating signal V$_m$ and the carrier signal:

$$m = \frac{Vm}{Vc} \tag{1}$$

The modulation index in SPWM technique for cascaded multilevel inverter configuration is given by:

$$m = \frac{Vm}{(N-1)Vc} \tag{2}$$

Where N is number of levels. For under modulation 0<m<1. For over modulation m>1.

Generally, over modulation is not desired because of the presence of the lower frequency harmonics in the output voltage and subsequent distortion in the load current.

3.2 Frequency Modulation

It is the ratio of frequency of the triangular carrier signal f_C to the frequency of sinusoidal reference signal f_S. It controls harmonics in the output voltage.

$$mf = \frac{fc}{fs} \tag{3}$$

A novel down sampling based SVPWM has developed by adding triangular off set to sinusoidal fundamental waveform so as to shift the lower order harmonics to higher order side. This novel carrier is compared with the offset injected space vector reference waveform to generate the required PWM pulses to the inverter.

$$Voffset = \frac{-(V\max + V\min)}{2} \tag{4}$$

Vmax is maximum of VAN, VBN,VCN

Vmin is minimum of VAN, VBN,VCN

$$Ta = \frac{-(Va * Ts)}{Vdc} \tag{5}$$

$$Tb = \frac{-(Vb * Ts)}{Vdc} \tag{6}$$

$$Tc = \frac{-(Vc * Ts)}{Vdc} \tag{7}$$

An important detail is taken into account to avoid the function operating in negative values, which makes use of another offset in the reference voltage [12, 13]. Thus, substituting Equation (3), (4), (5) into Equation (1) and adding this offset, the Equation (5), (6), (7) is obtained.

$$Toffest = [\frac{To}{2} - T\min] \tag{8}$$

$$To = [Ts - Toffest] \tag{9}$$

$$Toffeset = [T\max - T\min] \tag{10}$$

In this paper, a simple technique to determine the offset voltage (To be added to the reference phase voltage for PWM generation for the entire modulation range) is presented, based onely on the sampled amplitudes of the reference phase voltages. The proposed modified reference PWM technique presents a simple way to determine the time instants at which the three reference phases cross the triangular carriers. To obtain the maximum possible peak amplitude of the fundamental phase voltage in linear modulation, the procedure for this is given in [14, 15].Shown in Figure 4.

After the modified SVPWM technique output, we can do the Down sampling of the order 10 each phase. Which is also sometimes called decimation, down sampling used for reduces the sampling rate and removes the samples from the signal. Whilst maintaining its length with respect to time. Some mathematically analysis to find out the down sampling shown in bellow, we can used descriptive time is 2e-6, sampling frequency is one by descriptive time ($10^6/2$), number of samples per phase is the ratio of sampling frequency by fundamental frequency such as 10k samples, in order reduced the down sampling by order of 10 such as 1k samples. By using the down sampling based modified space vector PWM technique such as PD, POD and APOD. We can observe the reduced the THD in output line voltage. We can observe the Figure 2, Figure 3 and Figure 4 is shown in the waveform results generated by adding the offset voltage described in with the reference sinusoidal waveform.
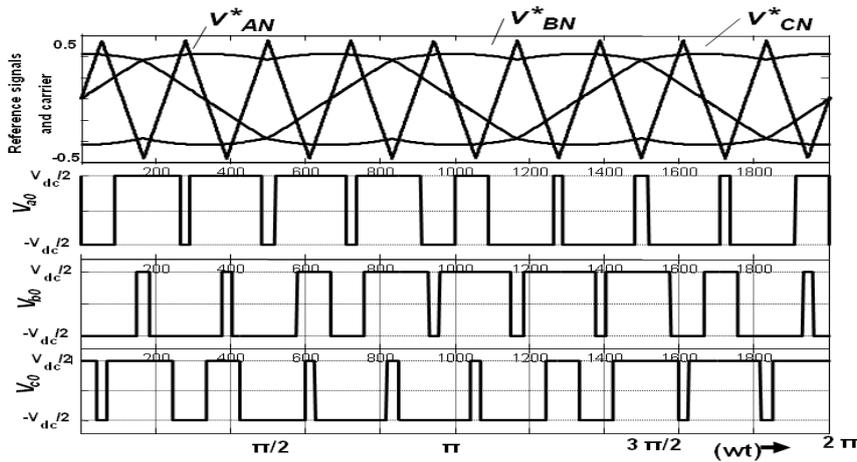
Figure 4. Carrier based SVPWM
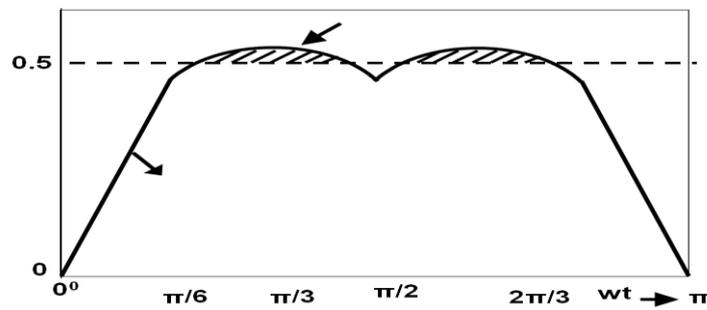
Figure 5. Linearization of the multilevel SVWM in over modulation region
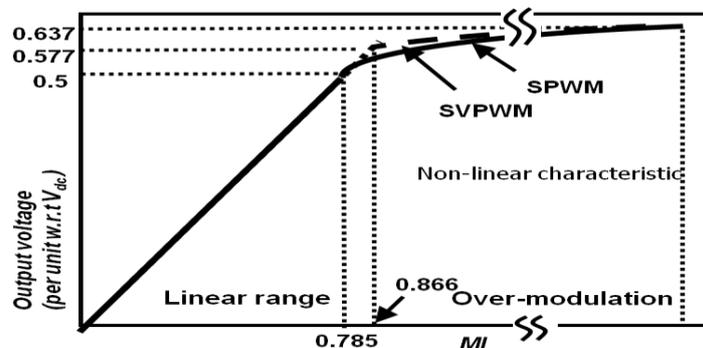
Figure 6. Linear and non linear characteristics of the multilevel SVPWM in modulation region

Again when reference signal is greater than carrier, the pole voltages are clamped to the DC link bus voltage. There is reduction in the fundamental component in the output voltage. Reduction in the output fundamental is proportional to the shaded area shown in Figure 5. The extended linear region in SVPWM as compared to SPWM shown in Figure 4. The voltage transfer characteristics is again non linear in the over modulation region similar to SPWM. An over-modulation scheme with the linear voltage transfer characteristics for a general *n*-level SVPWM signal generation. Reference signal to the PWM modulator is pre-scaled in over-modulation region such that the fundamental component of the original and the modified reference signal is same.The modified reference signal is always within carrier region. Thus voltage transfer characteristic is a linear function of the modulation index both in the linear-modulation as well as in the over-modulation region. The inverter leg switching times are directly obtained with a simple algorithm using only the sampled amplitudes of the reference phase voltages. Shown in Figure 6, Figure 7 and Figure 8.
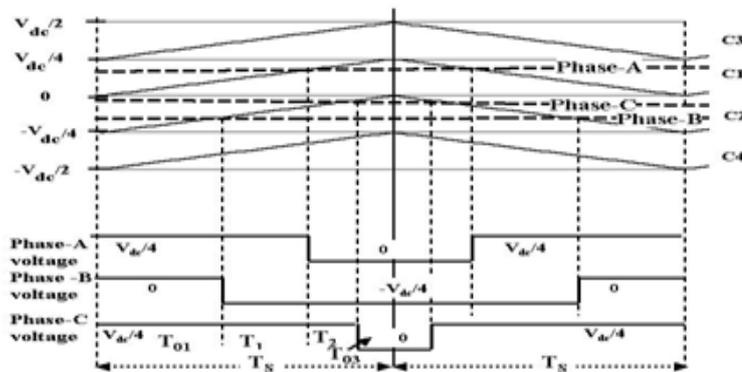
Figure 7. The inverter switching vectors and their switching time durations during sampling interval T_S (Reference voltages are within the inner carrier region, M < 0.433)
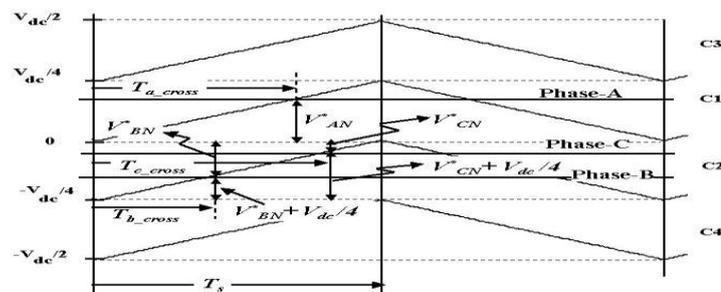
Figure 8. Determination of the T_{a_cross}, T_{b_cross} and T_{c_cross} during switching interval T_S (When reference voltages are spanning the inner carrier region, M < 0.433)
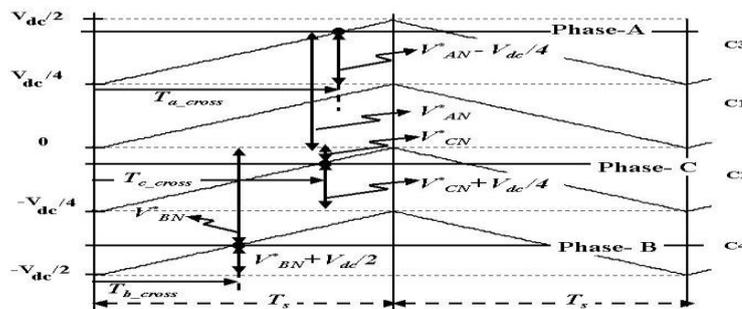
Figure 9. Determination of the T_{a_cross}, T_{b_cross} and T_{c_cross} during switching interval T_S (When reference voltages are spanning the entire carrier region, 0.433<M < 0.866
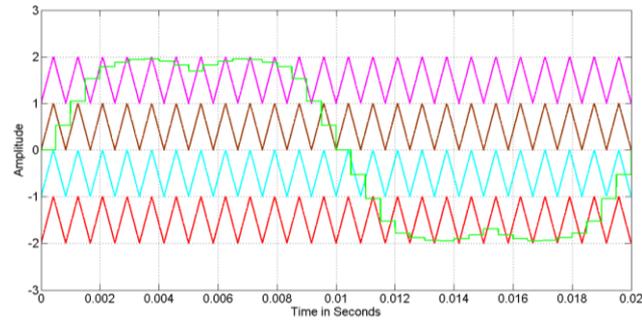
Figure 10. Down sampling based CSV PDPWM
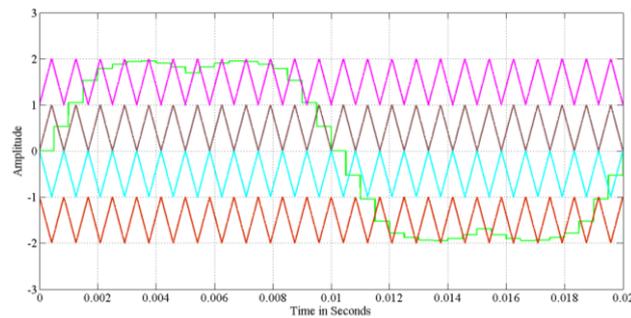
Figure 11. Down sampling based CSV PODPWM
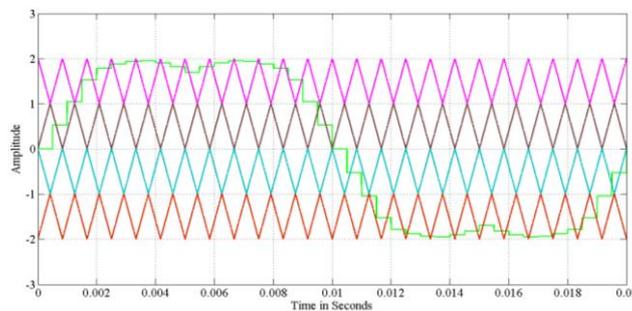
Figure 12. Down sampling based CSVAPODPWM

The pulse generation of the different down sampling based SVPWM techniques shown in above figures. Figure 10 Indicates the CSV PDPWM techniques, Figure 11. Indicates the CSV PODPWM techniques, Figure 12 Indicates the CSV APODPWM techniques.

3. Simulation Results and Discussions
The simulation study has performed and carried out three-phase seven level cascaded and diode clamped multilevel inverters behavior based on comparative regarding down sampling based clamping SVPWM control strategy such as CSV PDPWM, CSV PODPWM and CSV APODPWM techniques. In this simulation the carrier frequency used in this designed is about 1KHz.
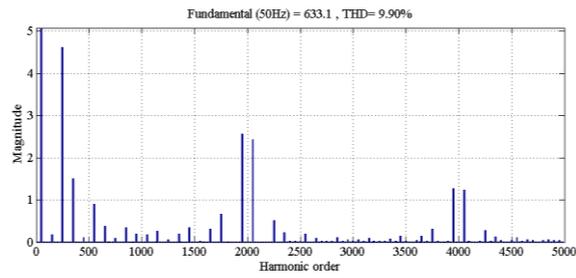
Figure 13. Seven level CHB CSV PDPWM
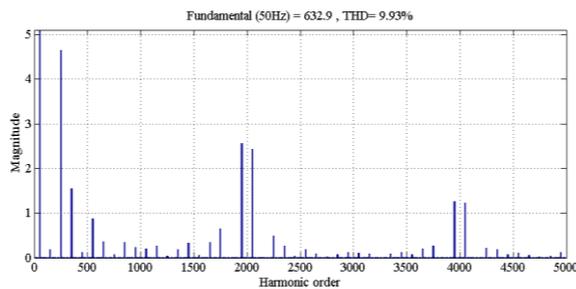
Figure 14. Sive level CHB CSV PODPWM
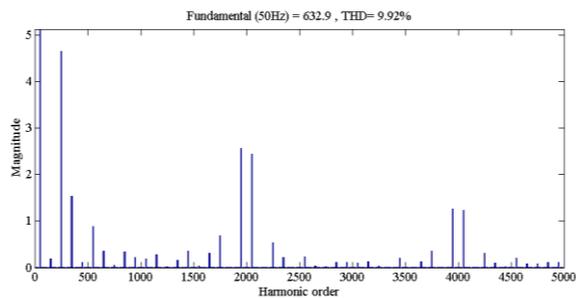
Figure 15. Seven level CHB CSV APODPWM

The seven level CHBMLI we have done matlab simulation using down sampling based clamping space vector PWM techniques. We have observe the performance of THD and load of the induction motor. The fft analysis of seven level inverter for both technique show in   Figure 13, Figure 14 and Figure 15. In the seven level single phase CMLI contain three H-bridges with series connections with the output phase voltage is 7 level and line voltage is 13 level of the inverter.
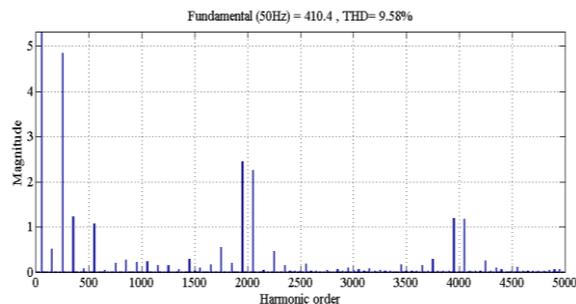
Figure 16. Seven level NPC CSV PDPWM
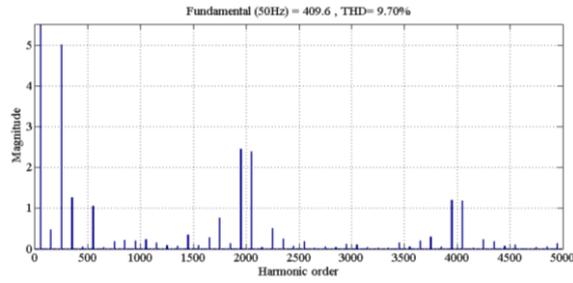
Figure 17. Seven level NPC CSV PODPWM
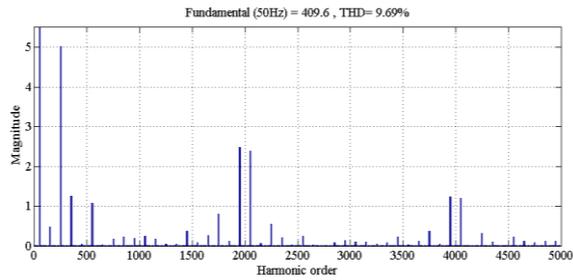
Figure 18. Seven level NPC APODPWM

The seven level diode clamped MLI we have done matlab simulation using down sampling based clamping space vector PWM techniques. We have observe the performance of THD and load of the induction motor. The fft analysis of seven level inverter for both technique show in Figure 16, Figure 17 and Figure 18. In the seven level single phase CMLI contain three H-bridges with series connections with the output phase voltage is 7 level and line voltage is 13 level of the inverter. We can observe the CSV-PDPWM techniques is perfect with the low THD, voltage and current shapes of the seven level CMLI. The comparision of THD for diode clamped and cascaded inverter using down sampling based SVPWM techniques shown in Table 1 and Table 2.

Table 1. The THD Performance of seven level cascaded inverter

S.No	PWM Techniques	THD% (V)
1	CSV PDPWM	9.90
2	CSV PODPWM	9.93
3	CSVAPODPWM	9.92

Table 2. The THD Performance of seven level diode clamped inverter

S.No	PWM Techniques	THD% (V)
1	CSV PDPWM	9.58
2	CSV PODPWM	9.70
3	CSVAPODPWM	9.69

Table. 3. Specifications of induction motor parameters

Parameters	Specifications
Input voltage	400VRMS(PhasePhase)
Inverter voltage	100(Volts)
Rotor speed	1440(RPM)
Fundamentalfrequency	50(Hz)
Switching frequency	1K (Hz)
Reference speed	1500(RPM)
Frequency modulation	200
Amplitude modulation	0.6
Sampling order	10

4. Conclusion

In this paper dealy with a new down sampling based modified Space vector Pulse width modulation technique so called Clamping Space vector Pulse width modulation technique. The reference sine wave generated as in case of conventional off set injected SVPWM technique is modified by down sampling the reference wave by order of 10. The comparison of THD of the proposed control strategies for seven level diode clamped and cascaded inverter. When compared, it is obvious that CSV PDPWM is the most efficient control strategy with low THD for all level of inverter. The THD analysis, line voltages, stator currents and speed and torque of the machine are calibrated and compared confirming the good-quality waveforms.

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