

# Voltage Sag Compensation in Fourteen Bus System during Line Interruption Using Interline Dynamic Voltage Restorer

Suresh. P\*, Baskaran. B

EEE Department, Annamalai University, No 47, Sri Krishna Nagar 3rd Cross Street, Chennai-77, Tamilnadu, India .Tel:+91-9094507054

\*Corresponding author, e-mail: suresh.sjce2@gmail.com

## Abstract

*This paper deals with power quality improvement in fourteen bus system (FBS) using IDVR. Investigations were carried out to find the improvement of real and reactive power by employing IDVR during line outage condition. The closed loop responses of PI, PID and FL controlled systems are modelled and simulated using simulink and the results are obtained. Load flow studies were conducted for healthy system, FBS with line outage and FBS with line outage with inclusion of IDVR. The simulation studies indicate that, the voltage under line outage condition with IDVR is almost equal to the voltage under healthy condition. The Responses of closed loop systems with PI, PID and FLC are compared and the analysis shows the improvement in dynamic response in terms of settling time, rise time and peak time and reduces the steady state error. The advantages of proposed system is improved voltage stability, flexibility to control real and reactive powers and concluded that FLC based IDVR system had better time response. The prototype for four bus system with IDVR is modelled and the results are obtained.*

**Keywords:** Flexible AC Transmission System (FACTS), Fuzzy, Fourteen Bus System (FBS), Interline Dynamic Voltage Restorer (IDVR), Power Quality, Proportional Integral (PI), Proportional Integral Derivative (PID)

**Copyright © 2017 Institute of Advanced Engineering and Science. All rights reserved.**

## 1. Introduction

Nowadays, power electronics plays a vital role in transmission lines and industries. Because of the very sensitive and less tolerant equipment are used. Therefore for a short time, voltage sag occurs in these places. Voltage sag is created by connecting an additional load in parallel with the existing load. Among the several novals, the dynamically voltage restorer is one of the power electronics devices which is technically advanced over economical for voltage sag mitigation in distribution system [1]. The DVR works by injecting ac voltage in series with the incoming supply voltage, the purpose of which is used to improve voltage quality. DVR involves injection of real and reactive power to the distribution system to compensate the voltage sag problems which determines the capacity of the energy storage devices. In order to meet the real power requirement an external energy storage is required especially for mitigating long duration voltage sag compensation, the maximum amount of real power which is supplied to the load is a deciding factor of DVR, while the reactive power is generated electronically by using VSI voltage injection from the DVR is an appropriate phase advanced with respect to source side voltage can reduce energy consumption. For some phase advance technique alone, energy requirement cannot be met [2]. Therefore for mitigating deep long duration sags, as it is merely a way of optimizing existing energy storage. By dynamically replenished the DC link of the DVR that can be capable of mitigating deep sags with long durations.

The interline DVR proposed in this paper is to introduce a new way that recovers the energy in the common variable DC energy storage. IDVR is the combination of different DVRs which protect the sensitive loads in various distribution feeders. These feeds are originated from different grid substations. These DVRs are connected to common DC link. The above proposed theory deals with the balancing problems in no of transmission lines at a given substation. In [3] IPFC, the real power is transferred directly between the compensating lines and the reactive power is transferred within each individuals lines. Similarly in IDVR transfer the real power

between the sensitive loads in individual's lines. In IPFC the lines are originated from single grid substation whereas IDVR lines are originated from different substations. In IDVR one of the DVR, compensate the voltage sag by transferring the real power from DC link while the DC link voltage at specific level other DVRs are used. Generally, there are two control schemes, open loop [4] and closed loop [5], which is used in the DVR applications. The above discussion does not deal with comparison of fourteen bus system with and without line interruption. The objective of proposed system is to compare the response with closed loop controllers using IDVR. The organization of the paper is as follows: Section II deals with configuration of IDVR. Section III provides the results of contingency analysis. Section IV compares the simulation results of closed loop controllers with IDVR. Section V shows the experimental setup.

**2. Interline Dynamic Voltage Restorer System**

The interline dynamic voltage restorer consists of four bus connected with two source supplying different load. If sag occurs in feeder 1, the compensating voltage reactive power supplied to the load through feeder 2 with IDVR. The above process is developed further by increasing the no of buses in order to increase real and reactive power for compensation. The fourteen bus system is developed with IDVR employing PI, PID and FUZZY controllers in closed loop. Hence this method provides had better time response. Consider two feeders supplying different load. Here voltage sag occurs in feeder 1, the load is disconnected from feeder 1 and it is supplied with IDVR. Simulation of voltage insertion is implemented by a voltage loss across series connected impedance and reactance.

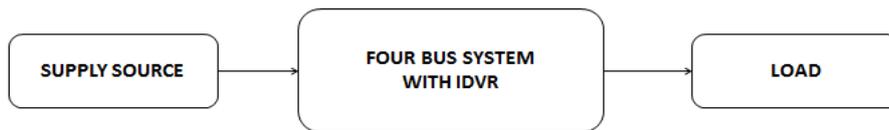


Figure 1. Block Diagram of Existing Method

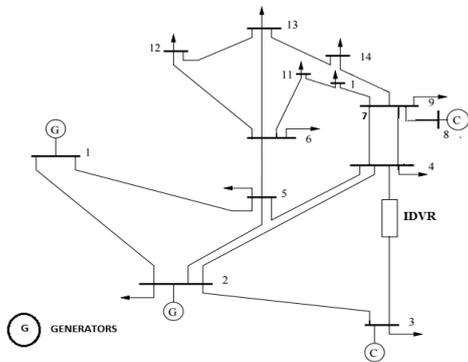


Figure 2. Single line diagram of Proposed Fourteen Bus System with IDVR

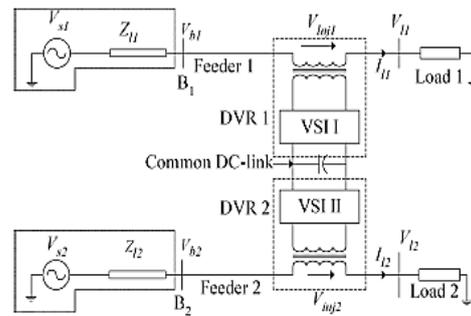


Figure 3. Interline Dynamic Voltage Restorer

Magnitude of load voltage should not disturb by impedance insertion. To keeping the load voltage magnitude unvaried, the insertion of voltage having two components likely V<sub>r</sub> real power and V<sub>y</sub> reactive power. In real power absorption V<sub>r</sub> is in phase according to their relative phasor and reactive power V<sub>y</sub> takes place between the load voltage V<sub>L</sub> which it does not change the voltage magnitude. Figure 4 shows the equivalent circuit diagram of feeder with series voltage impedance injection. Figure 5 shows the phasor diagram of feeder.

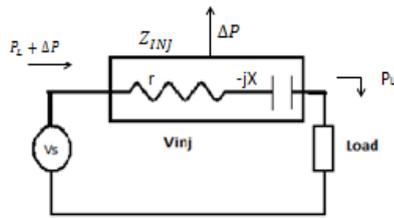


Figure 4. Equivalent circuit diagram of feeder with series injection

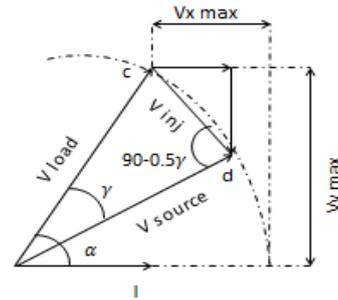


Figure 5. Phasor diagram of Feeder

Input Power is given by

$$P_L + \delta p = VI \cos(\alpha - \gamma) \tag{1}$$

Output Power is given by

$$P_L = VI \cos(\alpha) \tag{2}$$

Here

$$\gamma = \alpha - \cos^{-1}\left(\frac{P_L + \delta p}{VI}\right) \tag{3}$$

The power factor angle  $\gamma$  and maximum angle  $\alpha$  will be unity. The maximum value for  $\delta p$  is given by

$$\delta p_{max} = VI(1 - \cos(\alpha)) \tag{4}$$

Absorbed real power from feeder resistance  $r$  is given by

$$r = \frac{\delta p}{I^2} = \frac{VI(\cos(\alpha - \gamma) - \cos(\alpha))}{I^2} \tag{5}$$

Length  $cd$  is given by

$$|Vinj| = 2V \sin(0.5\gamma) = \sqrt{Vr^2 + Vy^2} \tag{6}$$

Capacitive reactance  $Cx$  can be given as

$$Cx = \sqrt{\frac{(Vinj)^2 - Vr^2}{I^2}} \tag{7}$$

Substitute  $Vinj$  value in 7 equation we get

$$Cx = \sqrt{\left(4 \frac{V^2}{I^2} \sin^2(0.5\gamma) - r^2\right)} \tag{8}$$

### 3. Results and Analysis

Contingencies are defined as potentially harmful disturbances that occur during the steady state operation of a power system. Load flow constitutes the most important study in a power system for planning, operation and expansion. The purpose of load flow study is to compute operating conditions of the power system under steady state. These operating

conditions are normally voltage magnitudes and phase angles at different buses, line flows (MW and MVAR), real and reactive power supplied by the generators and power loss.

**3.1. Normal Condition**

Fourteen bus systems with IDVR under normal condition is shown in Figure 6. The voltage at bus 4 is shown in Figure 7 and its peak value is 4000V. The RMS voltage at bus 4 is shown in Figure 8 and its value is 2750V. The real and reactive powers at bus 4 are shown in Figure 9. The value of real power  $2.5 \cdot 10^5$ W reactive power  $2.6 \cdot 10^4$ VAR

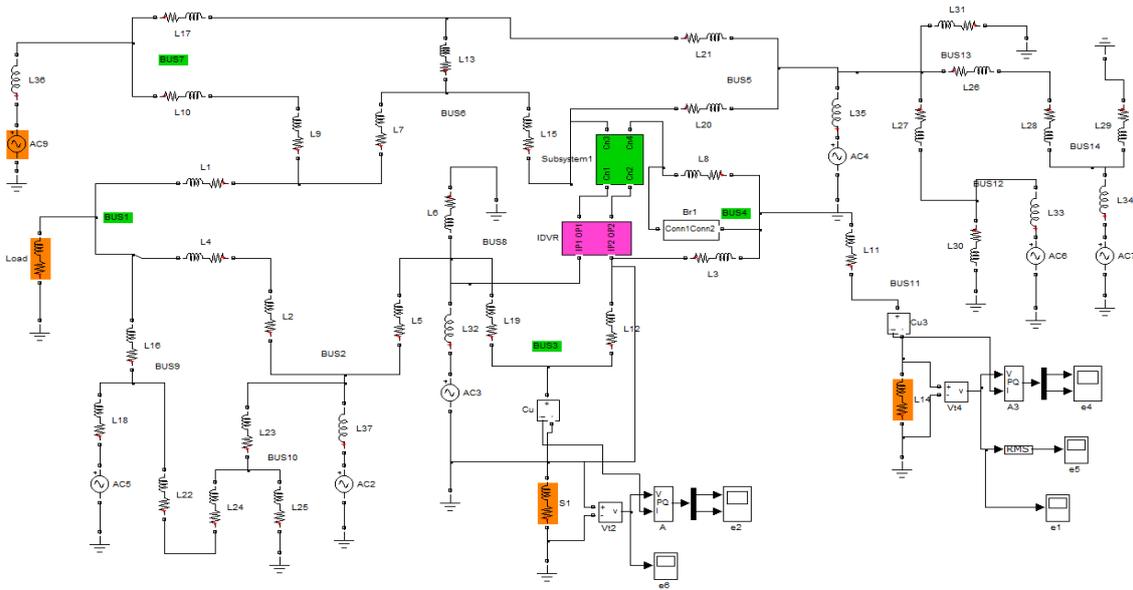


Figure 6. Simulink model for Fourteen Bus System with IDVR under Normal Condition

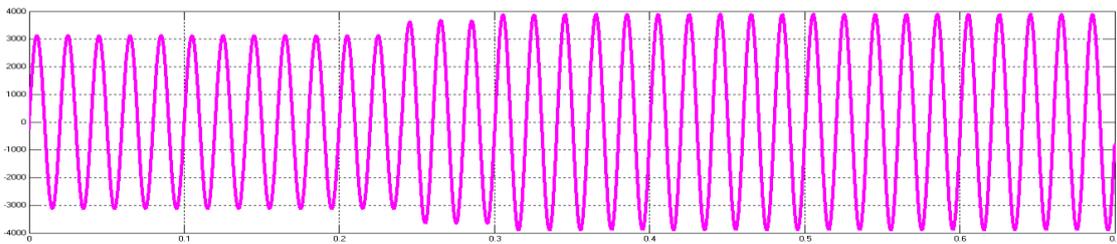


Figure 7. Simulation results for Voltage at bus-4

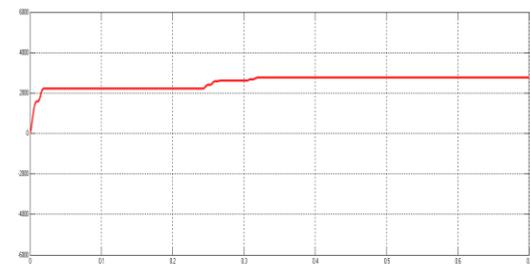


Figure 8. Simulation results for RMS voltage at bus-4

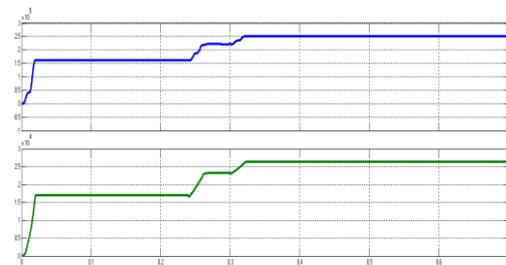


Figure 9. Simulation results for Real & Reactive power at bus-4

**3.2. Line 2 Open and IDVR Off Condition**

The fourteen bus system with line 2 open and IDVR off condition system is shown in Figure 10. The voltage of bus 4 is shown in Figure 11 and its peak value is 3000V. The RMS voltage at bus 4 is shown in Figure 12 and its value is 2000V. The real and reactive powers at bus 4 are shown in Figure 13 and its value of real and reactive power is  $1.5 \cdot 10^5$ W and reactive power is  $1.7 \cdot 10^4$ VAR.

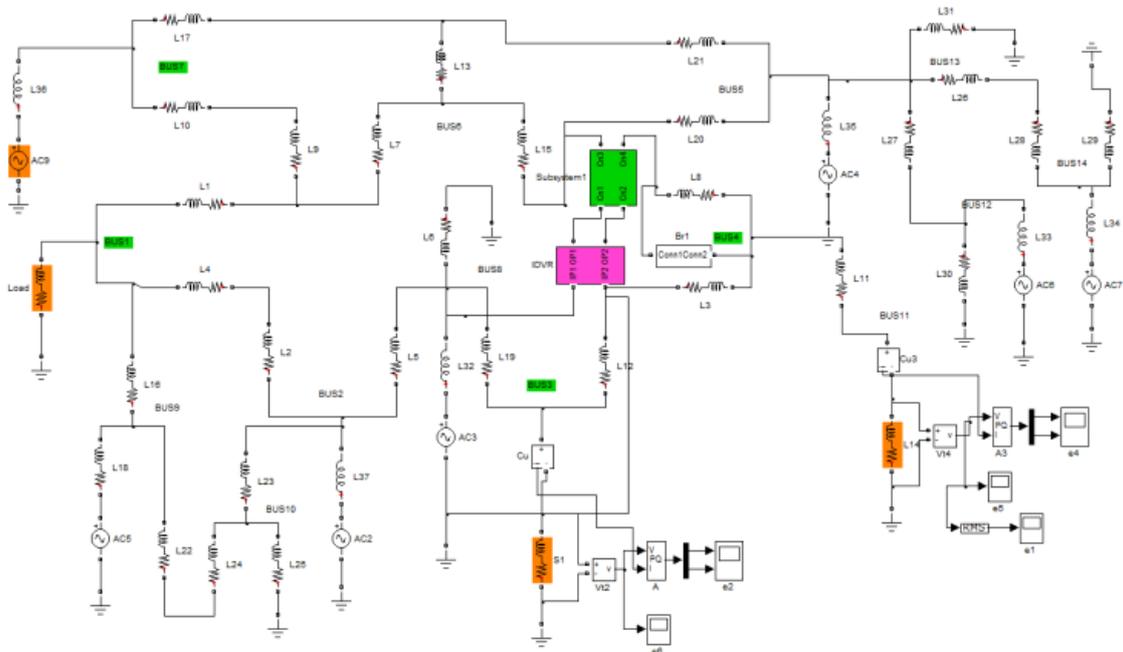


Figure 10. Simulink model of fourteen bus system with Line 2 open and IDVR off condition.

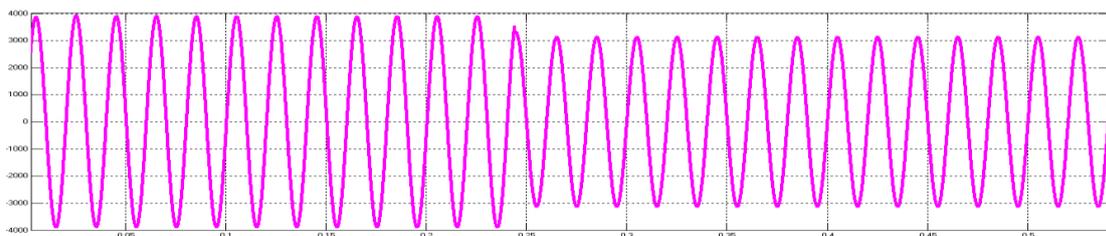


Figure 11. Simulation results for Voltage at bus-4

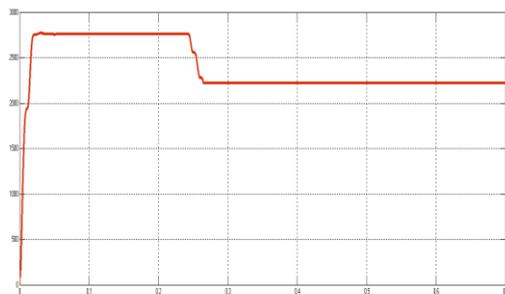


Figure 12. Simulation results for RMS voltage at bus-4

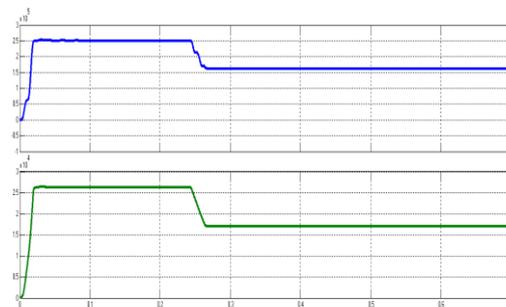


Figure 13. Simulation results for Real & Reactive power at bus-4.

### 3.3. Line 2 Open and IDVR on Condition

Fourteen bus system with line 2 open and IDVR on condition system is shown in Figure 14. The voltage at bus 4 is shown in Figure 15 and its peak value is 3800V. The RMS voltages at bus 4 are shown in Figure 16 and its value is 2600V. The real and reactive powers at bus 4 are shown in Figure 17 and its value of real power is 0.225MW and reactive power is 0.023MVAR.

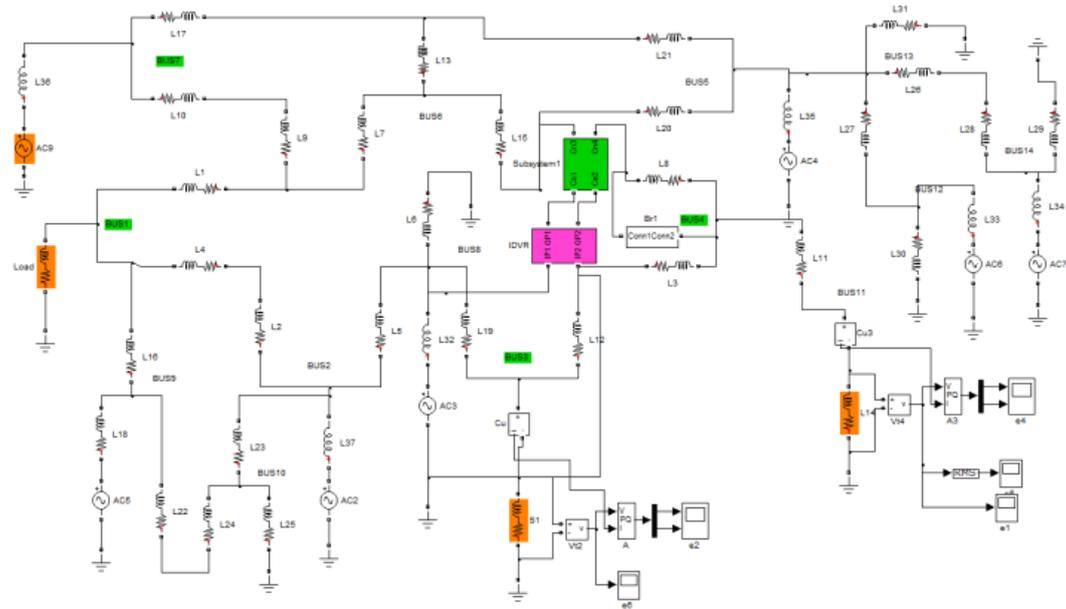


Figure 14. Simulink Model of Fourteen Bus System with Line 2 Open and IDVR On Condition

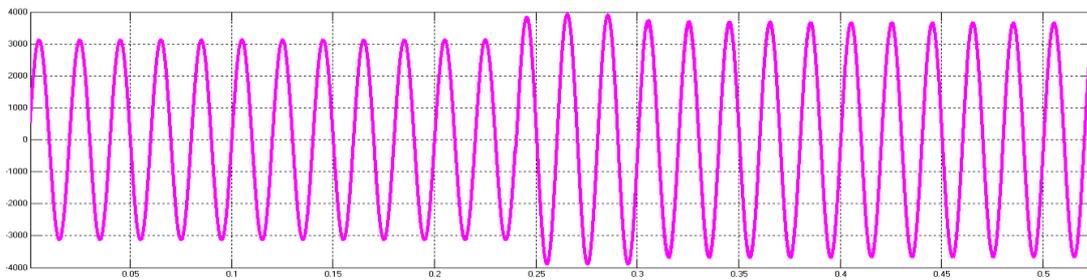


Figure 15. Simulation results for Voltage at bus-4

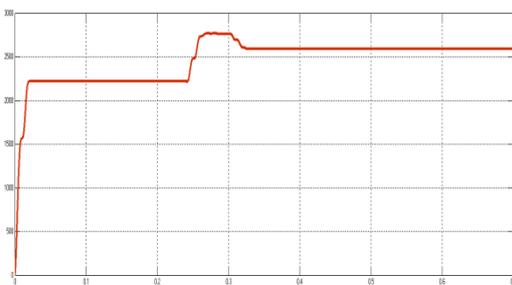


Figure 16. Simulation results for RMS voltage at bus-4

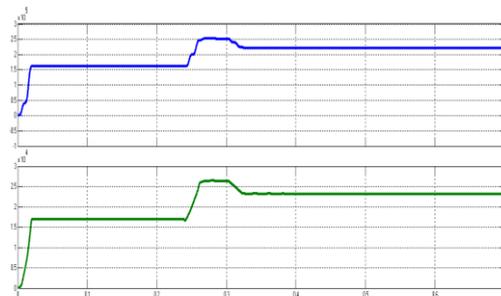


Figure 17. Simulation results for Real & Reactive power at bus-4

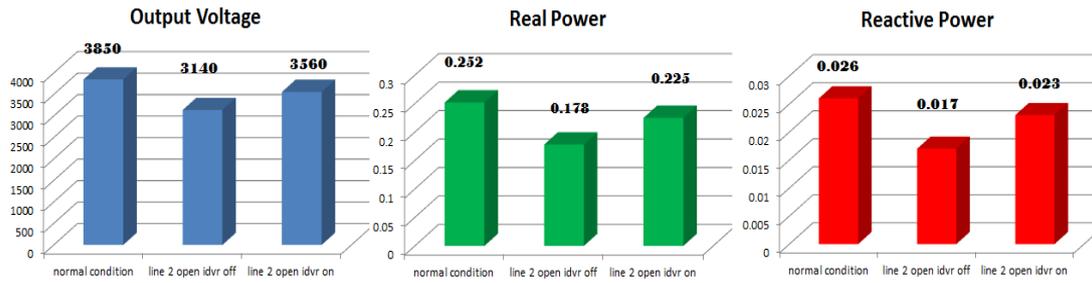


Chart 1. Comparison of Output voltage, Real and Reactive Power

4. Closed Loop Response

4.1. Design of PI Voltage Controller

PI controller is mainly used to eliminate the steady state error resulting from P controller. However, in terms of the speed of the response and overall stability of the system, it has a negative impact.

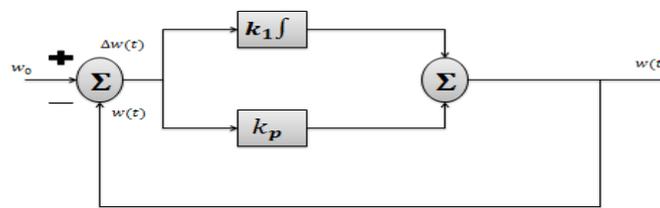


Figure 18. Design of PI Controller

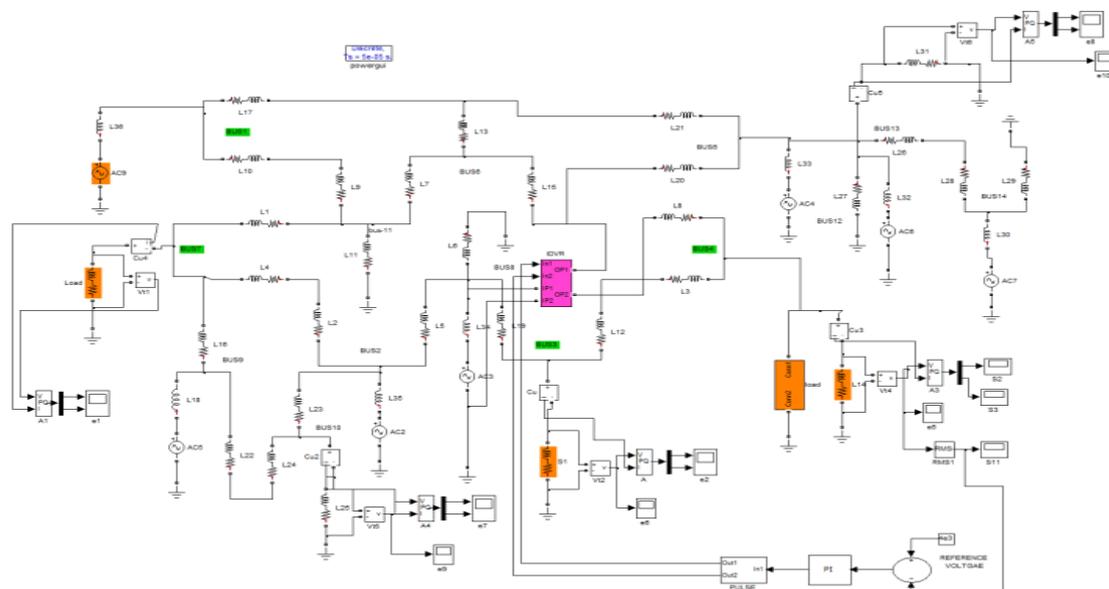


Figure 19. Simulink Model for Fourteen bus IDVR System with PI Controller

The Simulink diagram of the closed loop controlled IDVR system with the PI controller is shown in the Figure 19. The AC output voltage of the CT is rectified using a controlled rectifier. The DC is converted into AC using a PWM inverter, and the output voltage of the inverter is injected using a transformer. The load voltage is sensed and it is rectified and compared with a

reference voltage .The error signal is applied to the PI controller .The output of the PI controller is used to produce the required pulse width for the switches of the inverter. The voltage across the load 3 and the load 4 are shown in Figure 20.The peak value is 3500V. The RMS voltage is shown in Figure 21 and its value is 2500V. The new load is connected at 0.33 seconds and the voltage is compensated at 0.42 seconds

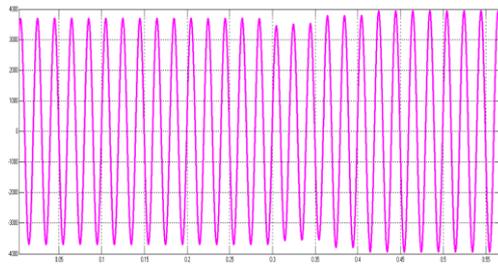


Figure 20. Output voltage waveform of fourteen bus IDVR with PI controller.

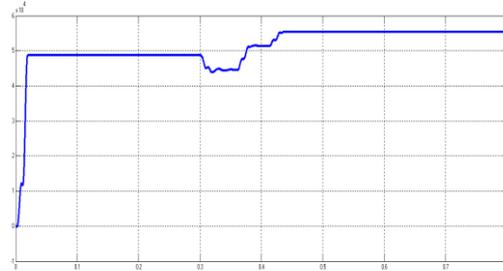


Figure 22. Real power waveform of fourteen bus IDVR with PI controller

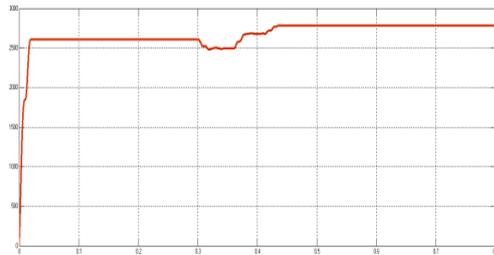


Figure 21. RMS Voltage waveform of fourteen bus IDVR with PI controller

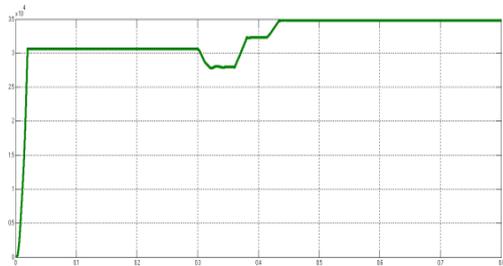


Figure 23. Reactive power waveform of fourteen bus IDVR with PI controller

#### 4.2. Design of PID Controller

PID controller has the optimum control dynamics including zero steady state error, short rise time, oscillation free and high stability. The necessity of using a derivative gain component in addition to the PI controller is to eradicate the overshoot and the oscillations occurring in the response of the system. One of the main advantages of the PID controller is that it can be used with higher order processes including more than single energy storage.

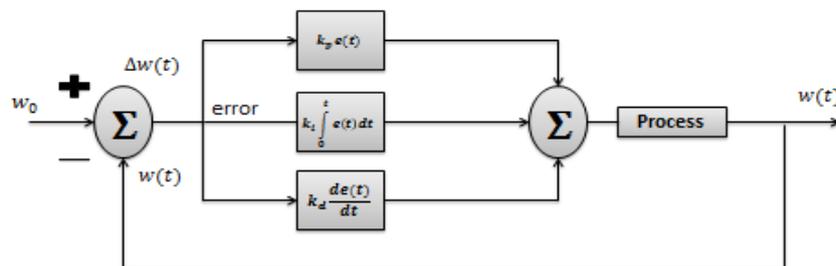


Figure 24. Design of PID Controller

Closed loop system with the PID controller is shown in Figure 25. The voltage across the load 3 and the load 4 are shown in Figure 26.The RMS voltage across the load is shown in Figure 27 and its value is 2500V. The new load is connected at 0.32 seconds and the voltage is compensated at 0.37 seconds.

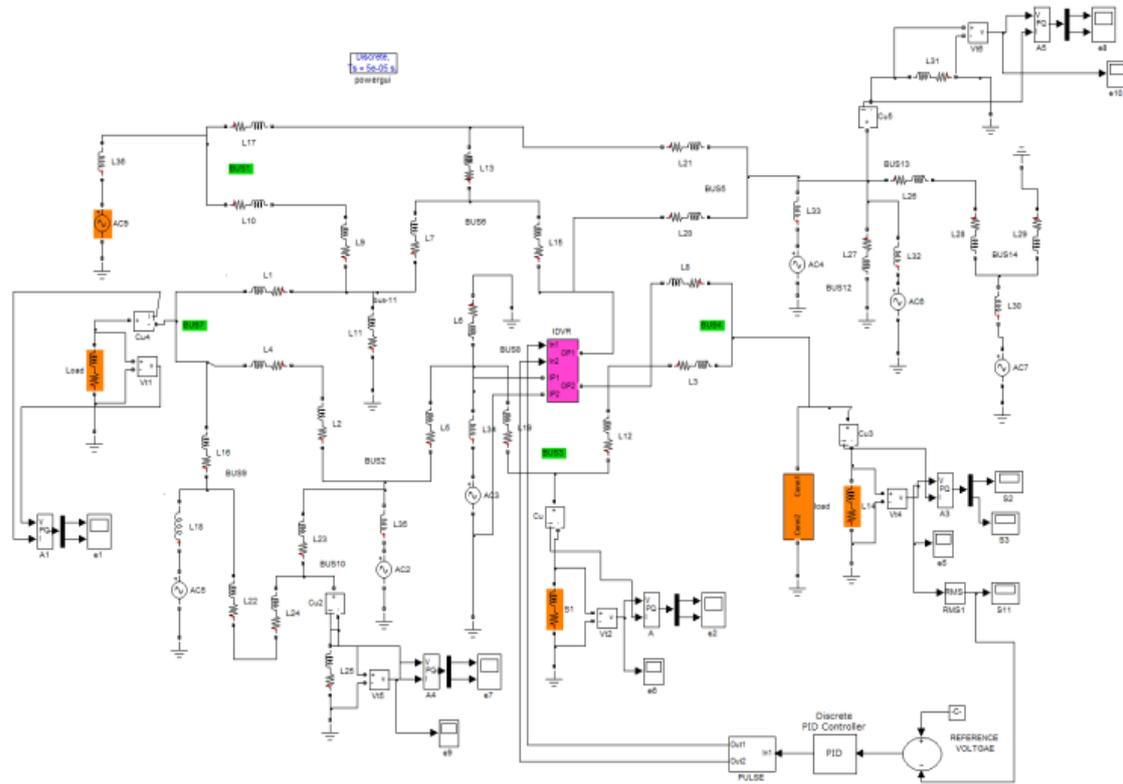


Figure 25. Simulink Model for Fourteen Bus IDVR system with PID controller

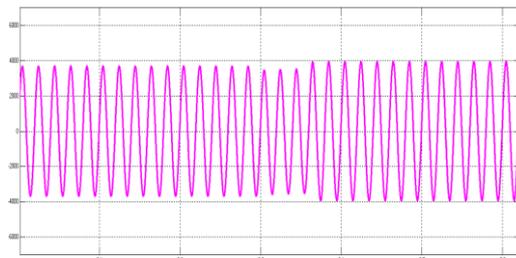


Figure 26. Output voltage waveform of fourteen bus IDVR with PID controller

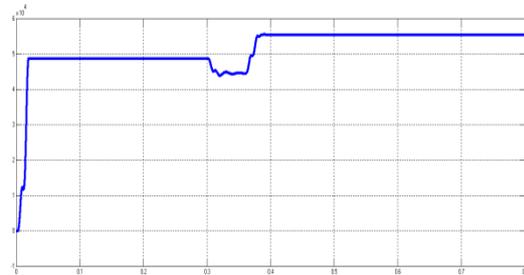


Figure 28. Real power waveform of fourteen bus IDVR with PID controller.

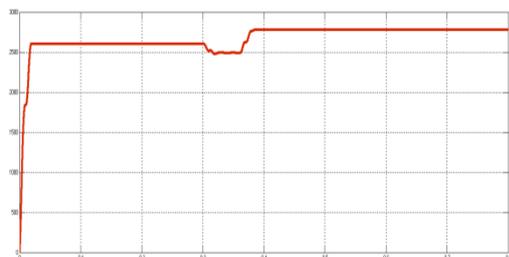


Figure 27. RMS Voltage waveform of fourteen bus IDVR with PID controller

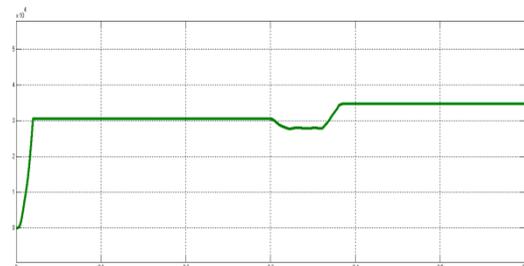


Figure 29. Reactive power waveform of fourteen bus IDVR with PID controller

**4.3. Sub Section 2**

A fuzzy logic controller consists of three main operations: Fuzzification, Inference Engine and Defuzzification. The input crisp or numerical data are fed into fuzzy logic rule based system where substantial quantities are represented into linguistic variables with appropriate membership functions. These linguistic variables are then used in the antecedents of a set of fuzzy "IF-THEN" rules within an inference engine to result in a new set of fuzzy linguistic variables or consequent.

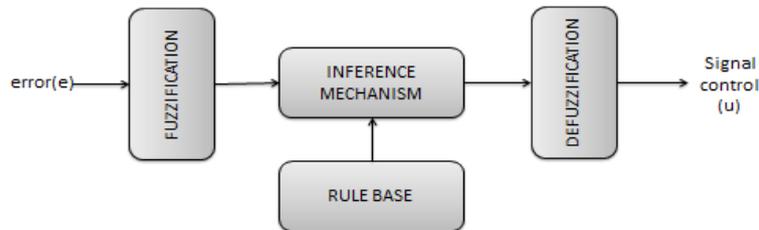


Figure 30. Design of Fuzzy Logic Controller

Simulink model of closed loop system with FLC is shown in Figure 31. The PID controller is replaced by FLC voltage across load 3 and load 4 are shown in Figure 32. The RMS voltage across the load is shown in Figure 33. The new load is connected at 0.31 seconds and the voltage is compensated at 0.32 seconds. The steady state error is as low as 0.08V.

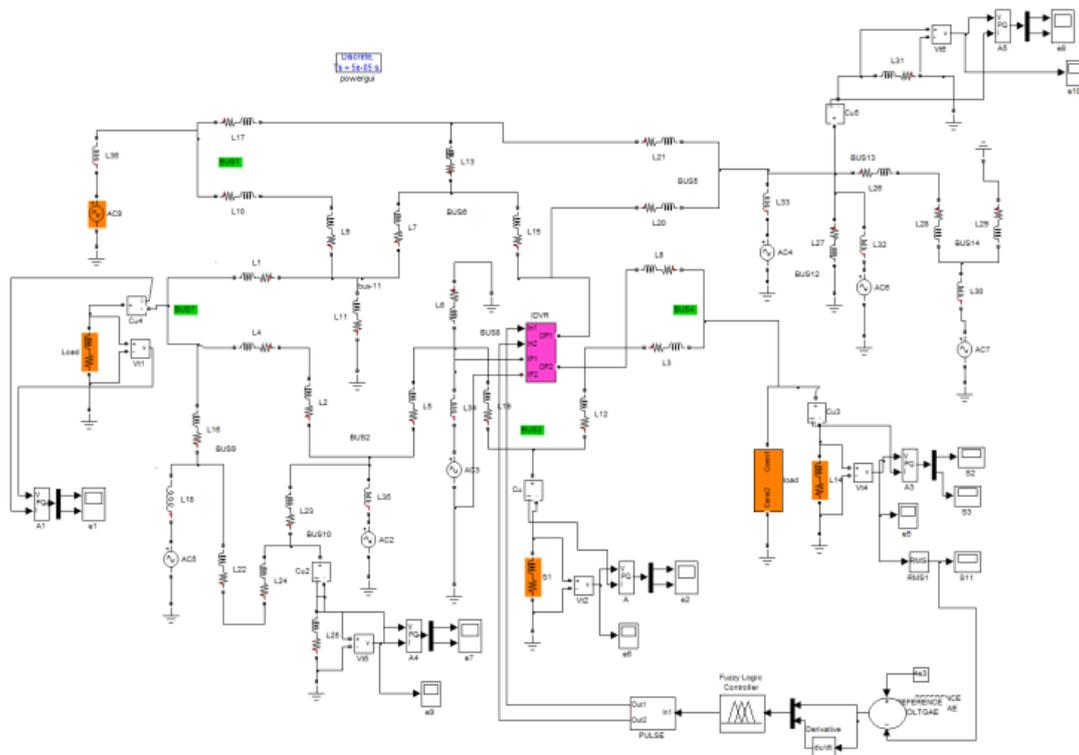


Figure 31. Simulink model for Fourteen Bus IDVR system with FL Controller

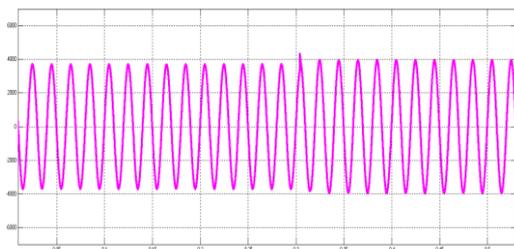


Figure 32. Output voltage waveform of fourteen bus IDVR with FL controller

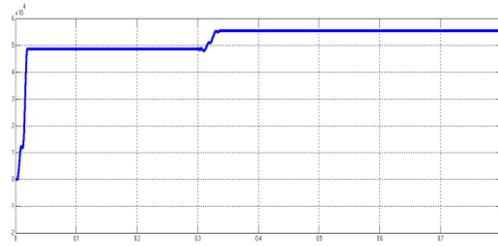


Figure 34. Real power waveform of fourteen bus IDVR with FL controller

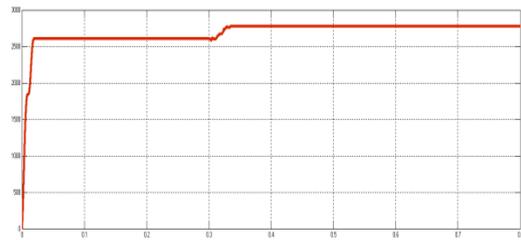


Figure 33. RMS Voltage waveform of fourteen bus IDVR with FL controller.

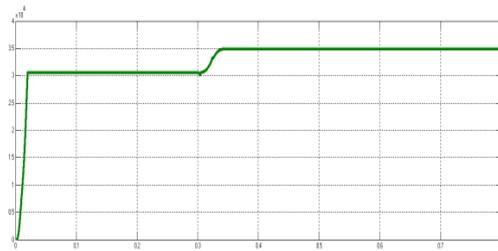


Figure 35. Reactive power waveform of fourteen bus IDVDFC with FL controller.

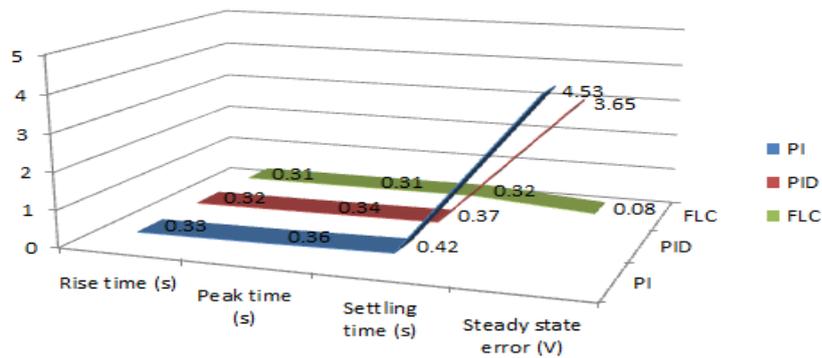


Chart 2. Closed loop time response

**5. Experimental Results**

The hardware model of four bus system with interline dynamic voltage restorer and is shown in Figure 36.



Figure 36. Hardware Setup Four Bus System with IDVR

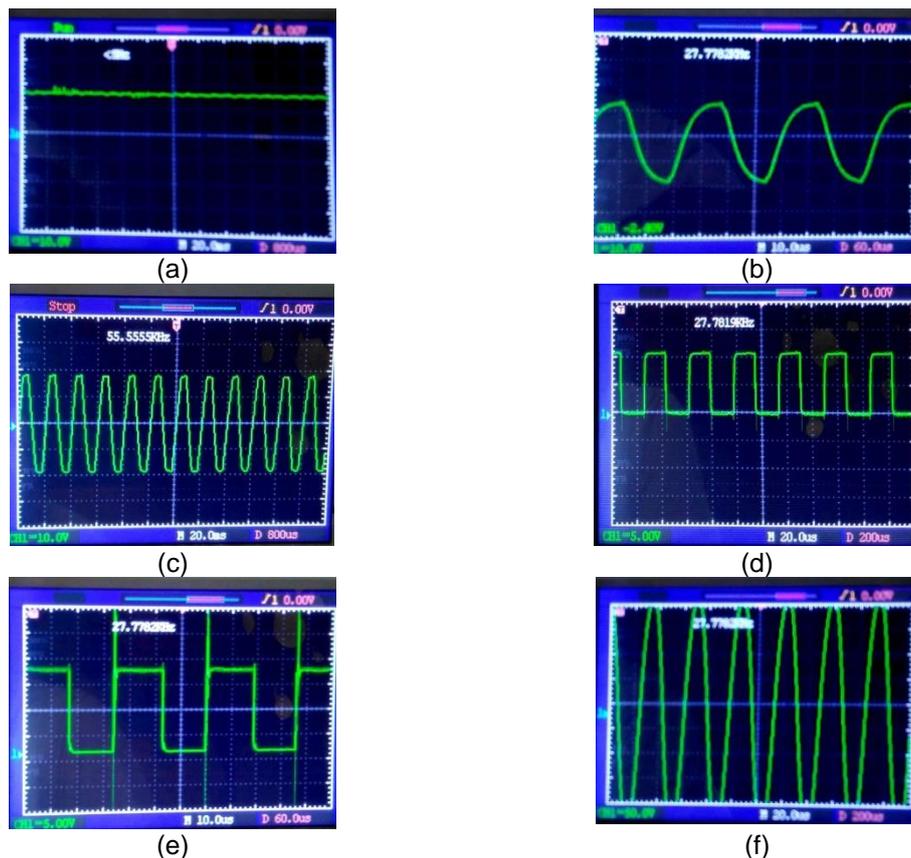


Figure 37. (a)Capacitor Voltage (b) Rectifier Voltage (c) Sag occurs in Load 1 (d) Pulse for Control Circuit 1 (e) Pulse for Control Circuit 2 (f) Voltage Sag compensation voltage in load 1

## 6. Conclusion

The results of fourteen bus system with and without IDVR are modelled and simulated. FBS with line outage and inclusion of IDVR is also simulated. The change in voltage during line outage is only 0.3KV by including IDVR. The changes in real power and reactive power are 0.03MW and 0.003 MVAR respectively. The closed loop controlled compensation in fourteen bus system was achieved using PI, PID and FLC controllers. The comparison of the responses indicates that the FLC produces better dynamic response than PI and PID controlled systems. The steady state error of fourteen bus system with FLC controller is 56% less in comparison to proportional integrated controller. The prototype model for four bus system with IDVR is modelled and results are obtained and compared with simulation results. The FBS with proposed IDVR has benefits like improved voltage profile and power transfer ability. The disadvantage of IDVR is that it requires six IGBTs.

The scope of the present work is to study the power quality improvement in fourteen bus system with IDVR. The power quality improvement in thirty three bus system will be investigated in future

## References

- [1] A Ghosh, G. Ledwich. Compensation of distribution system voltage using DVR. *IEEE Trans. Power Del.* 2002; 17(4): 1030–1036.
- [2] SS Choi, BH Li, DM Vilathgamuwa. Dynamic voltage restoration with minimum energy injection. *IEEE Trans. Power Syst.*, 2000; 15(1): 51–57.
- [3] L Gyugyi, KK Sen, CD Schauder. The interline power flow controller concept: A new approach to power flow management in transmission system. *IEEE Trans. Power Del.* 1999; 14(3): 1115–1123.
- [4] JG Niesen, F Blaabjerg, N. Mohan. Control strategies for dynamic voltage restorer compensating voltage sags with phase jump. *Proc. 16<sup>th</sup> Annu. IEEE APEC*, 2001; 2: 1267–1273.

- [5] M Vilathgamuwa, AADR Perera, SS Choi. Performance improvement of the dynamic voltage restorer with closed-loop load voltage and current-mode control. *IEEE Trans. Power Electron.* 2002; 17(5) 824–834.
- [6] Ramya, G, V Ganapathy. Comparison of Five Level and Seven Level Inverter Based Static Compensator System. *Indonesian Journal of Electrical Engineering and Computer Science* 3.3 (2016): 706-713.
- [7] Ramya, G, V Ganapathy, P Suresh. Power Quality Improvement Using Multi-Level Inverter Based DVR and DSTATCOM Using Neuro-Fuzzy Controller. *International Journal of Power Electronics and Drive Systems (IJPEDS)* 8.1 (2017): 316-324.
- [8] Suresh, P, B Baskaran. Voltage Sag Compensation in Multiline Distribution System using Closed Loop Controlled IDVR. *International Journal of Applied Engineering Research* 12.8 (2017): 1576-1583.
- [9] Suresh, P, B Baskaran. Reduction of Line Losses by using Interline Dynamic Voltage Restorer. *International Journal of Control Theory and Application.* 2016; 9(25): 417-422
- [10] Elhaj, Nabil, M Brahim Sedra, Hind Djeghloud. DFPI-based Control of the DC-bus Voltage and the AC-side Current of a Shunt Active Power Filter. *Bulletin of Electrical Engineering and Informatics* 5.4 (2016): 430-441.
- [11] Prasad, Miska, Ashok Kumar Akella. Performance Evaluation of Three Different Inverter Configurations of DVR for Mitigation of Voltage Events. *Indonesian Journal of Electrical Engineering and Informatics (IJEI)* 4.4 (2016): 225-239.
- [12] Suresh, P, B Baskaran. Power Quality Improvement of Nine Bus System during Line Interruption Using IVDFC. *International Journal of Applied Engineering Research* 12.10 (2017): 2527-2537.
- [13] a, Suresh, Baskaran b, and Ramya c. Performance Evaluation Of Custom Power Devices To Mitigate Voltage Sag In Power Distribution Network. *International Journal of Advanced Research* 5, no. 4 (April 30, 2017): 725–734. doi:10.21474/ijar01/388
- [14] Suresh, P, B Baskaran, G Ramya. Fuzzy Logic Controller Based IDVR in IEEE 30 Bus System for Voltage Sag Compensation. *Indian Journal of Science and Technology* 10.29 (2017).

## APPENDIX

### Simulation parameters

Bus no	Voltage	Load Impedance	
		Resistance	Impedance
1	6350	-	-
2	-	8Ω	23mH
3	-	5Ω	14mH
4	-	9Ω	9mH
5	6350	-	-
6	-	10Ω	40mH
7	-	18Ω	25mH
8	6350	-	-
9	-	45Ω	55mH
10	-	33Ω	65mH
11	6350	-	-
12	-	62Ω	42mH
13	-	45Ω	59mH
14	6350	5Ω	-

Buses	Line Impedance	
	Resistance	Inductance
1-2	5Ω	22mH
2-3	3 Ω	15mH
3-4	13Ω	8mH
4-5	15Ω	26mH
5-6	25Ω	32mH
6-11	10Ω	22mH
6-12	26Ω	17mH
12-13	45Ω	32mH
13-14	35Ω	28mH
14-9	43Ω	11mH
11-7	90Ω	36mH