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Neoteric Hybrid Multilevel Cascade Inverter Based on Low Switch Numbers Along with Low Voltage Stress: Design, Analysis, Verification

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Abstract

With the purpose of rein in the high voltage of flexible power systems, renovation and amendment of multi-level structures aimed at acquisition of high quality voltage is certainly required. In this regard, robust topology must be occupied that encompass the maximum output voltage levels along with minimum of switch number, of course, with taking into account of Peak Inverse Voltage (PIV). In this paper, a neoteric high-performance multilevel cascaded inverter is suggested up to the problem of repetitive output levels to be unraveled and also number of output voltage levels to be maximized. It has been constructed by series-connected multilevel inverters blocks and three-level inverter. The simulation results along with experimental results extracted by manufactured prototype have transparently approved high efficiency of proposed inverter as well as its feasibility. Apart from above, new mathematical approach has been presented to calculate and define the DC voltage sources magnitudes in asymmetric converter.

Keywords*: multilevel inverter, asymmetrical inverter, PV-Battery, voltage stress*

1. Introduction

Of late years, many various multilevel inverter structures have been suggested that lead to application of them in different parts of power system. To be noted that, the most prominent topologies are based on these structures: diode clamped, flying capacitor, and cascaded H-bridge that all have pursued high-quality outputvoltage (low distortion and low dv/dt), lows witching frequency, and low voltage semiconductors [1-3]. An overwhelming majority of them, the topologies based on cascaded H-bridge power cells which are constructed by series connection of several inverters are of interests for scholars.

In general, the multilevel structures have been categorized in two so-called symmetric and asymmetric inverters. The symmetric inverters encompass equal DC voltage sin the event that the asymmetric types include different DC voltage ratios. Despite the advantage of high-quality voltage acquisition, the multilevel inverters horn Ina great number of semiconductor switches, or in other words, cost price up [4-6]. In these structures, to obtain ahigh quality voltage, the increasing number of switches (components) isn't avoidable. This issue creates a drastic stimulus in scholars which this field to be more evaluatedand scrutinized insofar as number of switches to be reduced. It is worth mentioning that the asymmetric inverters can provide high-quality voltage along with low harmonic content so that total number of switches is less that the symmetric topologies.

In this regard, several literatures have reported various suggestions and inventions of new topologies based on cascaded multilevel inverter [4-12]. With considering more precise details [5-6], Banaei proposed a hybrid topologies based on a mixture of cascaded basic modules with one H-bridge module, and as well asemploying different algorithms to calculate and define the DC voltage sources magnitudes of symmetric and asymmetric inverters [7], Ajami has presented new symmetrical and asymmetrical topologies to minimize the number of total embedded switches and their voltage stress. Also, the suggested multilevel inverter in [8] has been made up a series and parallel connections of DC voltage sources by Hinago. A new multilevel converter topology with fewer power electronic switches is introduced in [9] by Gupta [9] 15-level inverter with asymmetric sourceconfiguration has been proposed to attain minimum number of switches (ten switches) and conduction losses [10], Chattopadhyay has

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manufactured a symmetric cascaded inverter with a level doubling network to enhance the power quality, decrease the switching frequency, and also minimize the cost and size of the power filter [11], Banaei has investigated lower total Peak Inverse Voltage (PIV) via presentation of two multilevel inverters (symmetric and asymmetric inverters) which have been constructed by connections of cell unit hierarchy with six power switches [12], Babaei has presented 39-level multilevel inverter constructed by 20 IGBTs which is on basis of two inverter legs in series for each cell [13], Laali has suggested a new basic multilevel cascaded inverter (49-level inverter) that is based on the series connection of new type of inverter i.e. mixture of bidirectional and unidirectional switches.

Considering the outstanding features all kinds of aforementioned multilevel inverters, the developed structure suggested in this paper has conquered them. In fact, it can be resolutely identified as a robust neoteric hybrid multilevel cascade inverter that the switch numbers are significantly less than number of embedded switches in other above mentioned inverters. In order to clarify and certify the high performance of the proposed inverters, computer-aided simulations have been carried out using MATLAB/SIMULINK. Meantime, the experimental case in laboratory scale has transparently corroborated the feasibility of this inverter.

2. Suggested Topology

The suggested circuit topologies can provide a high-quality AC voltage without increasing the number of switches and DC voltage sources, and accordingly two methods are proposed DC voltage sources magnitudes. As mentioned before, approximately all scholars who have researched and worked in this field of study have pursued high-quality voltage acquisition considering low embedded switch numbers in their structures.

The suggested hybrid topology is constructed by two inverter structures i.e. compound of three-level inverter with developed cascaded H-bridge inverter that Figure 1 depicts the its power circuit. In fact, each phase in the proposed topology consists of series-connected developed cascaded H-bridge and three-level inverter. Regarding to a required levels number of output voltage, number of DC sources and switches will be calculated and figured out.

According to Figure 1, the output voltage of the multilevel inverter can be presented by:

$$V_{Ag} = V_{A1} + V_{A2} + ... + V_{An} \quad (1)$$

Where *n* is number of DC source. The substantial number of voltage levels will depend on the DC source values. Two DC source configurations and corresponding number of voltage levels are subsequently expressed. Here of, the first method points to symmetric module.

a) 'Symmetric' structure is constructed by equal DC voltage sources, i.e.:

$$V_1^{'} = V_1 = V_2 = ... = V_k = E \quad (2)$$

Accordingly, maximum output voltage V_{Agmax} for symmetric algorithm will be:

$$V_{Ag\max} = \frac{(2n-1)E}{2} \qquad n \geq 2 \quad (3)$$

And also, levels number of output voltage (*m*):

$$m = 4n - 1 \qquad n \geq 2 \quad (4)$$

In symmetric structure, three bidirectional switches in three-level inverter part can be removed from circuit of inverter. The number of switches per inverter leg (sw) is:

$$sw = 5n - 3 \qquad n \geq 2 \quad (5)$$

The levels number in phase voltage with respect to the embedded switch numbers can be calculated:

$$m = \frac{4sw+7}{5} \tag{6}$$

The number of DC voltage sources (N_{dc}) in three-phase system with respect to the levels in phase voltage can be expressed by:

$$N_{dc} = \frac{3m-5}{4} \tag{7}$$

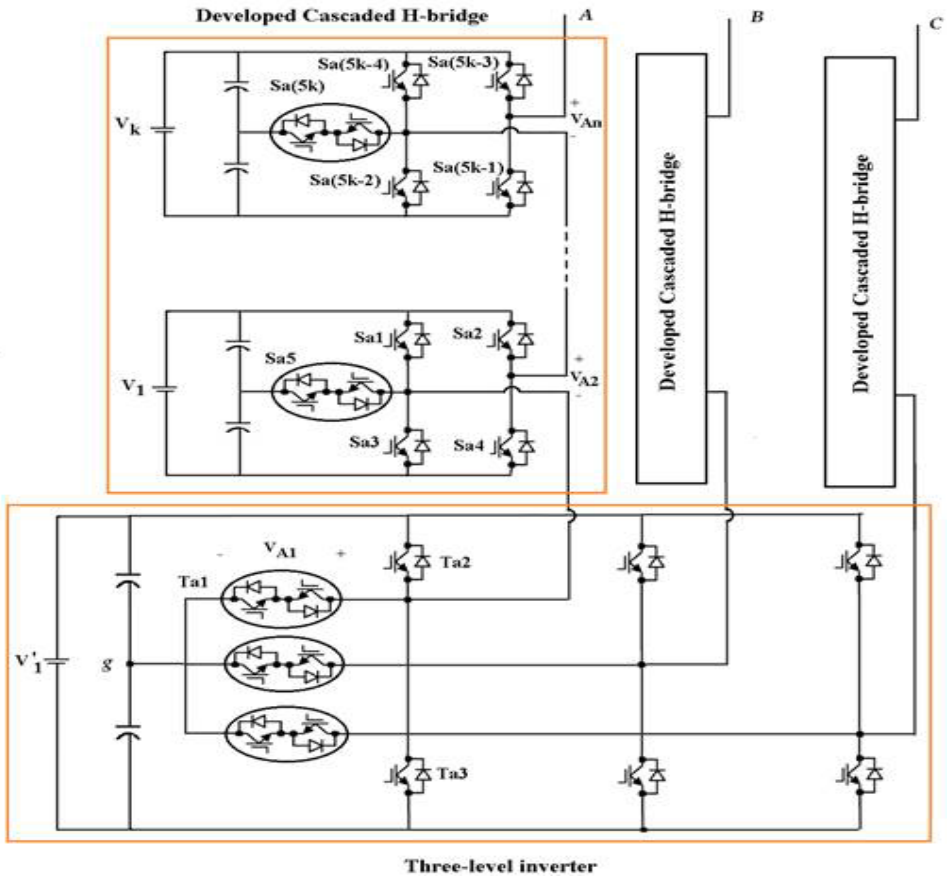


Figure 1. Circuit of the suggested multilevel inverter

b) Asymmetric' structure is constructed by unequal DC voltage sources:

$$V_1^{'} = E$$

$$V_i = (3*5^{i-1})E \qquad i = 1,2,...,k \tag{8}$$

The maximum output voltage is calculated as:

$$V_{Ag\max} = \frac{(3*5^{n-1}-1)E}{4} \qquad n \geq 2 \tag{9}$$

The number of steps *m* (voltage levels) in phase with respect to the number of the used basic units can be calculated as:

$$m = 3*5^{n-1} \tag{12}$$

The switches with high-voltage capability (high withstand voltage) have higher price as compared with low-voltage capacity. It must be noted that, the semiconductor switches in proposed topology endure low voltage stress i.e. lower cost price than other types. In the proposed hybrid structure, voltage stresses of switches (VS) arecomputed as follows:

$$VS_{Ta1} = \frac{V_1^{'}}{2} \tag{13}$$

$$VS_{Ta2} = VS_{Ta3} = V_1^{'} \tag{14}$$

$$VS_{Sa(5i)} = \frac{V_i}{2} \qquad i = 1,2,...,k \tag{15}$$

$$VS_{Sa(5i-1)} = VS_{Sa(5i-2)} = VS_{Sa(5i-3)} = VS_{Sa(5i-4)} = V_i \tag{16}$$

It is worth mentioning that, this topology can be taken into account numerous DC supplies, especially whenever higher levels number of output voltage to be required, and even it is the likelihood to substitute the DC sources with renewable energy such as photovoltaic or fuel cell.

Grid and load-connected photovoltaic (PV) systems are a common and good proven due to their portions to renewable energy generation. The sight of PV systems is to elicit the maximum power from PV arrays and exalting the efficiency.

3. Comparision Study

Here to fore, many different topologies have been suggested to acquire high levels number of output voltage along with low number of embedded switches provided thepower switches do not endure high voltage stress.In this regard, Refs [5-7, 11, 13] have justly presented novel and good structures.This part of study in order to provide an equitable judgment, advantages and disadvantages of our hybrid inverterhas been dealt with and compared alongside of the state of the art multilevel inverter topologies presented in [5-7, 11, 13]. Ref. [5] and [13] has done a comparison study among proposed inverter with an H-bridge cascaded multilevel inverter. Brief descriptive statement of selected topologies is shown in Table 1. Figure 2 shows levels number of output voltage in terms of number of utilized switches in suggested hybrid topology and presented topologies in Ref. [5-6, 11, 13]. As can be seen from Figure 2, the suggested hybrid topology provides higher voltage levels as compared with presented topologies in [5-6, 11, 13].

It must be noted that, our suggested topology and presented topology in [13] use bidirectional switches in their structures. The bidirectional switches have higher price than unidirectional switches. Figure 3 shows levels number of output voltage in terms of number of utilized IGBTs in suggested hybrid topology and presented topologies in [5-6, 11, 13].

Table 1. Descriptive Statement of Selected Topologies

	[5, 6]	[11]	[13]	Proposed
Voltage levels asymmetric state	$2^{n+1}-1$	$2^{n+1}-1$	$7^{\frac{n}{2}}$	$3*5^{n-1}$
Voltage levels symmetric state	$2n+1$	$2n+1$	$2n+1$	$4n-1$
No. of switches	$2n+4$	$2n+4$	$3n$	$5n-2$
No. of IGBT	$2n+4$	$2n+4$	$4n$	$6n-2$
No. of DC-link capacitors	-	-	-	$2n$

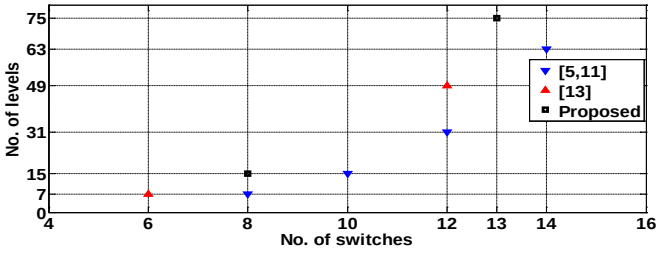


Figure 2. Levels number of output voltage in terms of number of utilized switches

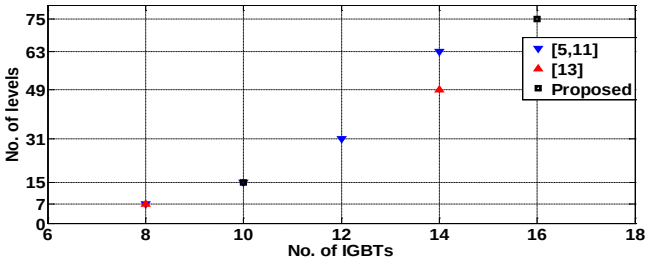


Figure 3. Levels number of output voltage in terms of number of utilized IGBTs

Apart from above mentioned inspected targets, the rate of voltage and current of the semiconductor switches has played an important and key role in cost price of inverter. Imagine! The presented converters in [5], [11] and [13] have twelve switches in one phase that output voltage of all converters is equal. What is more important here is that our suggested converter has been constructed by thirteen switches. The presented structures in [5], [11] and [13] (Figure 4) have been made up by twelve switches which produce output phase voltage of 15E.

The switches'PIV of presented converter in [5] is attained by:

$$PIV == \sum_{i=1}^{K} Vsw,i \tag{17}$$

Where, K and Vsw,i are the number of switches and PIV of switches, respectively. Table 2 shows number of voltage levels and type of switches in terms of voltage stress. Note that, he values of Table 2 have been given for three-phase system. In accordance with Table 2, it is obvious that the suggestedstructure has been constructed by switches with lower voltage stress while generates higher voltage levels as compared with others.

Table 2 has transparently indicated that the standing voltage on switches in the suggested topology is significantly less than the presented topologies in [5] and [11]. Although the presented topologies in [5] and [11] have low number of switches in comparison with CHB multilevel inverter but some switches in these topologies have high voltage stress in the event that the our suggested inverter and presented topology in [13] are cascaded structures.

Table 2. Comparison Study

	[5]		[11]		[13]		Proposed	
Levels	31		31		49		75	
DC source	12		12		12		7	
	voltage	number	voltage	number	voltage	number	voltage	Number
Switches Type in terms of voltage stress	E	6	E	6			0.416E	3
	2E	6	2E	6	1.25E	6	0.81E	6
	4E	6	4E	6	1.875E	12	1.216E	3
	8E	6	7E	6	8.75E	6	2.43E	12
	15E	12	15E	6	13.125E	12	6.08E	3
							12.16E	12
PIV	300E		222E		240E		203.058E	

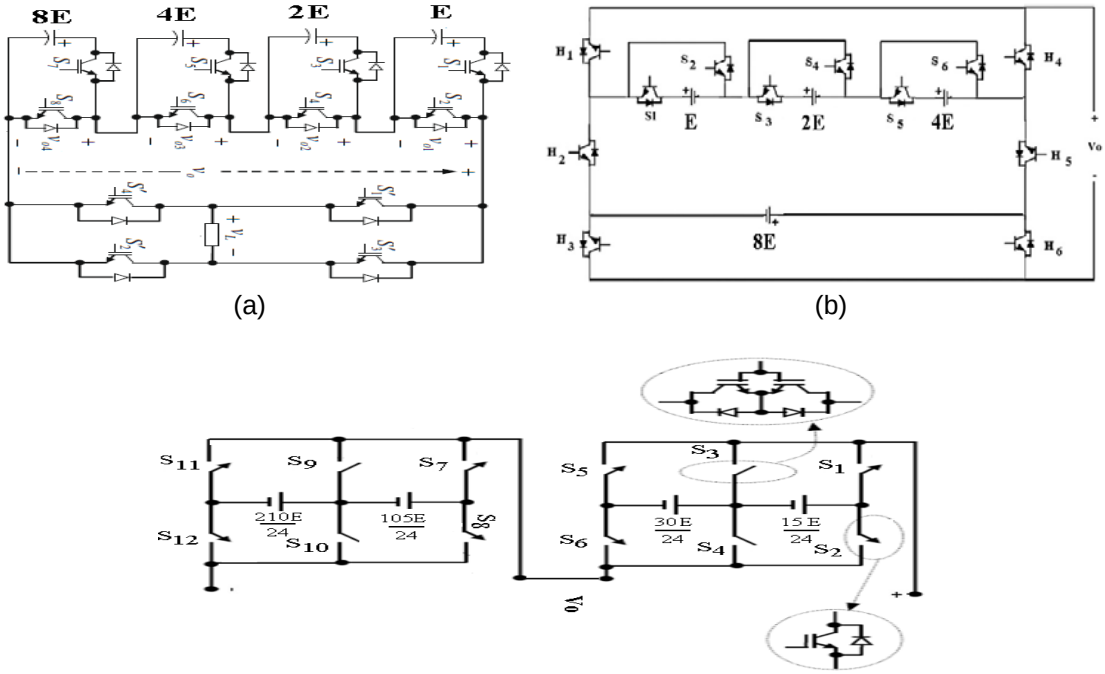


Figure 4. Circuits of [5], [11] and [13] (a) [5], (b) [11] and [13]

4. Operation of Suggested inverter

In order to test and analyze the performance of the suggested hybrid inverter, typical 15-level inverter topology shown in Figure 1 has been simulated by using MATLAB/SIMULINK. In circuit of 15-level inverters shown in Figure 6, the first and the second unit are fed with E and 3E, respectively. While the DC value is taken E=40 V and also the output frequency simulation is 50 Hz.

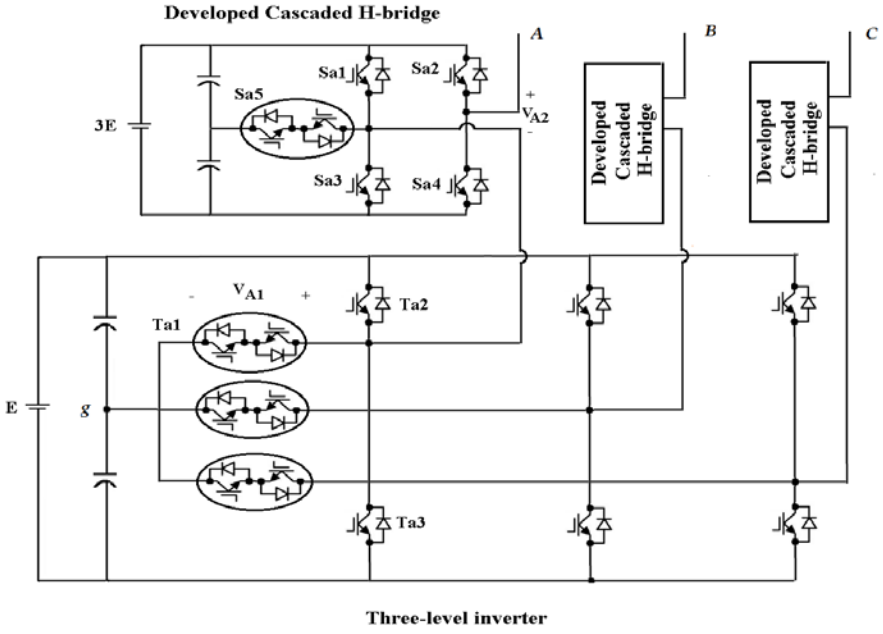


Figure 6. Circuit of suggested 15-level inverter

Operation of multilevel inverters depends on modulation strategy that various modulation strategies exist. In this paper, the fundamental frequency switching method has been used [14-18]. Table 3 shows the ON switches look-up table which is presented for phase A.

Switching of other phases will be alike, with the exception that to obtain the gate pulses for the switches in phases B and C, the shifted gate pulses signal of 120° and 240° must be taken into account, respectively. As shown in Table 3, in the proposed15-level topology, to provide any voltage level in the output, three switches must conduct in each phase. As can be seen, Figure 7 depicts the phase output voltages (V_{ph}) with fifteen levels.

5. Experimental Results

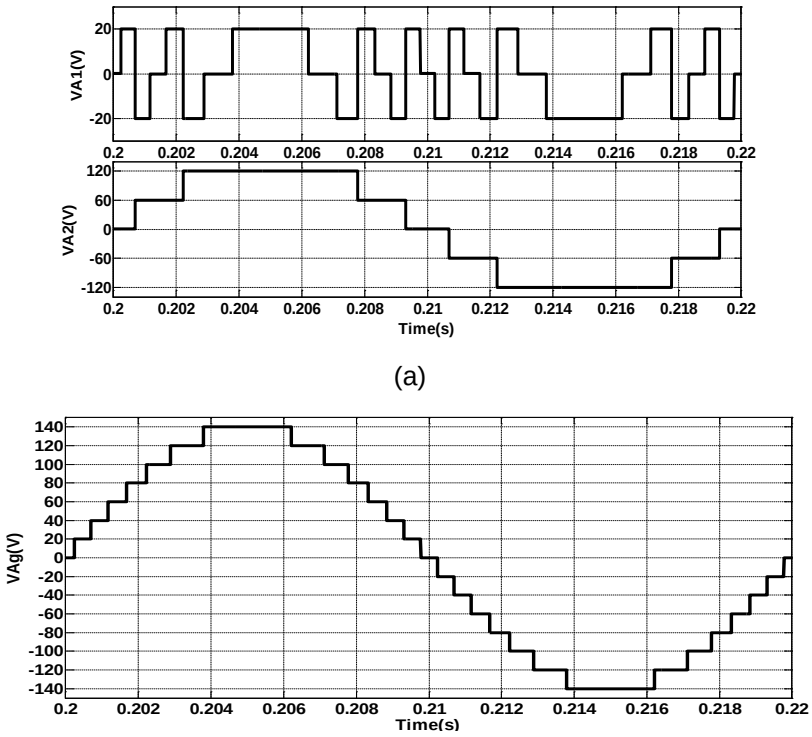
To deal with and analyze the operation of the suggested topology, a topology based on Figure 4 is engaged for this study. As mentioned in prior part, the parameters of experimental results are same the simulation results. For this topology, examinations have been executed on the R–L load while R=30 Ω and L=36mH with the frequency of 50 Hz for output voltage. Resistance of inductor in load is 10 Ω.

The prototype inverter has been manufactured using TLP250 as the IGBT driver, BUP403s as switching devices with internal anti-parallel diodes. The bidirectional switches consists of two IGBTs. The maximum phase-to-ground output voltage will be 140 V. The look-up table of switching is like to Table 3.

The operation of one phase of suggested inverteris depicted in Figure. 8. Note that, the output voltage is sum of VA1 and VA2 voltages. The phase-to-ground output voltage (VAg) is shown in Figure 8(c). It is clear that the staircase wave shown in Figure 8 has fifteen voltage levels. The voltage of resistant part of the load is shown in Figure 8(c). This wave shows current.

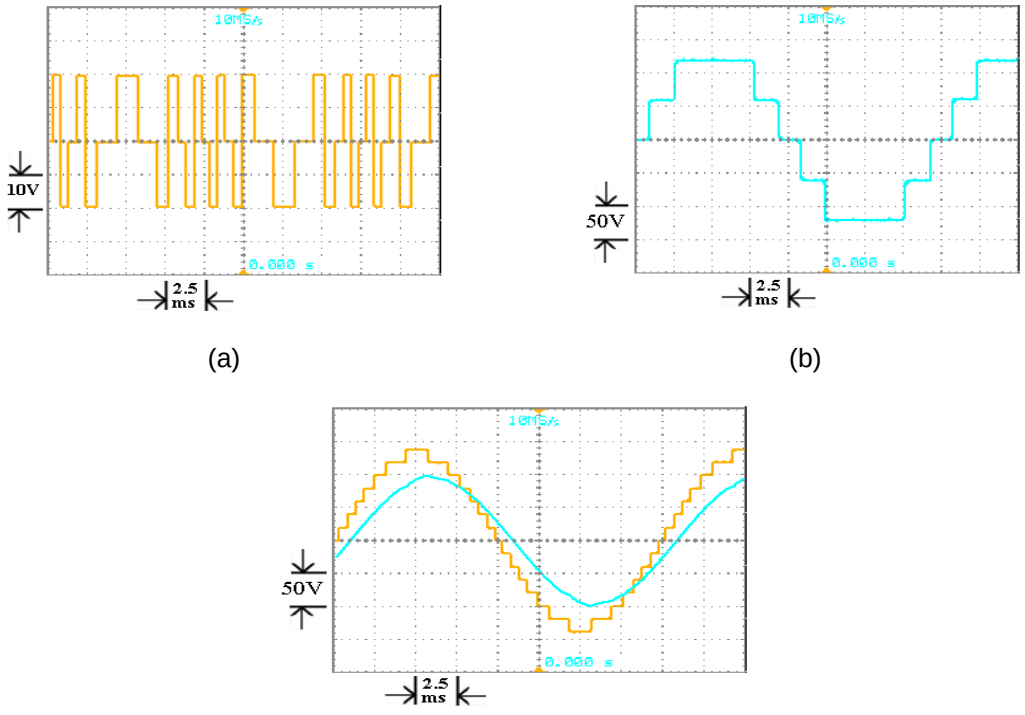
Table 3. ON Switches Look-up Table

State	T_{a1}	T_{a2}	T_{a3}	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	V_{Ag}
1	off	on	off	off	on	on	off	Off	$\frac{7E}{2}$
2	on	off	off	off	on	on	off	Off	$\frac{6E}{2}$
3	off	off	on	off	on	on	off	Off	$\frac{5E}{2}$
4	off	on	off	off	on	off	off	On	$\frac{4E}{2}$
5	on	off	off	off	on	off	off	On	$\frac{3E}{2}$
6	off	off	on	off	on	off	off	On	$\frac{2E}{2}$
7	off	on	off	on	on	off	off	Off	$\frac{E}{2}$
8	on	off	off	on	on	off	off	Off	0
9	off	off	on	off	off	on	on	Off	$\frac{-E}{2}$
10	off	on	off	off	off	off	on	On	$\frac{-2E}{2}$
11	on	off	off	off	off	off	on	On	$\frac{-3E}{2}$
12	off	off	on	off	off	off	on	On	$\frac{-4E}{2}$
13	off	on	off	on	off	off	on	Off	$\frac{-5E}{2}$
14	on	off	off	on	off	off	on	Off	$\frac{-6E}{2}$
15	off	off	on	on	off	off	on	Off	$\frac{-7E}{2}$



(a)

Figure 7. (a) VA1 and VA2, (b) phase output voltages (VAg) according to operation of proposed topology



(a) (b)

(c)

Figure 8. (a) V_{A1} and V_{A2}, (b) phase output voltages (V_{Ag}) according to operation of proposed topology

5. Conclusion

In this paper, a neoteric three-phase cascaded multilevel inverter was suggested aimed at acquisition of high levels number of output voltage along with low number of embedded semiconductor switches provided the power switches do not endure high voltage stress. To clarify and certify high efficiency of suggested topology, it had been dealt with and compared with the latest presented topologies. In the interim, the computer-aided design of three-phase hybrid multilevel inverter has been carried out using MATLAB/SIMULINK. To sum up, both the simulation and lab prototype results have transparently corroborated all aforementioned targets as well as its feasibility.

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