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Layout Effects on High Frequency and Noise Parameters in MOSFETs

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Abstract

This study reviews related studies on the impact of the layout dependent effects on high frequency and RF noise parameter performances, carried out over the past decade. It specifically focuses on the doughnut and multi- finger layouts. The doughnut style involves the polygonal and the 4- sided techniques, while the multi-finger involving the narrow-oxide diffusion (OD) and multi-OD. The polygonal versus 4-sided doughnut and the narrow-OD with multi-fingers versus multi-OD with multi- fingers are reviewed in this study. The high frequency parameters, which are of concern in this study, are the cut- off frequency (f_T) and the maximum frequency (f_{MAX}), whereas the noise parameters involved are noise resistance (R_N) and the minimum noise figure (NF_{min}). In addition, MOSFET parameters, which are affected by the layout style that in turn may contribute to the changes in these high frequency, and noise parameters are also detailed. Such parameters include transconductance (G_m); gate resistance (R_g); effective mobility (μ_{eff}); and parasitic capacitances (c_{gg} and c_{gd}). Investigation by others has revealed that the polygonal doughnut may have a larger total area in comparison with the 4- sided doughnut. It is also found by means of this review that the multi-finger layout style with narrow-OD and high number of fingers may have the best performance in f_T and f_{MAX}, owing partly to the improvement in G_m, μ_{eff}, c_{gg}, c_{gd} and low frequency noise (LFN). A multi-OD with a lower number of fingers may lead to a lower performance in f_T due to a lower G_m. Upon comparing the doughnut and the multi-finger layout styles, the doughnuts appeared to perform better than a standard multi-finger layout for f_T, f_{MAX}, G_m and μ_{eff} but are poorer in terms of LFN. It can then be concluded that the narrow-OD multi-finger may cause the increase of c_{gg} as the transistor becomes narrower, whereas a multi-OD multi-finger may have high R_g and therefore may lead to the increase of f_T and f_{MAX} as the transistor becomes narrower. Besides, the doughnut layout style has a higher G_m and f_T, leading to larger μ_{eff} from the elimination of shallow trench isolation (STI) stress.

***Keywords**: layout-dependent effects, high frequency parameters, RF noise parameters, doughnut layout styles, multi-finger layout styles.*

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1. Introduction

The purpose of this paper is to review the closely related studies on the layout impact on the high frequency and noise parameters of the MOSFET, carried out over the past decade. It is hypothesized that the layout style may affect the high frequency parameters (i.e., f_T and f_{MAX}) and also the noise parameters (i.e., R_N and NF_{min}) due to the impact which it may have on the parameters of the MOSFET (such as G_m, μ_{eff} and parasitic capacitances, c_{gg} and c_{gd}). This hypothesis has been developed based on the equations governing these parameters.

Upon comprehensively reviewing the literature, it was found that several layout styles have been looked into for this purpose. One such study which looked into the doughnut layout style with polygonal pattern was reported by Lopez in 2005 [5] . Five years on, Yeh et al. [3], [4], reported some insights on the determination of the effects of channel width scaling on both low and high frequency noise when shallow trench isolation (STI) stress was imposed on the multi-finger MOSFET. Besides the multi-finger, the report also included a discussion zooming in on the impact of the layout dependent stress on transistor parameters such as μ_{eff} and G_m, for a 90nm doughnut MOSFET. This impact was then compared to the impact of the standard multi-

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finger type (see Figure 1(a)). In the following year, Yeh & Guo [6], by means of their work, identified a new method which is capable of determining the impact of layout-dependent parasitic capacitances, such as the gate finger sidewall, C_{of}, and finger-end fringing capacitance, C_f(poly-end), on the inversion carrier density, Q_{inv} and μ_{eff} of a nanoscale multi-finger MOSFET.

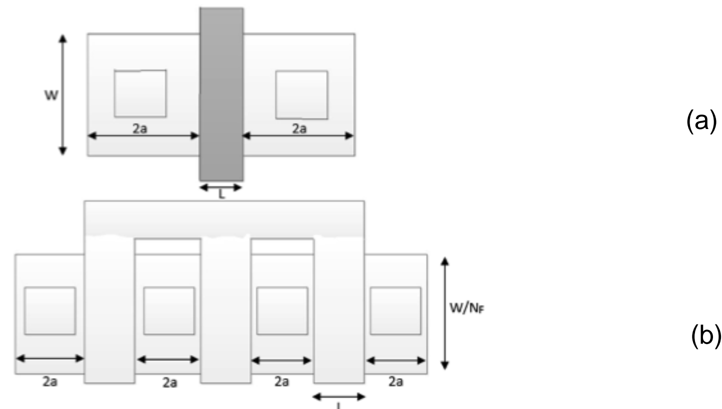


Figure 1. (a) Standard single poly-gate and (b) odd number finger layout style for MOS transistor [5]

As Yeh pursued his interest in the area, in the year of 2012 [7], he reported his work on the impact of narrow width effects on f_T, f_{MAX} and radio frequency (RF) noise in 35nm multi-finger NMOS [7]. In another research report published in the same year [8], the work described was similar to that of the former but the investigation was extended to both NMOS and PMOS. The research was to investigate the layout- dependence effects on f_T, f_{MAX}, and RF noise (i.e. NF_{min}) and noise resistance (R_N)) in sub-40nm multi-finger MOSFETs.

In the year of 2013 [9], [10], another member in Yeh's group, Ku published a study on the impact of layout dependent stress on the gate capacitance, c_{gg}, and gate resistance, R_g, subsequently affecting f_T, f_{MAX}, NF_{min}, R_N and optimum admittance ($Re(Y_{opt})$ and $|Im(Y_{opt})|$)) performances in multi-finger and doughnut MOSFETs [9]. This study can be considered as an extension of another study carried out in the year of 2010 which only focused on the impact of the layout dependent stress on G_m, μ_{eff} and LFN. In addition, another related study was published in the same year following up the work of the former which was conducted on both sub-40nm PMOS and NMOS between standard multi-finger and narrow-OD layout style [10].

2. Research Method

In this section, a brief study on different layout styles, which are multi-finger and doughnut layout.

2.1. An Investigation Into the Impact of Multi-Finger Layout

The aggressive scaling of CMOS technology being incorporated into the nanoscale has made the studies on the layout stress impact on CMOS performances an important focus. The impact of channel-width scaling on f_T and f_{MAX} performances in multi-finger MOSFETs has extensively been studied by Yeh and his research team [7]–[11].

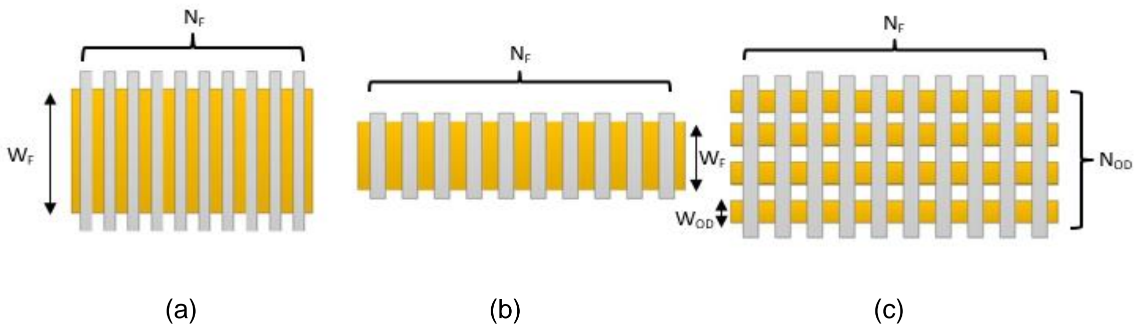
Referring to Figure 1, the equations which deal with the total area of the standard transistor and the total area of the transistor with fingers, with the transistor width, channel length, number of fingers and distance between center of contact and the edge of the gate are as follows [5]:

$$A_{Finger}= \frac{W}{N_F} ((N_F+1)2a+LN_F) \quad (1)$$

$$A_{standard} =W(4a+L) \quad (2)$$

where A_{Finger} and $A_{standard}$ are the total area of the multi-finger and standard MOSFETs, respectively, a is the distance between center of contact and the edge of the gate, L is the length of polygate, and W is the width of the layout (W = W1 + W2 + W3).

Multi-finger MOSFETs have widely been used to reduce R_g. In this regard, Yeh [3] implemented narrow-OD and multi-OD which were derived from a standard multi-finger transistor (see Figure 2(a)). Fixed was L at 90 nm and total channel-width (W_{tot}) at 32 μm.



(a) (b) (c)

Figure 2. Layout of multi-finger MOSFETs (a) standard, (b) narrow-OD, (c) multi-OD[3].

Figures 2(a)-(c) indicate the layouts for standard, narrow-OD, and multi- OD transistors respectively, where W_F is the finger width, N_F is the number of fingers, W_{OD} is the OD width and N_{OD} is the OD finger number.

In the study carried out by Yeh [3], the standard multi-finger as can be seen in Figure 2 (a) has a fixed finger width, W_F, of 2 μm and an N_F of 16. Therefore, the total channel width, $W_{tot}= W_F \times N_F$ = 2 μm×16 = 32 μm. In the same study, the narrow-OD (as shown in Figure 2(b)), displayed a layout design similar to that of Wtot as can be seen in Figure 2(a), but only with a smaller W_{OD}. For the narrow-OD designs, two layouts with $W_F \times N_F$ = 1μm×32 and 0.5μm×64 were administered. Finally, for the multi-OD as shown in Figure 2(c), Yeh [3] constructed three designs i.e., N_F and W_F were fixed at 16 and 2μm, respectively while the variations of OD width observed for W_{OD}, and OD finger number, N_{OD} were $W_F = W_{OD} \times N_{OD}$ = 2μm×1, 0.25μm×8, and 0.125μm×16.

By means of using the same layout styles as shown in Figure 2, Yeh [7] continued investigating the impact of narrow-OD width effect on high frequency performance and RF noise in 35 nm multi-finger NMOS. Narrow- OD and multi-OD were meant to improve the narrow-OD width effects like STI stress, R_g, and parasitic capacitances (i.e., c_{gg} and c_{gd}), and also to assess if they had any impact on NF_{min}, G_m, f_T, f_{MAX}. The devices were fabricated in 65nm CMOS process with gate length (Lg) of 35nm and Wtot = 64 μm. Noise analysis was conducted for the frequencies level of up to 18 GHz.

Yeh and Guo, [8] further fabricated the standard multi-finger, narrow-OD and multi-OD on not just the NMOS but also on the PMOS. In earlier related studies reported in the literature, the RF noise parameter characterization was focused on the flicker noise for the NMOS. Only in the year of 2013 publications looking into the impact on high frequency noise performance from narrow-OD width transistors were observed [10]. The investigation was carried out on 65 nm NMOS and PMOS with Lg aggressively scaled to below 40nm.

2.2. Investigations on the Impact of Doughnut Layout

The doughnut layout is normally used as a ring transistor, as the corners are considered insignificant to the drain current (IDS) but it may have more effects on the gate input capacitance, Cgg [12]. In the study reported by Lopez [5], a doughnut transistor was characterized and its performance was subsequently compared with several other layout styles in terms of the speed capability and layout area. It is a known fact that the reduction of parasitic capacitance can help improve the switching speed of a transistor, and layout of a transistor affecting this capacitance. This is clearly shown in Equation 3, in which parasitic capacitance is in inverse proportion to the switching speed of a transistor [5]:

$$S = \frac{W/L}{c_{out}} \quad (3)$$

$$C_{out} = c_{db} + c_{gd} \quad (4)$$

Where S is the switching speed of transistor, C_{out} is the capacitance at the output node and W/L being the size ratio of transistor. On the other hand, c_{db} is the drain-body capacitance and c_{gd} is the gate-drain capacitance. The doughnut transistor has been known as an efficient way of reducing the parasitic capacitance; i.e., c_{db} and c_{gd}, for a high speed application while maintaining large W/L ratios at the same time.

Lopez et al. [5], focused on assessing the impact of the doughnut transistor on the high frequency parameters and noise performances. Lopez studied the doughnut layout with multi-sides polygonal shape (see Figure 3). In their study, expressions were derived for the general W/L η-sides (η is the constant of side number) regular polygonal-shape doughnut transistor for determining IDS and total layout area (refer to Equations 5 and 6), [5]:

$$\left(\frac{W}{L}\right)_{eq} = 2\eta \frac{\tan(\pi/\eta)}{\ln(W2/W1)} \quad (5)$$

$$I_{DS} = 2\eta \frac{\tan(\pi/\eta)}{\ln(W2/W1)} \frac{1}{2} \mu C_{ox} (V_{DS})^2 \quad (6)$$

$$A = \frac{1}{2} Pa \quad (7)$$

$$a = \frac{s}{2} + d \quad (8)$$

Where C_{ox} is the oxide capacitance and V_{DS} is the drain-source voltage of transistor. A is the total area, P is the perimeter of the whole layout, a is the distance between center of contact and the edge of the gate (a = X1 or X2), s is the size of contact, and d is the minimum distance between the drain contact and edge of the gate.

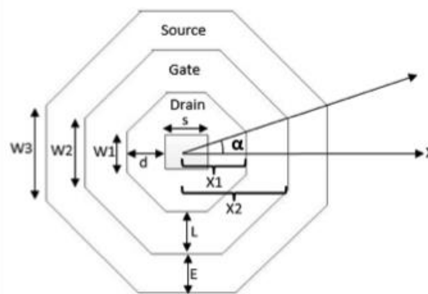


Figure 3. Polygonal-shape for doughnut layout transistor [5]

Meanwhile, the doughnut layout by Yeh [4], was for 4-side polygons with two layout dimensions that were implemented with different space between poly-gate and STI edge; i.e., SA, as shown in Figure 4. Figure 4 (a) shows that a doughnut MOSFET with space from poly-gate to STI edge follows the minimum rule, i.e. 0.3 μm (D1), and Figure 4 (b) displays a doughnut MOSFET with 10 times larger space between poly-gate and STI edge, i.e. 3 μm. It was found from the investigation [3] that the doughnut layout gave higher μ_{eff} and f_T , which may solve the potential degradation of f_{MAX} due to large c_{gg} in a doughnut layout larger than standard multi-finger (Figure 2(a)). This can be deduced from Equations (9) and (10), i.e. from the f_T and capacitances relationship and the f_{MAX} and f_T equation [7]

$$f_T = \frac{G_m}{2\pi\sqrt{(c_{gg}{}^2 - c_{gd}{}^2)}} \quad (9)$$

$$f_{MAX} = \frac{f_T}{2\sqrt{R_g(G_m+2\pi f_T c_{gd}) + g_{ds}(R_i+R_s)}} \quad (10)$$

Where R_i and R_s are the input and source resistance of the transistor and g_{ds} is the source-drain conductance. Using the same doughnut layout in Figure 4, Yeh and Guo,[8] focused on the layout-dependency stress effects, i.e. STI stress ($\sigma_\perp$ and $\sigma_\parallel$) for high frequency on the transistor's I_{DS}, G_m, μ_{eff} and f_T on the NMOS and PMOS in their work. The expression that describes the relationship between the STI stress and the mobility is given by Equations (11) and (12): [3]

$$\frac{\Delta\mu}{\mu_0} = -(\pm\kappa_\parallel\sigma_\parallel) \quad (11)$$

$$\sigma_\parallel = \kappa.\mathrm{Log}\,\frac{SA_{ref}}{SA} \quad (12)$$

where $\sigma_\parallel$ is the longitudinal stress of STI stress, $\kappa_\parallel$ is the equivalent mobility variation, μ_0 is the mobility reference, $\Delta\mu$ is the mobility variation due to STI stress, and SA_{ref} is reference of SA, which is 3 µm.

The equations above are true assuming that transverse stress, $\sigma_\perp$ is negligibly small and may be neglected. In other words, the doughnut layout is free from transverse stress effect. The study conducted was concentrated on the layout effects to G_m, μ_{eff}, f_T, and flicker noise. The NMOS and PMOS doughnut layouts had the advantage over the standard multi-finger transistor in terms of lower flicker noise and an increase in f_T. Further study on the 4-sides polygon doughnut in the aspect of its impact on R_g and RF noise parameter, NF_{min}, performance was conducted by Ku [9].

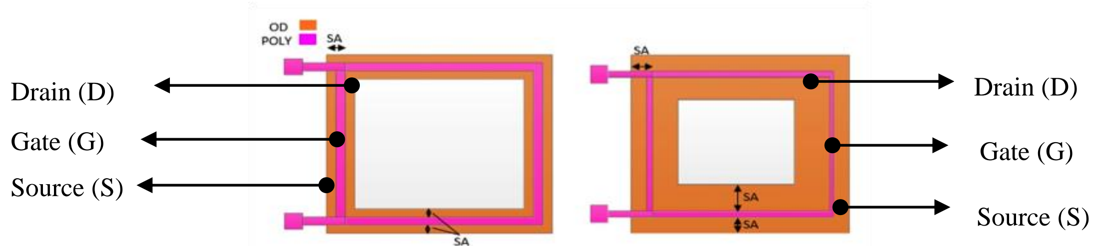


Figure 4. A simple representation of the MOSFET doughnut layout with two major layers, i.e. active region (or oxide diffusion, OD) and poly gate (POLY) (a) SA = 0.3µm, (b) SA = 3µm [3],[4]

3. Results and Analysis

In this section, explanation and comprehensive discussion are given on the results obtained from the research work conducted on multi-finger layout style.

3.1. Multi-finger Impacts

Work by Yeh from [7],[4] and [6] includes varying W_F and N_F of the narrow-OD, and varying W_{OD} and N_{OD} of the multi-OD MOSFETs, to study the effect of stress on μ_{eff}, G_m, f_T and f_{MAX}. The two designs were benchmarked against a standard multi-finger layout transistor (refer to Figure 2a). For all three layout styles, Wtot was fixed at 32 µm. When comparing with the standard layout design, it is found that when the W_F of the narrow-OD was decreased, the G_m will also decrease which consequently gave negative impact on high frequency performance, f_T (from Equation (9)). It was found that G_m degradation was caused by STI compression [3].

Another work by Yeh demonstrates c_{gg} and c_{gd} extracted using measured S-parameter with open-M1 de-embedding and the Raphael simulation [6]. This simulation precisely determines the parameters associated with the intrinsic channel and realize accurate extraction of μ_{eff} in multi-finger MOSFETs with various narrow W_F. From the narrow-OD multi-finger (refer to Figure 2b) experiments, with Wtot fixed at 32 µm while W_F and N_F varied, the narrower W_F

will result in lower I_{DS} and G_m. The G_m degradation was due to the reason stated before and the increase of C_{gg} was due to finger-end fringing capacitance. Reduction in G_m was the reason for the lowering in I_{DS}. Per Equation (9), these factors are responsible for the f_T degradation in narrow-OD devices.

The multi-OD experiments gave results which oppose the ones obtained from the narrow-OD. The experiments for the multi-OD have N_F and W_F fixed at 16 and 2μm, respectively, while W_{OD} and N_{OD} were varied. The results show that I_{DS} and G_m increase while μ_{eff} decreases when W_{OD} is reduced. A higher G_m is due to the dominance of W effect over STI, but unfortunately cannot prevent the degradation of f_T. This is because when W_{OD} becomes smaller, R_g and C_{gg} will also be higher, consequently leading to the penalty in f_T, f_{MAX} and NF_{min}. This is shown by Equations (13) to (16):[7]

$$F_{min} = 1 + 2R_N Re(Y_{opt})[1 + R_N Re(Y_{opt})] \quad (13)$$

$$NF_{min} = 10Log(F_{min}) \quad (14)$$

$$R_N = R_g + \gamma \frac{g_{d0}}{(G_m)^2} \quad \text{for } (\gamma>1) \quad (15)$$

$$R_g = \frac{Re(Y_{11})}{(Im(Y_{11})^2} \quad (16)$$

where $Re(Y_{11})$ is the real value of Y-parameter, $Im(Y_{11})$ is the imaginary value of Y-parameter, F_{min} is the minimum noise factor, g_{d0} is the gate conductance at zero V_{DS}, and $Re(Y_{opt})$ is the real value of optimum source admittance of NF_{min}.

The narrow-OD devices present low R_g, when compared to the multi-OD as multi-OD has higher stress STI than narrow-OD. However, this does not prevent it from suffering low f_T and high NF_{min}. This is because the narrow-OD has large C_{gg} which will cause f_T to degrade (shown by equation (9)) and when combined with a low R_g cannot guarantee a lower R_N due to G_m degradation (from equation (15)).

3.1.1 Narrow-OD Multi-Finger

DC analysis was also done by Kuo Ling Yeh and his team [1-2], and I_{DS} follows the trend of G_m for narrow-OD multi- finger, while a smaller W_F leads to lower I_{DS} (per equation (18)). The decrease in W_{OD} leads to a decrease in V_T, which present an inverse narrow-width effect (INWE) that comes from an increase in STI stress process [3]:

$$G_m = W_{eff} C_{ox(inv)} \mu_{eff} \frac{V_{DS}}{L_{eff}} \quad (17)$$

$$I_{DS} = G_m(V_{GS} - V_T - \lambda V_{DS}) \quad (18)$$

Where W_{eff} is the effective channel width, $C_{ox(inv)}$ is the equivalent oxide thickness under inversion and L_{eff} is the effective channel length.

Experiments were conducted on the layout impacts on for high frequency parameters, i.e., f_T and f_{MAX}, by [7], [8], [10], [4], R_g by [7], [8], [10], [11] and c_{gg} by [8], [10]. A standard multi-finger (Figure 2(a)) at W_F = 2 μm has the highest f_T compared to when W_F decreases. The high f_T can also be related to the high G_m as shown in equation (9). The results of experiments on the device show that a standard multi-finger (Figure 2(a)) at W_F = 2 μm has the smallest c_{gg}. This explains why a standard multi-finger (Figure 2(a)) has the highest f_T since it has the highest G_m and smallest c_{gg}. Parameter f_{MAX} has the same trend as f_T, the lower f_T leads to low f_{MAX} when referring to equation (10).

For RF noise parameter performance analysis, there are two types of RF noise; high frequency noise, such as NF_{min}, R_N, $Re(Y_{opt})$ and $Im(Y_{opt})$. As for the results from the high frequency noise parameter (i.e., NF_{min}, R_N, $Re(Y_{opt})$ and $Im(Y_{opt})$) experiments conducted by [7], [8], [10], the decrease in W_F causes an increase in NF_{min} and $Re(Y_{opt})$ but decreases in R_N and $Im(Y_{opt})$. Theoretically from equations (13) – (15), a low R_g leads to lower R_N, low R_N which then leads to low F_{min} and therefore NF_{min}. But the result shows an opposite from theory which can only be explained by one reason i.e. the increase in $Re(Y_{opt})$ overcomes the reduction in R_N.

3.1.2 Multi-OD Multi Finger

The f_T and f_{MAX} NMOS of a multi-OD NMOS increases accordingly with of W_{OD}. This is because c_{gg} increases with the W_{OD} increase, causes G_m to decrease and thus affects f_T and f_{MAX} (refer to equation (9) and (10)). In addition, a DC performance analysis of the multi-OD NMOS was conducted by Yeh [11]. The trend of I_{DS}, G_m, and V_T are the same where all three increase with the increment of W_{OD}.

RF noise parameter analysis in multi-OD NMOS was also performed for high frequency noise. The investigation on the high frequency noise parameter by [7] shows that R_g and NF_{min} have trends which are the same as G_m, which is inversely proportional to R_N. While R_N of multi-OD with W_{OD} = 0.125 µm is higher than multi-OD with W_{OD} = 0.25 µm. This can be due to the decrease in $\frac{g_{do}}{{G_m}^2}$ in equation (15) which offsets the increase of R_g in a reverse correlation between R_N and R_g [10].

3.2. Doughnut Impact

In this section, explanation and comprehensive discussion are given on the results obtained from the research work conducted on doughnut layout style.

3.2.1. Impact on the Transistor Size

Lopez found that a ring layout has drain diffusion surrounded by the transistor channel and source (referring to Figure 2(b) in [12]) [5]. This style reduced transistor layout area and the values of the output parameters, here the switching speed of device. Consequently, a large W/L ratio can be realized through parallel connection of the doughnut with minimal dimension cells. A demerit of the doughnut layout is that this style has a bad effect (tendency to break) on the source diffusion when under very high power operation [5]. The solution proposed was a circle-like layout transistor, a polygonal doughnut, with as many numbers of sides as possible (shown in Figure 3). For a polygonal doughnut layout style, the drain area will decrease with the increase of the number of sides.

Besides the polygonal doughnut, Lopez performed a comparison between standard single poly-gate transistor with an odd N_F finger layout style in terms of its drain area and total area as in Figure 1. Equations (7) and (8) show the total area calculation for a general number ŋ- side of a regular doughnut layout, while equations (2) and (1) show the total area calculation of an odd number of finger layout and standard single poly-gate layout transistor, respectively.

Theoretically, for a fixed s and d of the polygonal doughnut layout, a higher number of sides (ŋ) will lower the drain area, even lower than the drain area of a standard transistor of equivalent W/L (refer to Figure 2(a)). The decrement of drain area will result in better switching speed of the transistor [13]. In Lopez's work [5], the result shows that the total layout area was bigger for the polygonal doughnut transistor regardless of the number of sides than of the standard or finger transistor. Hence, a reduced drain area does not contribute to a reduced total layout area of the whole transistor. It has been found that the polygonal doughnut transistor reduces 81% of its drain area while it increases the total layout area by less than 10% [5] when compared to the standard transistor (in Figure 1(a)). This demonstrates that a polygonal doughnut layout can reduce the drain area with only a small increase in the total layout area.

3.2.2. Impact on Transistor's Parameters

3.2.2.1 NMOS

(i) G_m and V_T

Other works on doughnut transistor layout were conducted by [9], [4], [6] for the purpose of eliminating the transverse stress from STI on NMOS and PMOS. The layouts were of the 4-side doughnut style (Figure 4). In NMOS, It was found that the G_m of the doughnut layout is degraded when the space between STI edge and poly (SA) is made smaller than of a standard multi-finger (Figure 2(a)). Doughnut with SA= 0.3 µm has 9.7% reduced G_m than the doughnut layout with SA= 3 µm, however, the latter has 7.5% higher G_m as compared to standard multi-finger (Figure 2(a)) [4]. V_T for doughnut layout with SA= 0.3 µm is larger than the V_T of the doughnut layout with SA= 3 µm, but the latter has a larger or the same V_T as that of a standard multi-finger (Figure 2(a)). I_{DS} for a standard multi-finger (Figure 2(a)) is larger than doughnut layout with SA = 0.3 µm but smaller than doughnut layout with SA = 3 µm. This is because V_T rolls of due to the narrow-width effect in doughnut layout [6].

(ii) High frequency and noise

Analysis of f_T, f_{MAX}, c_{gg} and R_g are discussed below. The performance of f_T is the same as of I_{DS} performance, where doughnut layout with SA= 0.3 µm is lower than a standard multi-finger (Figure 2(a)) and doughnut layout with SA= 3 µm is the highest. This follows the expression of equation (9), where f_T is directly proportional to G_m under a fixed c_{gg} and c_{gd}. Hence, the flow is descending with a SA= 3 µm doughnut layout, followed by standard multi-finger, and finally by the SA= 0.3 µm for f_T performance. In addition to that, f_{MAX} for a doughnut layout with SA= 0.3 µm is 4 to 6 times slower and doughnut layout with SA= 3 µm is more than 6 times slower than a standard multi-finger (Figure 2(a)). The f_{MAX} trend is not consistent with the f_T, this might be due to the influence of R_g . The R_g of the doughnut layout with SA= 3 µm is 27 times higher than doughnut layout with SA= 0.3 µm; the latter is 17 times higher than the standard multi-finger (Figure 2(a)). This is proven by equation (10), in which a high R_g will lead to lower f_{MAX}. For high frequency noise, i.e. NF_{min}, it is found that it follows the flow of R_g with according to equation (13) to (15). A high R_g will lead to higher R_N, and this eventually leads to higher NF_{min}.

3.2.2.2 PMOS

(i) G_m and V_T

On the other hand, the PMOS doughnut layout has higher G_m and μ_{eff} than the standard multi-finger MOSFETs device (Figure 2(a)). Doughnut layout with SA= 0.3 µm has 12.2% higher Gm and doughnut layout with SA= 3 µm has 7.6% higher G_m than the standard multi-finger. While doughnut layout with SA= 0.3 µm has 12.5% higher µeff and doughnut layout with SA= 3 µm increase has 6.3% higher µeff than the standard multi-finger. DC performance, i.e. V_T and I_{DS}, of PMOS doughnut layout, is similar to the performance of G_m. Doughnut layout with SA= 0.3 µm has the highest V_T and I_{DS}, followed by doughnut layout with SA= 3 µm and then standard multi-finger (Figure 2(a)).

(ii) High frequency and noise

This trend is followed by f_T, with doughnut SA= 0.3 µm having 28% higher f_T than doughnut layout with SA= 3 µm and standard multi-finger (Figure 2(a)). On the other hand, f_{MAX} has the opposite result, while standard multi-finger (Figure 2(a)) has the largest f_{MAX} followed by doughnut layout with SA= 3 µm and doughnut layout with SA= 0.3 µm.

However, according to equation (10), the increase of R_g will decrease the f_{MAX} performance of transistor. The final parameter analyzed by [9] was NF_{min}. This is one of the important key parameters of MOSFET especially in RF circuit design. NF_{min} in a PMOS doughnut layout style with SA= 3 µm is the largest, doughnut layout with SA= 0.3 µm is lower and standard multi-finger (Figure 2(a)) has the smallest NF_{min}.. Indeed, the doughnut shows significantly higher NF_{min} as compared to a standard multi-finger. It is shown that doughnut layout with SA = 3 µm has the highest NF_{min} compared with the other two layouts. The increase in R_g contributes to a larger R_N, and leads to a higher NF_{min}.

Both NMOS and PMOS may benefit from the doughnut layout; however, the layout dependence of G_m and R_g is a critical trade-off in determining high frequency parameter's performance, such as f_{MAX} and NF_{min}. This study suggests that multi-finger layout transistor remains the better choice for RF circuit designs compared to doughnut layout transistor.

4. Conclusion

The impacts of layout-dependent STI stress on high frequency (f_T and f_{MAX}) performance of multi-finger MOSFETs with various layouts, including standard, narrow-OD, and multi-OD were studied. The decrease in G_m with finger width (W_F) scaling in narrow-OD NMOS demonstrates μ_{eff} degradation from compressive STI stress along the transverse direction. In contrast, the multi-OD NMOS reveals an abnormal G_m increase for an extremely narrow OD width. Meanwhile, a polygonal doughnut layout is an efficient way to reduce parasitic capacitances for high-speed application while maintaining large W/L ratios.

From these studies, selection can be made systematically on the optimum number of sides for the doughnut layout as a trade-off between the desired W/L and the drain capacitance reduction. Also, the reduction of C_{gg} and R_g may serve as a solution for the potential degradation of f_{MAX} and NF_{min} , respectively, for RF digital and analog application. It may thus be

concluded that as transistor becomes smaller in W_F, it will lead to an increase of c_{gg} in narrow-OD. Meanwhile, a multi-OD multi-finger has a higher R_g as W_{OD} becomes smaller. Both of the mentioned consequences will lead to the increase of f_T and f_{MAX}. Other than that, doughnut layout style eliminates $\sigma_{\perp}$ stress which leads to larger μ_{eff} than a standard multi-finger. This, in return enhances, the G_m and f_T.

The results from the RF noise study shows the increased of measured NF_{min} can be due to larger C_{gg}. The lower R_g cannot guarantee lower R_N due to a competing factor from G_m degradation. The trade-off of smaller width effect on high frequency performance and RF noise provides a significant guideline for multi-finger and doughnut MOSFETs layout for RF circuits design using nanoscale CMOS technology.

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References

[1] RA Hastings. *The art of Analog Layout*, 2nd Edition ed.: Pearson Prentice Hall, 2006.
[2] TH Lee. *The Design of CMOS Radio-Frequency Integrated Circuits*: Cambridge University Press, 2004.
[3] KL Yeh, JC Guo. The Impact of Layout-Dependent STI Stress and Effective Width on Low-Frequency Noise and High-Frequency Performance in Nanoscale nMOSFETs. *IEEE Transactions on Electron Devices*. 2010; 57: 3092-3100.
[4] KL Yeh, CY Ku, JC Guo. The impact of MOSFET layout dependent stress on high frequency characteristics and flicker noise. *IEEE Radio Frequency Integrated Circuits Symposium*. 2010; 577-580.
[5] P Lopez, M Oberst, H Neubauer, J Hauer, D Cabello. Performance analysis of high-speed MOS transistors with different layout styles. *2005 IEEE International Symposium on Circuits and Systems*. 2005; 4: 3688-3691.
[6] KL Yeh, JC Guo, Layout-Dependent Stress Effect on High-Frequency Characteristics and Flicker Noise in Multifinger and Donut MOSFETs. *IEEE Transactions on Electron Devices*. 2011; 58: 3140-3146.
[7] KL Yeh, C Chih-Shiang, JC Guo. Layout-dependent effects on high frequency performance and noise of sub-40nm multi-finger n-channel and p-channel MOSFETs. *IEEE/MTT-S International Microwave Symposium Digest*. 2012: 1-3.
[8] KL Yeh, CS Chang, JC Guo. The impact of narrow width effects on high frequency performance and noise in 35nm multi-finger n-MOSFETs. *2012 IEEE Radio Frequency Integrated Circuits Symposium.* 2012: 355-358.
[9] CY Ku, KL Yeh, JC Guo. The impact of layout dependent stress and gate resistance on high frequency performance and noise in multifinger and donut MOSFETs. *2013 IEEE MTT-S International Microwave Symposium Digest (MTT)*. 2013: 1-3.
[10] KL Yeh, JC Guo. Narrow-Width Effect on High-Frequency Performance and RF Noise of Sub-40-nm Multifinger nMOSFETs and pMOSFETs. *IEEE Transactions on Electron Devices*. 2013; 60: 109-116.
[11] KL Yeh, JC Guo. A New Method for Layout-Dependent Parasitic Capacitance Analysis and Effective Mobility Extraction in Nanoscale Multifinger MOSFETs, *IEEE Transactions on Electron Devices*. 2011; 58: 2838-2846.
[12] B Razavi, KF Lee, RH Yan. Design of high-speed, low-power frequency dividers and phase-locked loops in deep submicron CMOS, *IEEE Journal of Solid-State Circuits*l. 1995; 30: 101-109.
[13] RP Jindal. Noise associated with distributed resistance of MOSFET gate structures in integrated circuits. *IEEE Transactions on Electron Devices*. 1984; 31: 1505-1509.