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# Comparative Analysis of Time and Physical Redundancy Techniques for Fault Detection

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***Abstract***

*The integration level in today's world is continuously increasing in VLSI chips. VLSI circuit verification is a major challenge in these days. Integration capacity of VLSI circuits mimics the testing complexity of circuits. There is a significant chunk of the testing cost with respect to the whole fabrication prices. Hence it is important to cut down the verification cost. Time required during testing is a main factor for the cost of a chip. This time is directly proportional to the number of testing in the circuitry. So the test set should be very small. There is one way to generate a small test set is to compact a large test set parameters. The main drawback of the compaction results on the quality of the original test set. This aspect of compaction has motivated the work present here with some methods of fault detection and avoidance techniques via redundancy logic as Time redundancy and physical redundancy.*

***Keywords****: test circuits, physical redundancy, time redundancy*



## 1. Introduction

There is a main aspect of the VLSI process is to analyse the failure i.e. the process of detecting the cause of failure of any chip. Once a chip has failed in a test, the important thing is to determine the cause of its failure as this can lead to improvement in the design of the chip and the manufacturing process. The first step in failure analysis is Fault detection in which by logical analysis we can find a list of likely defect sites or regions. Basically fault diagnosis or detection minuscule the effective testing area of the chip. Several fault categorization and positioning techniques have been propounded and they can be classified with systematic techniques. Fault categorization defines the type of fault on the fault levels in the system. There are different techniques introduced for the defect diagnosis in circuits.

In [1], redundancy methods for error diagnosis are briefly surveyed. It includes various methods like resemblance with duality expression logic, time redundancy method, Self-checking circuits and memory arrays methods etc. In [2], applications of very basic views and ideas, motivation, and methods of defect tolerance have been propounded. The topics include fault categorization, redundancy methods, reliability design, prospective of fault tolerance system and some methodologies to short out the fault tolerant challenges. RH Khade and DS Chaudhari introduce the different fault detecting methods for digital and analog integrated circuits in [3]. It includes the small test set method where fault can be detected in the minimum time. One more technique is introduced in this paper named as differential measurement technique. This technique is very helpful to catch whether the circuit is error free or not. AK. Jameil introduces a digital circuit testing simulator named as deductive fault simulator in [4]. It has a set of ten gates and three inputs and only one output that generate comparison results by simulation encryption. This simulator justifies its adequacy for fault diagnosis by meticulous results and calculations.

In [5], a very strong and adaptable testing technique for single failure named as signature analysis is proposed. This technique is very effective and beneficial because of its reappearing quality. I Koren and Z Koren Surveyed different strengthening and designing methods for fault tolerant in [6]. Hence the circuit can be more reliable against the faults and failures. In [7], the authors proposed the methods for fault detection and test reduction in combinational circuits. Here are total 11 techniques surveyed that varies from foundation to the modern fast adaptive techniques. Advantages and disadvantages of those techniques are examined here. In [8] the error is examined in MODEL SIM 6.3 simulation software here coding

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is done by VHDL programming. This software is very useful for the sequential circuits.Author proposes an error testing method named as Fault injection in [9]. It is used for the assessment of device metrics such as stability, security and fault treatment of the object system. Fault injection infuses error into the system and observes the system to examine its conducts towards faults.

## 2. Defect Detection

A planning for a circuit synthesis may be unsuccessful at the level of verifications. It will demote the class of effects and decisions. There may be origins for the failure as

a. Verification was not right.
b. The synthesis process was incorrect.
c. The circuit plan was inaccurate.
d. The requirements were improper

The function of verification is much valuable to discover whether something proceeding incorrect. On the other hand the position of diagnosis is also much essential to decide precisely what is going fallacious seeing as accuracy and usefulness of verification is very seminal for the grade of creations. Defect detection techniques are necessary for fault tolerance and the motivations behind these are

a. Rate of diagnosis
b. Treatment
c. Supply raised
d. Production elevated
e. Diagnosis granularity

VLSI chip construction trades are trimming an unceasing crushing to rising of the construction turn over. Integrated circuit fabricators are continuously troubleshooting for reduction of defective parts. A single error can make the full chip worthless thus a system chip must be trustworthy. Therefore, there is a worth of error diagnosis and fault fixing method in these days. A fabricator may be able to enhance the circuit devise or the fabrication operation by study of the parts. That study may include failure validation tests and may crack the root of failure for every single part of the circuit. There are many other useful self checking and fault detection techniques present in VLSI circuit testing world [3-4].

a. Self-checking circuit technique.
b. Monotonic logic technique.
c. Fault detection by Single bit error detection.
d. Single stuck fault detection concept for by pipelining method.
e. Path delay fault testing technique.

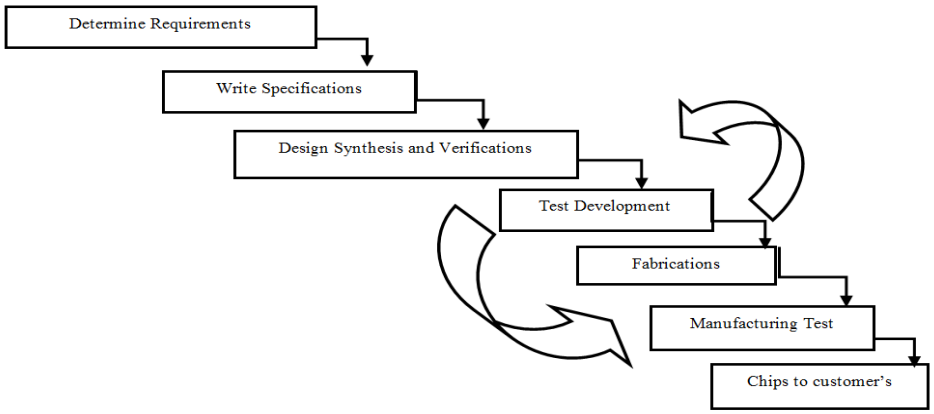



Figure 2. VLSI realization process

A significant and essential part of the fabrication operation is error validation. Grade and prudence are two main utilities of validation and verification of circuits. These two features are

highly vulnerable and cannot be demarcate without the other. A particular standard means pleasing the customer's requirements at lowest price. The goal of verification is to eliminate all ruinous goods before they arrive to the customers because the quantity of damaged goods hugely affects the cost of useful goods. An acute awareness of the standards of fabrication and verification is vital for an engineer to plan a class of product. This paper has been discussed some of these techniques with experiments and designed in PROTEUS Software. Tables and Figures are presented center, as shown below and cited in the manuscript.

## 3. Defect Detection Techniques

Here are two proposed techniques for detection of faults present in a circuit.

1. Duplication with complementary logic with the use of dual expression.
2. Permanent fault detection using time redundancy.

### 3.1. Duplication of complementary logic (Physical Redundancy)

The two duplicate resulting functions are compared with the use of duality concept in this technique. Comparator decides the failure of any one of the functions as fault detection. The functions are operated as duals of each other rather than exact duplication of each other. One function is designed using positive logic as F and the other function is designed using negative logic as FD. The outputs must be complementary to each other if the operation is correct. There are three benefits of complementary logic function:

(1) Chances of common-mode failure due to operating fault can be reduce by use of dual operation function. (2) The probability of errors that are delicate to voltage alteration causes identical effects can be minimized because the voltage alteration on the identical lines in both functions are in dissimilar directions. (3) A short between two identical lines effects in one of the two lines in which one line retaining an invalid value and the other retaining the valid value because these two lines are always at dissimilar voltage levels subsequently the error can be uncovered absolutely.

If P AND Q are complementary modules.
If S and T are inputs. And P= S.T
As we know P and Q are complementary modules:
Q= S+T
If the value of P will be 0/1, then the value of Q should be 1/0.
Suppose we have a function
A = (P1.P2 .P3) + (P4. P5. P6)
AD= (P1 + P2 + P3). (P4. + P5. + P6)
Here A and AD are complementary modules
According to XOR gate logic,
Here A and AD are complementary modules
According to XOR gate logic,

Table 1. Verification table using XOR gate

| a | b | c |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

FAULT

Only when F and $F_D$ will be complementary to each other the result will be high as 1, otherwise there may be a fault if output is 0, from this we can detect the fault in the circuit.

Moreover this technique of testing can be done using half adder circuit. Figure 3 shows the half adder circuit and its complementary module circuit which is tested by the XOR gate using PROTEUS Software.

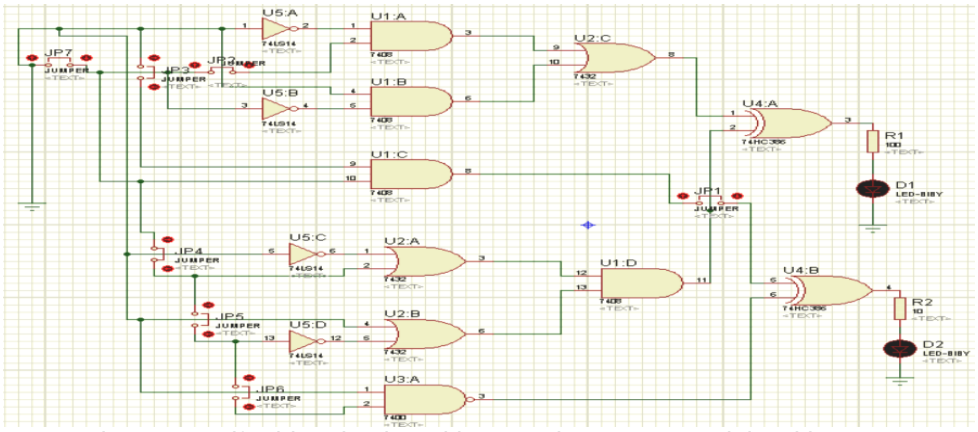



Figure 3. Half adder circuit and its complementary module with LEDs

LEDs D1 and D2 blink according to high output as 1. Output 1 shows the error free circuit by simulation.

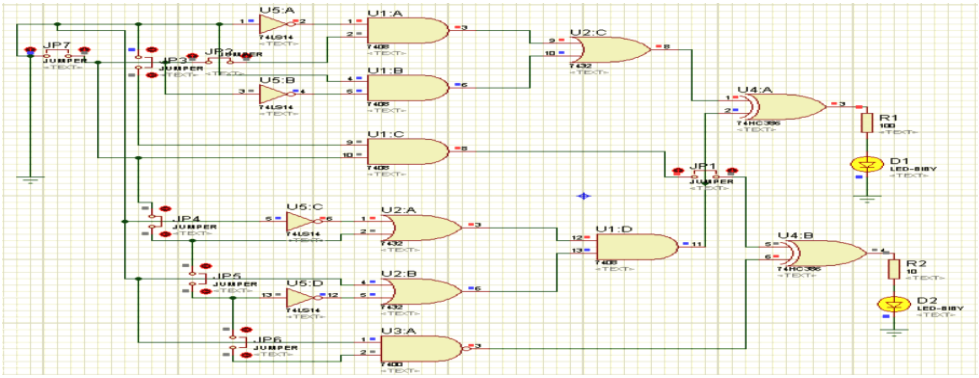



Figure 4. LEDs glowing status showing error free circuit.

In case LEDs D1 and D2 do not blink then there may be a fault in the circuit. In such a way the fault can be detected in the circuit. It is a very good and a simple technique of fault detection but it has some drawbacks also that it cannot detect the location of fault exactly. Only fault detection is possible by this technique. Second drawback is complexity issue. Circuit testing would be more cost effective with the increase of complexity in this technique.

### 3.2. Permanent Fault Detection using Time Redundancy

Time redundancy is great technique which minimizes the error diagnosis hardware by taking some additional time. The main abstraction of time redundancy is to reproduce operations in a way both transient and permanent faults can be easily detected. Figure 4 is showing the method to detect transient fault. The data must be reformed when it is executed the next time to detect permanent faults using this technique. At the last the stored results are compared by the comparator. Consequently it detects faults by the comparison of stored results. This technique is all depends upon reformation of operation with time [1].

### 3.3. Transient fault detection

Transient faults are transitory errors which occur due to bad system connections and inaccessibility of resources. Consequently, errors may be disappearing in reattempting the same operation in transient faulty system. In transient faulty system, the fault can be detected by re-execution of operation various times.

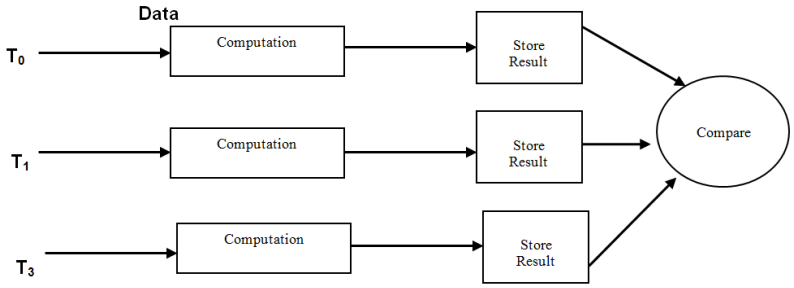
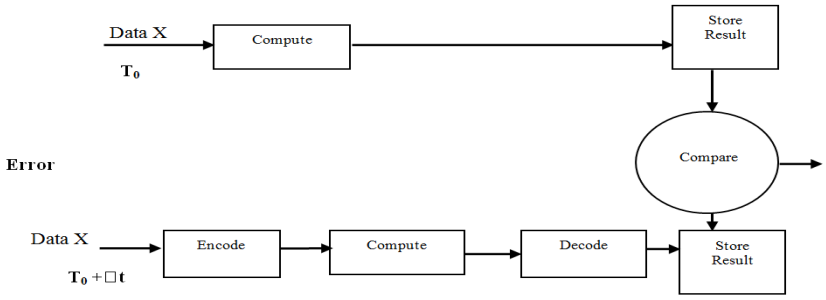



Figure 5. Time redundancy block diagram

The major drawbacks of this techniques are time, cost and delay. In this technique due to the duplicate and compare approach the all loss and penalty paid an extra hardware.

### 3.4. Permanent fault detection

This type of failure known by its endurance behaviour. The fault remains the same until the faulty component fixes error or substituted by another one. Permanent fault can be detected by re-execution of operation various times using several encryption strategies. More or less redundant hardware is required in this technique.




### 3.5. Discrimination between transient and permanent faults

The major factor is time redundancy to discriminate between transient and permanent faults. By re-execution operation after detection of the fault:

a. If fault vanishes it would be the transient fault.
b. If fault does not vanish it would be the permanent fault. This fault can vanish only by substitution of the faulty part or fixing the error of that part.
c. Permanent fault reserves resources

## 4. Result and discussion

From the results, different types of errors could be categorized and positioned on the circuit with strong fidelity. This shows that the suggested methods are capable to provide satisfactory precision in both of the fault categorization, and fault evaluation.

Table 2. Comparison Matrix of Fault Detection Methods

| Method | Speed of detection | Area and Cost | Delay | Power Consumption | Coverage |
|---|---|---|---|---|---|
| Duplication with complementary logic | Fast-As per the gate delay. | Large-due to dual circuit addition Cost- high | Less-same circuitry is repeated | Large-due to effective large effective area | Good-all manifest errors are detected |
| Permanent fault detection using time redundancy. | Slow-every stored value and comparator take different times | Large-due to redundant hardware Cost-low | Large–Every redundant component provide delay | Very high-due to redundant hardware | Very Good-transient fault & permanent faults can be detected |

## 5. Conclusion

This paper reassessments and examines two different techniques used for detecting errors in combinational digital circuits. VLSI permits us to integrate maximum circuitry in compact and more trust worthy collection. Fault detection and fault location can now be contributed inside the IC level. VLSI performs the feasibility for enhancing the design performance of fault tolerant systems by using some class of techniques all through the system.

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