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Current Steering Digital Analog Converter with Partial Binary Tree Network (PBTN)

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Abstract

DACs are essential devices in many digital systems which require high performance data converters. Thus, shrinking of supply voltage, budget constraints of test times, and rising bandwidth requirement causing DAC architectures to highly relying on matched components to perform data conversions. However, matched components are nearly impossible to fabricate; there are always mismatch errors which causes the difference between the designed and actual component value. Dynamic Element Matching (DEM) is one of the techniques that are commonly used to reduce component mismatch error. This technique is a randomization technique to select one of the appropriate codes for each of the digital input value before entering DAC block. Thus, in this research, a new DEM algorithm is proposed on Current-Steering DAC with Partial Binary Tree Network (PBTN) algorithm that utilizes a lower complexity circuit to produce output signals with less glitch. Simulation results for 6-bit 1-MSB PBTN DAC produces 0.3184LSB of DNL, 0.0062LSB of INL, and a power consumption of 14.13 mW, while using only 126 transmission gates.

Keywords: *Partial Binary Tree Network, Current Steering DAC, Differential Non-Linearity, Integral Non-Linearity*

1. Introduction

DAC (Digital to Analog Converter) is an important element in many digital systems which require data converters with high performances from digital form to analog form. DAC rely on matched components to perform data conversion. However, matched components are very difficult or nearly impossible to realize on silicon since mismatch errors always exist in real implementation. Several techniques were applied to reduce or eliminate the effect of component mismatch errors such as enlarge the devices, digital calibration, self-calibration, error- averaging or dynamic element matching [1, 2]. Dynamic Element Matching (DEM) is one of the techniques applied in DAC to reduce component mismatch error. This technique is a randomization technique that randomly selects one of the codes for each of the digital input before entering DAC block. By using this technique, the time average of equivalent component at each component position are equal or nearly equal, which reduces the effect of component differences in the circuits. DEM capable of transforming the imperfection of each 1 bit DAC into broadband noise by randomizing the position of each DAC and sum up the result so that the effect of mismatch error is averaged [3]. The connection of DEM DAC is shown in Figure 1. The results of each 1 bit DAC will be summed to yield the desired output value of DAC.

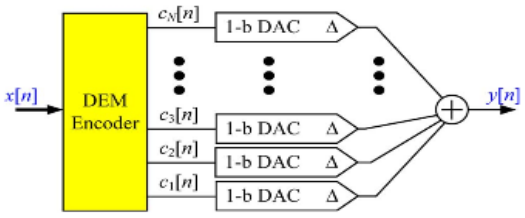

Figure 1. Structure of DEM DAC [3]

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However, the limitation of this technique is that DAC will suffer from excessive digital hardware complexity. A complicated encoding is usually necessary for conventional DEM encoders which will lead to many switch transitions happen at the same time resulting glitches in the output signal. Hence, Partial Binary Tree Network (PBTN), a new DEM algorithm to Current-Steering DAC is proposed in this paper to overcome glitches transition with low complexity. PBTN is an algorithm that utilizes the advantage of Binary Tree Network (BTN) with less hardware complexity by using much lower transmission gates compared to BTN [4]. 1-MSB PBTN is implemented to do full random switching in 1-bit MSB while other layers of LSBs are performing partial randomization due to less effect on scrambling of DAC noise.

2. Design Methodology

This section consists of three subsections that explain the design of 6-bit DEM PBTN DAC which are presented in Subsections 2.1, 2.2 and 2.3. A hardware complexity comparison between FRDEM, GCN equivalent, BTN and PBTN with 1-MSB randomization is briefly explained in Subsection 2.1. In Subsection 2.2, the propsed design of 1-MSB PBTN is presented. The Subsection 2.3 will present the final design of the 6-bit PBTN DAC.

2.1. Types of DEM Technique

Table 1 below shows the number of transmission gates required for different DEM technique for B bits of DEM DACs [4]. Thus, if 3-bit DAC is required, PBTN DAC will only need 14 transmission gates as opposed to i.e. BTN DAC that will require 32 transmission gates. Therefore, for simplicity of the explanation of the PBTN design, a 3-bit PBTN design will be discussed in detail instead of the 6-bit PBTN due to the complexity of the circuit.

Table 1. Number of transmission used for different B bit DACs

Type of DEM technique	Number of Transmission Gate required for B Bit DAC
FRDEM	$2^{B+3} - 4B - 8$
GCN	$B2^{B+1}$
BTN	$2^{B+1} + B2^{B} - 2B - 2$
1-MSB PBTN	$2^{B+1} - 2$

2.2. Partial Binary Three Network

Partial Binary Tree Network is a new DEM algorithm that combines the advantage of Binary Tree Network in [4], but with less hardware complexity compared to BTN. The PBTN method needs only 1-bit MSB undergo full random switching while other layers of LSBs are performing partial randomization due to less effect on scrambling of DAC noise.

Figure 2 illustrates a 3-bit PBTN. In general, a B bit PBTN will require B layers, 1 control signal, and 2^{B} unit of DAC and with total number of (2^{B+1} −2) transmission gates. For a 3-bit PBTN, it will consist of 3 layers, 1 control signal C_k, 8 unit DAC elements and 14 transmission gates. For 1-MSB PBTN, it only requires one control signal, C_k, a random bit sequence. This control signal C_k will cause random unit DAC being activated per input signal *x(b)*. For example, in Figure 2, if control signal C_2 is logical zero, input from MSB X_2 will be connected to four output lines $t_0(n)$, $t_1(n)$, $t_2(n)$, $t_3(n)$, input from X_1 will connected to two output lines $t_4(n)$, $t_5(n)$, and LSB X_0 will connected to 1 output line $t_6(n)$. If the given input is '101', then only five output lines will be at logical one. If the control signal was logical one, number of activated output(s) remain the same, but the position of the activated output line will be changed.

Based on Figure 2, 1-MSB PBTN is built using a transmission gate (shown in Figure 3), constructed by using one PMOS and one NMOS which is also known as the MOSFET switch to allow analog switch pass a signal level from the input to the output. Two extra MOSFETs, which are PM0 and NM0 were also included to realize the inverted 'Sel' input at the PM1.

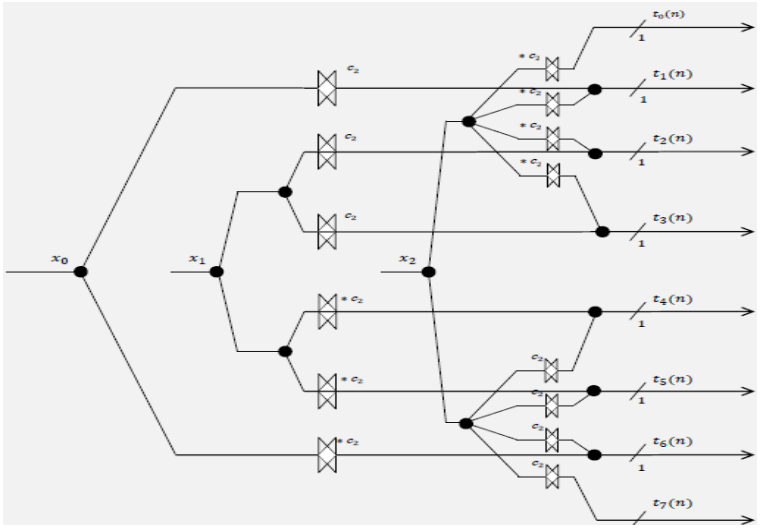

Figure 2. 3-bit 1-MSB PBTN

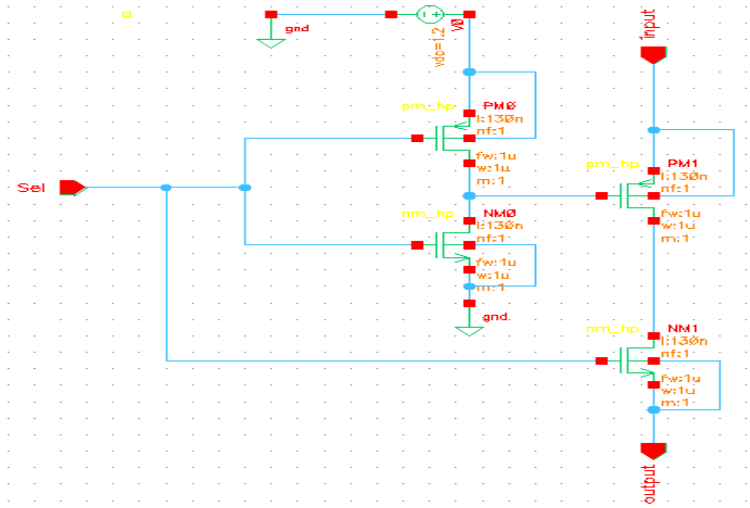

Figure 3. Transmission Gate Design

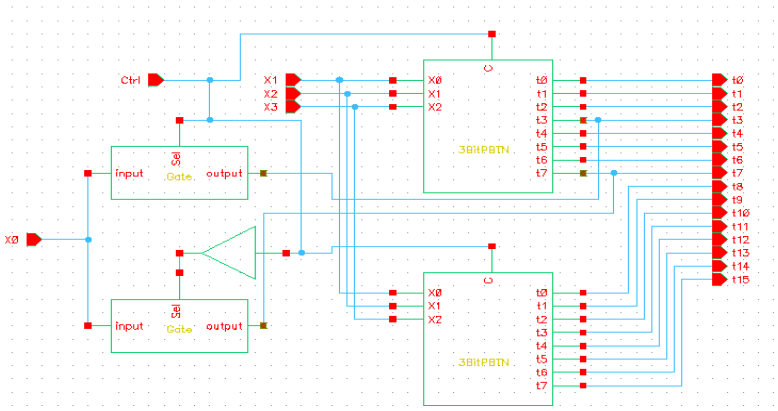

Figure 4. 4-bit 1-MSB PBTN built by using two 3-bit PBTN circuit blocks

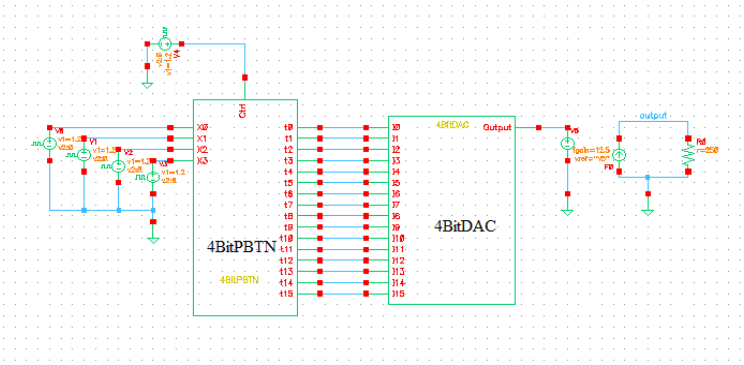

Figure 5. 4-bit 1-MSB PBTN DAC circuit

After 3-bit PBTN is established, 4-bit PBTN can be built by connecting two blocks of 3 bit 1-MSB PBTN. First three bits of binary code input were connected to two blocks of 3-bit 1-MSB PBTN. LSB X0 of the input bit were connected to two extra transmission gates, and its output were connected to output line t3 and t7 as shown in Figure 4. This circuit is later extended to build the 6-bit PBTN DAC. Figure 5 shows the block diagram of the 4-bit PBTN DAC.

2.3. 6-bit PBTN Current Steering DAC

Current Steering DAC is built based on the architecture as in Figure 6 [5]. Current Steering DAC was chosen in this research because it has constant output impedance and high conversion rate compared to other DACs. Thus, current steering DAC can handle high frequency signal used in today's technology which used boards based on 10 GHz application. In this research, to build an n-bit current steering DAC, 2^n current sources were needed. The input digital code is in the form of binary code that will be translated into thermometer code by the PBTN circuit, then the required current sources will be activated randomly.

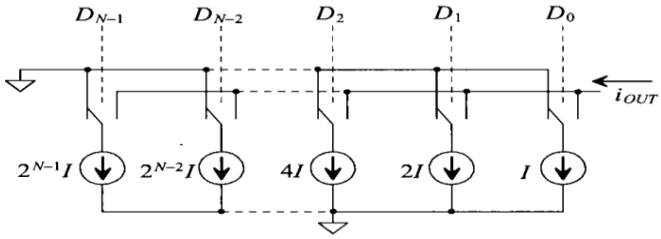

Figure 6. Current steering DAC [5]

Figure 7 shows the switchable current source circuit used to build the DAC. Each of the switchable current cell is made up of 1 pair of PMOS and 1 pair of NMOS transistors which work as cascaded current mirror, self-biased circuit and a switch. In a current cell, switching signals need to be properly matched to improve the glitch performance. The drain of NM0 and PM3 are connected to the gate which acts as a diode. When NM0 and PM3 are operating at saturation region the current obtained is:

$$K_p(V_{GSP} - V_{TP})^2 = K_n(V_{GSN} - V_{TN})^2 \quad (1)$$

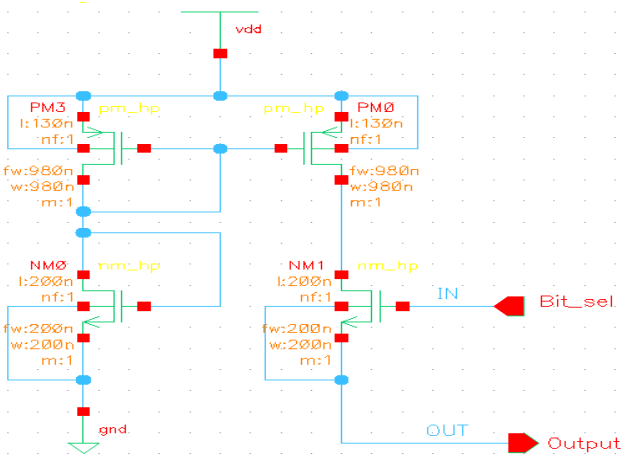

Figure 7. Switchable current source

In Figure 8, a 6-Bit PBTN-DEM current steering DAC was built by using 64 relatively simple switchable current sources (from Figure 7), connected to a 6-bit PBTN circuit (built based on the architecture as discussed in Subsection 2.2). The current sources would be activated randomly per input codes from PBTN block. The current will have summed up at the output resistor to produce the required output voltage.

For full scale output voltage from binary code '111111', 63 blocks of switchable current sources would be turned 'ON' and the remaining 1 current source will be remaining 'OFF' as a dummy block. Each of the current source forms a block of DAC which produce 20 µA current. The currents from 63 blocks will sum up and produce potential difference across output resistor as per required. In this research, the output voltage is designed to be around 1 V. Hence, 250-ohm resistor was used as an output resistor and the current 20 µA is amplified by a factor of 3.125. From Ohm's Law,

$$V_{out} = (2^6 - 1) \times IR = 63 \times 3.125 \times 20\,uA \times 250\Omega = 0.98\,V \quad (2)$$

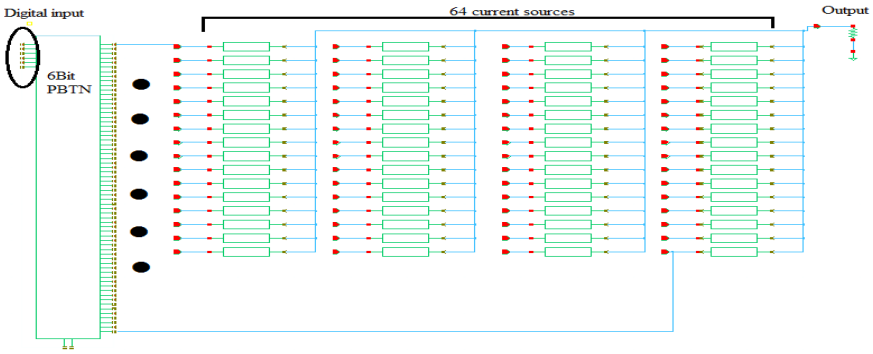

Figure 8. 1-MSB 6-Bit PBTN DAC

3. Results and Analysis

This section provides the results and discussion of the 1-MSB 6-Bit PBTN DAC. The digital input signal used for the simulation were varied from '000000' to '111111' with an update rate of 1 kHz. Simulation result for 6-bit 1-MSB PBTN DAC is shown in Figure 9. It can be observed that the output has negligible offset error of 677.5 µV. Highest glitch in the simulation result is 407.9 mV, which happened when digital inputs transition from '011111' to '100000'. This is caused by MSB transition from 0 to 1 and all LSBs which undergo transition from 1 to 0.

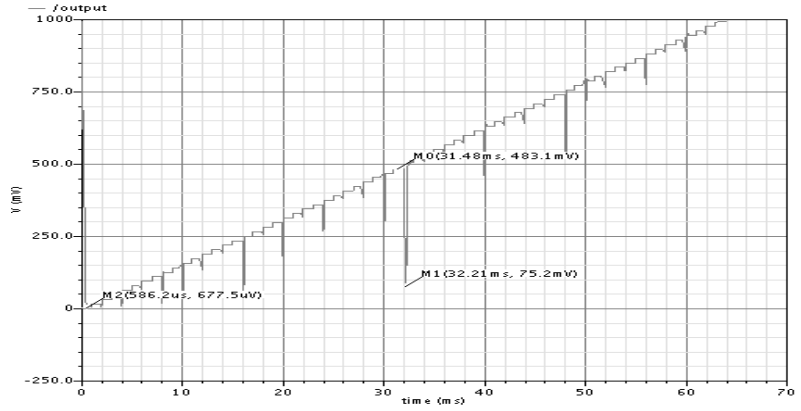

Figure 9. Simulation result of 6-Bit 1-MSB PBTN

Based on the data extracted from Figure 9, the results for the INL and DNL were calculated and tabulated in Table 2. The result for the power consumption is also presented for comparison with another works.

Table 2. Comparison with existing current steering DAC

DEM Architecture	This Work Partial Binary Tree Network (1MSB)	[6] Not used	[7] Binary Tree Structure Random	[8] Hybrid Architecture
Technology	0.13 µm CMOS	0.18 µm CMOS	90 nm CMOS	0.35µm CMOS
Resolution	6-bit	6-bit	6-bit	6-bit
DNL error (LSB)	0.3184	0.06	0.26	0.04
INL error (LSB)	0.0062	0.1142	0.45	2.32
Number of transmission gate	126	Not used	2542	Not used
Power consumption	14.13mW	944.64uW	-	165mW

From Table 2, it can be observed that DNL error of this work has no advantages over existing designs in [6-8]. However, this work has a good INL rating of about 0.0062LSB which is much lower than the existing designs. Number of transmission gates used in this work also lower than existing work [7], which achieved 95% reduction. Power consumption of this work is about 91% lower than design using hybrid architecture [8], but it uses more power than [6]. However, designs in [6] and [8] are not based on DEM architecture.

4. Conclusion

The aim of this research was to introduce a new algorithm for Dynamic Element Matching Current Steering DAC with Partial Binary Tree Network. From our research, though the conventional Binary Tree Network Dynamic Element Matching DAC had a decent performance, however it comes with high hardware complexity. But, the proposed algorithm, PBTN solves this limitation by reducing the hardware complexity to a significant level. Simulation result show that novel PBTN had the same performance with existing algorithm. To proof the concept of the proposed algorithm, a 6-bit Current Steering DAC with PBTN-DEM of 1-MSB randomization was implemented using 0.13 µm Silterra CMOS process. The PBTN-DEM DAC has been successfully designed which result of DNL error 0.3184LSB and INL error of 0.062LSB. The proposed PBTN DEM also had a power consumption of around 14 mW.

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