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Analysis and Design of High Performance Phase Frequency Detector, Charge Pump and Loop Filter Circuits for Phase Locked Loop in Wireless Applications

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Abstract

This paper presents the analysis and design of high performance phase frequency detector, charge pump and loop filter circuits for phase locked loop in wireless applications. The proposed phase frequency detector (PFD) consumes only 8 µW and utilises small area. Also, at 1.8V voltage supply the maximum operation frequency of the conventional PFD is 500 MHz whereas proposed PFD is 5 GHz. Hence, highly suitable for low power, high speed and low jitter applications. The differential charge pump uses switches using NMOS and the inverter delays for up and down signals do not generate any offset due to its fully symmetric operation. This configuration doubles the range of output voltage compliance compared to single ended charge pump. Differential stage is less sensitive to the leakage current since leakage current behaves as common mode offset with the dual output stages. All the circuits are implemented using cadence 0.18 µm CMOS Process.

Keywords*:* DRC, GDI, LVS, PLL, VCO

1. Introduction

The Phase-locked loop, commonly known as the PLL is an essential component of modern electronic systems [1]. Having a wide range of applications over a broad frequency spectrum, the PLL has become one of the most essential elements in microprocessor boards of complex systems, wired and wireless communication systems and many other systems [2]. Advances in integrated circuit technology allowed phase-locked loop circuits to be used commonly in many areas such as communications, wireless systems, consumer electronics, and motor control [5]. The phase-locked loop is used in motor control to synchronize the motor speed to a reference frequency with extreme accuracy [3]. The phase-locked loop is used in the area of consumer electronics for applications ranging from television sets to microprocessors. The phase-locked loop performs the horizontal and vertical synchronization and colour subcarrier reconstruction in television sets [4]. The phase-locked loop is used in microprocessors and other digital circuits to generate a low jitter clock signal [6]. Typical communications applications of PLLs include clock and data recovery, coherent modulation of amplitude, frequency, and phase-modulated signals, phase-locked loop receivers, and frequency synthesis [5]. Such a vast array of applications has made the PLL quite a popular circuit among today's engineers. Like almost every physical system though, PLLs have to be constantly tested for correct operation and reliability.

This paper presents the design and implementation of high performance, low dead zone, phase frequency detector**,** charge pump and loop Filter circuits for PLL based frequency synthesizer for wireless applications. Section II presents the analysis and design of phase frequency detector. Analysis and design of charge pump circuit is presented in Section III. Loop filter design and simulation are discussed in Section IV. Finally, Section V presents the discussion and conclusion of the proposed work.

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2. Analysis and Design of Phase Frequency Detector

A PLL is a feedback system that compares the output phase with the input phase. The comparison is performed by a phase comparator or a phase detector. The circuit diagram of proposed Gate Diffusion Input Cells (GDI) is as shown in below Figure 1. It works similar to conventional PFDs but it has many advantages compared to conventional PFDs. This PFD is basically constructed with two GDI cells. A basic GDI cell contains four terminals – G (common gate input of nMOS and pMOS transistors), P (the outer diffusion node of pMOS transistor), N (the outer diffusion node of nMOS transistor), and D (common diffusion node of both transistors). This technique allows reducing power consumption, propagation delay and area of digital circuits. The GDI method is based on the simple cell shown in Figure 2. Table1 shows how different logic functions can be implemented with GDI cell.

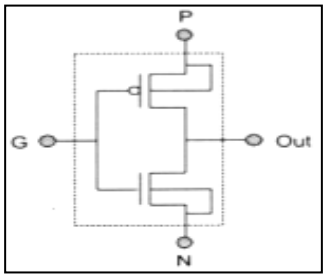

Figure1. Basic GDI Cell

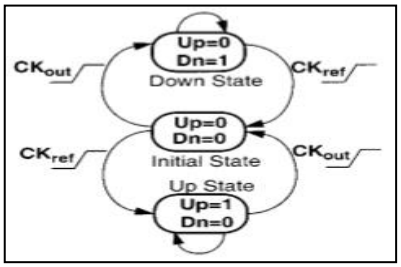

Figure 2. PFD State Diagram

When Fclk is equal to Fvco both the outputs that is Up and Down are zero, if Fclk is high compared to Fvco then up signal is high else down signal is high indicating the phase error between Fclk and Fvco. The conditions of inputs and outputs are depicted in state machine diagram shown in Figure 2.

Table 1. Logic Functions implemented with GDI cell

N	P	G	D	Function
0	B	A	A'B	F1
B	1	A	A'+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+A C	MUX
0	1	A	A'	NOT

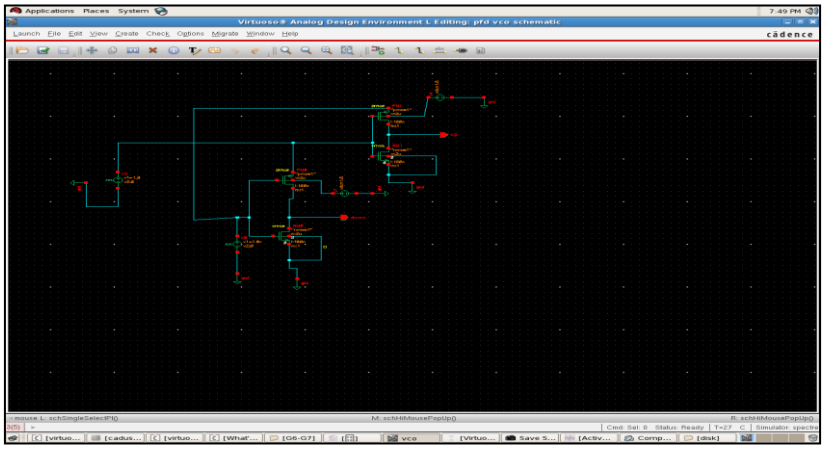

Figure 3. Schematic of PFD with GDI Cells

The schematic of PFD with GDI cells is given in Figure 3. It can be observed from this schematic that the PFD design using GDI has less complex hardware it than the conventional PFD. Hence, it requires less on-chip area.

2.1. Simulation Results

The phase frequency detector has been designed to implement the PLL at 5 GHz and simulated by Virtuoso Cadence Spectre for low dead zone, small area and low power consumption. The output of PFD with GDI cells is shown in Figure 4. The pulse illustrating phase difference is shown with UP signal with green colour. This circuit can be used in the application on high frequency, low dead zone and low power phase locked loop.

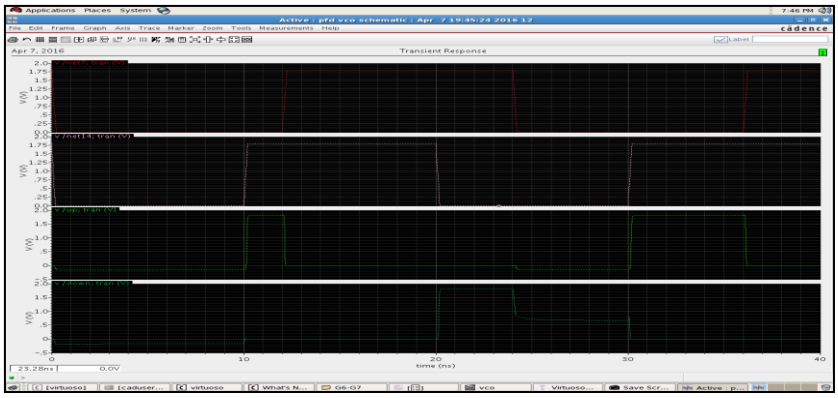

Figure 4. Output of PFD with GDI cells

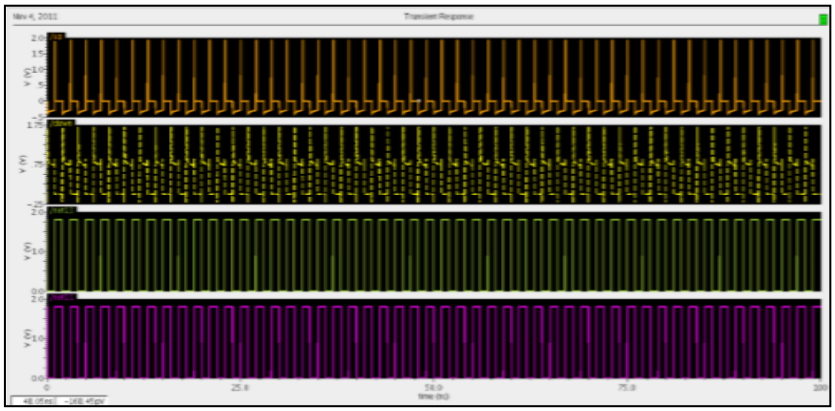

Figure 5. Simulation with Delay of 20ps

Figure 5 shows a longer simulation done on proposed PFD. The input CLK frequency is 500 MHz with Fclk leading Fvco by 20ps; this will result in having UP signal as we can see from the graph. This PFD were able to operate at much higher frequency 5GHZ is the highest frequency the PFD will operate at. Even at the phase difference of 20ps between Fclk and Fvco the proposed PFD is able to detect the difference which is depicted in Figure 5.

2.2. Circuit Layout and Performance Analysis

Virtuoso is the main layout editor of Cadence design tools. The phase frequency detector is implemented using Cadence Virtuoso 0.18µm technology. Figure 6 illustrates the layout of the conventional tri-state PFD. Layout of phase frequency detector with GDI cells are depicted in Figure 7. As shown, this PFD requires less on-chip area as compared to the conventional tri-state PFD**.** The performance comparison between both PFD topologies is shown in Table 2. Layout versus Schematic (LVS) comparison ensures that the layout actually

implements the required functionality. If the extraction program allows extracting also parasitic from the layout view, a more accurate, Post-Layout Simulation, can be performed taking into account the geometry of the circuit. The created mask layout must conform to a complex set of design rules, in order to ensure a lower probability of fabrication defects. A tool built into the Layout Editor, called Design Rule Checker (DRC), is used to detect any design rule violations during and after the mask layout design. Proposed Design shown in Figure 14 and 15 has clear DRC.

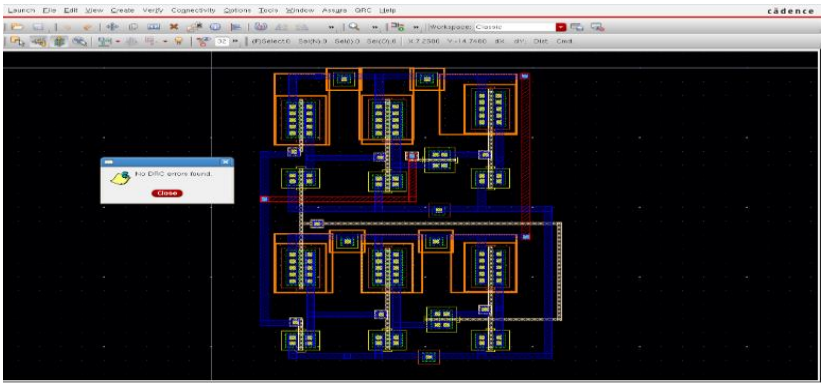

Figure 6. Layout of Conventional PFD

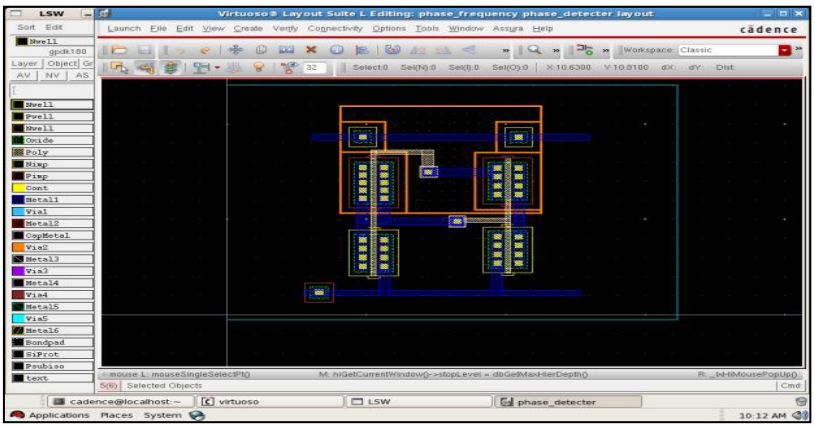

Figure 7. Layout of PFD with GDI cells

Table 2. Performance Comparison

Types of PFD	Power consumption	Maximum op. frequency	Dead zone
Conventional PFD	33.5uW	050MHz	100ps
PFD with GDI cell	8uW	5GHz	20ps

3. Analysis and Design of Charge Pump Circuit

A charge pump is a kind of DC convertor that uses a capacitor as an energy storage element. Signals coming from PFD are applied to the charge pump to steer the current into and out of the capacitor causing voltage to increase or decrease accordingly [1]. The capacitor actually forms part of the loop filter and not the charge pump itself. Figure 8 shows a basic charge pump circuit and one in operation.

The charge pump injects, subtracts, or leaves alone the charge stored across a capacitor in the low-pass filter, depending on the output of a sequential phase-detector circuit. When S1 is closed, I flow into the low-pass filter, increasing the control voltage to the VCO.

When S2 is closed, I flow out of the low-pass filter, decreasing the control voltage to the VCO. As illustrated in Figure 8(b), this process may be referred to as charging and discharging of the loop filter. When both switches are open, the top plate of the loop filter's first capacitor is open circuited and the output voltage remains constant in the steady state.

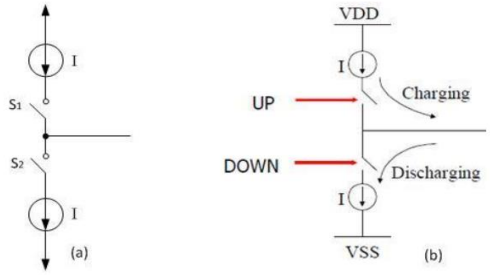

Figure 8. Simple Charge Pump

Charge pumps (CPs) are used in applications where low or high voltage than power supply are required. Charge pumps make use of capacitors as energy storage element and pump charges towards the output stage using switches to convert lower DC voltage level at the input into higher DC level voltage at the output. Charge pump is one of the important parts of PLL which converts the phase or frequency difference information into a voltage, used to tune the VCO. Charge pump converts the UP and DOWN signals generated by PFD into corresponding current values. Charge pump is followed by the loop filter. Charge pump either pumps current into loop filter or pump out the current from loop filter.

3.1. Single Ended Charge Pump

As shown in Figure 9, switch S1 is implemented using PMOS M3 while UP current source is implemented using the fixed biased M4 [27]. Similarly for discharging circuit M2 serves as switch S2 and M1 serves as DOWN current source. Inverter is inserted so that M3 will be on when QA is high. But insertion of inverter introduces a delay in path thereby introducing a skew between QA and QB. To eliminate this effect, a pass transistor gate is inserted between QB and M2. Hence delays of inverter and pass transistor gate become equal. Schematic of Single Ended Charge Pump using CMOS is shown in following Figure 10.

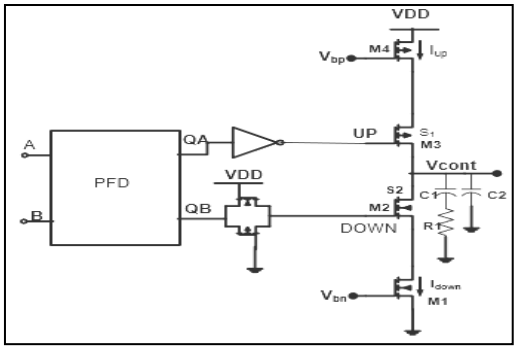

Figure 9. Implementation of Single Ended Charge Pump

3.2. Differential Charge Pump

In single ended charge pump, only two inputs UP and DOWN are given to the respective switches, while in differential charge pump two outputs of PFD are given to the two differential switches with each input inverted and given to the second input of the respective switch. Figure 11 shows the circuit of differential charge pump.

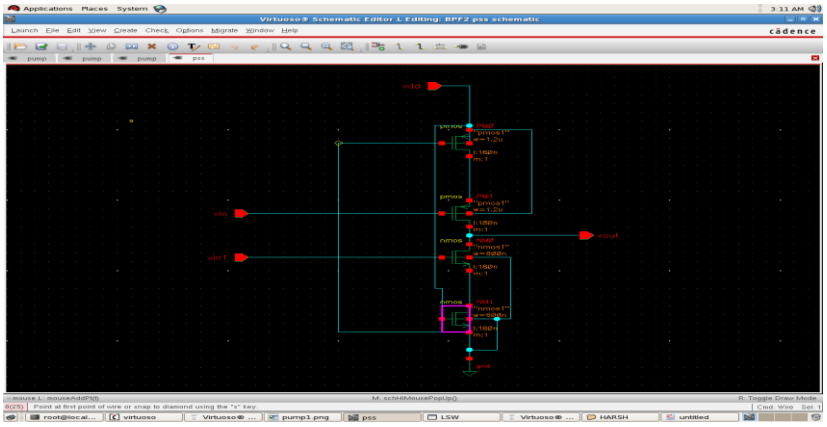

Figure10. Schematic of Single Ended Charge Pump

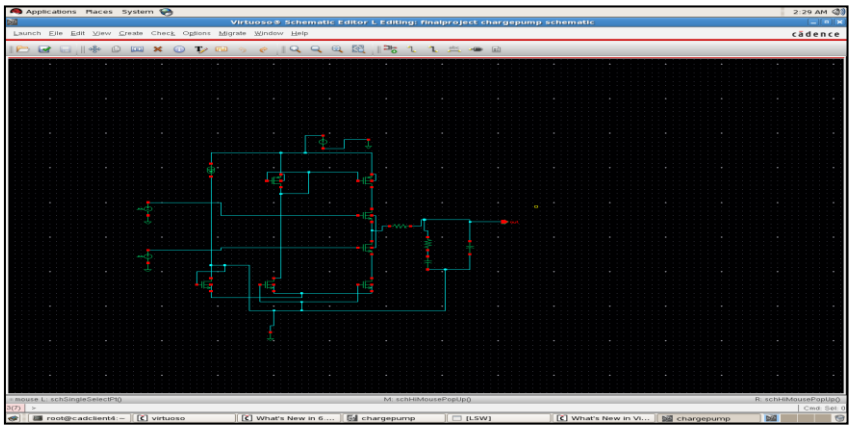

Figure 11. Schematic of Differential Charge Pump

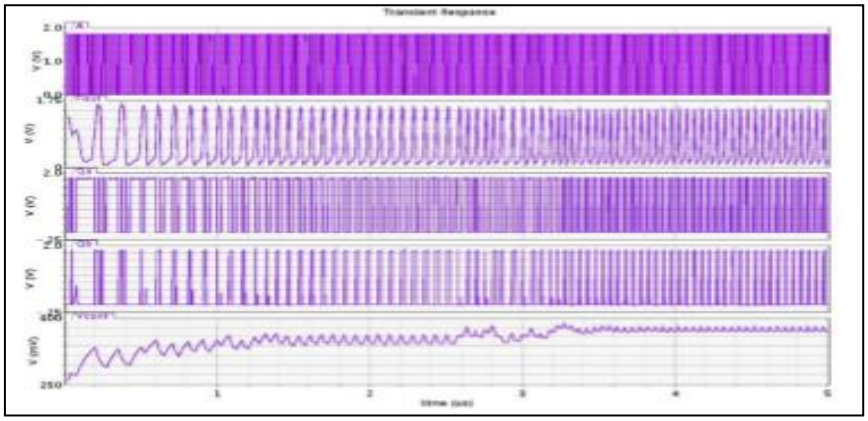

Figure 12. Transient response of Basic Charge Pump PLL

3.3. Simulation Results

All circuits in this work are implemented using “Cadence” tool in “Virtuoso Analog Design Environment”. The library used is GPDK180 with 180nm technology. All the circuits are simulated using “Spectre” simulator tool. The voltage supply used is 1.8V. Reference frequency is kept at 40MHz and simulation is run for 10μs.

3.3.1 Single Ended Charge Pump

The simulation is run for 10μs transient time period. Figure 12 shows the transient response of basic charge pump PLL while Figure 13 shows the time versus frequency response. As seen in Figure 12, the output frequency of PLL is initially away from the reference input frequency. The PFD then produces the pulses, such that CP-LPF combination drives the VCO towards the reference input frequency. Control voltage starts increasing and once the loop is locked, it remains relatively stable. As discussed earlier, this transition is nonlinear phenomenon which is clearly seen in Figure 13. It can also be seen that the loop is locked at 20MHz instead of 40MHz, which it should. The power consumption is found as 0.1751mW and current mismatch is found to be around 76μA. The value of reference spur is found to be -32.6155dBc.

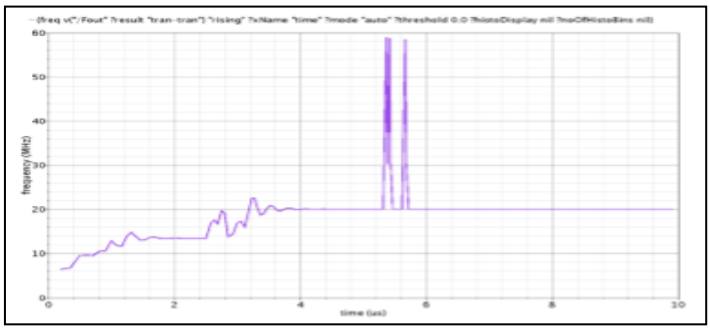

Figure 13. Time Verses Frequency Response of Basic Charge Pump PLL

3.3.2 Differential Charge Pump Circuit

Figure 14 shows the output for differential charge pump circuit. It also illustrates the output waveforms of PFD. CP basically used to convert the digital output of PFD into a current signal, so that a stable controllable signal is generated for oscillator to control the oscillation frequency. Charge pump stores the charge in the capacitor of Loop Filter.

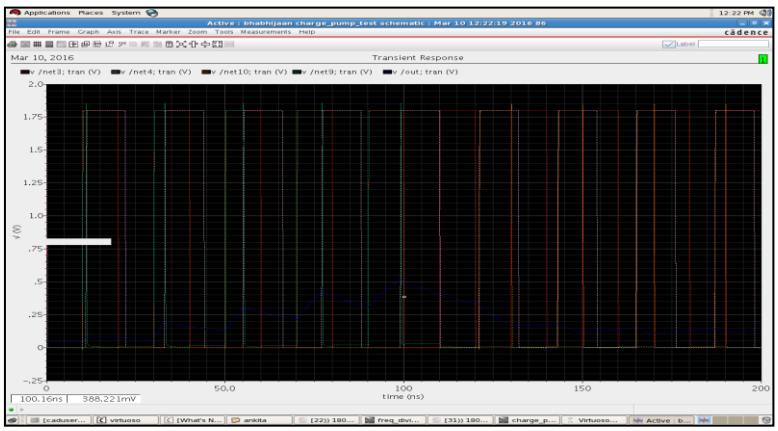

Figure 14. Output of Differential Charge Pump Circuit

4. Loop Filter Design and Simulation

Filters are frequently added after the charge pump to reduce the ripple. The function of the loop filter is to convert the output signal of phase frequency detector to control voltage and also to filter out any high frequency noise introduced by the PFD. The loop filter shown in Figure 15 used with this type of PFD is a simple RC low-pass filter. Since the output of the PFD

is oscillating, the output of the loop filter will show a ripple as well, even when the loop is locked. A ripple on the output of the loop filter with a frequency equal to the clock frequency will modulate the control voltage of the VCO. Figure 16 shows the output of loop filter. It is nothing but the AC response of loop filter.

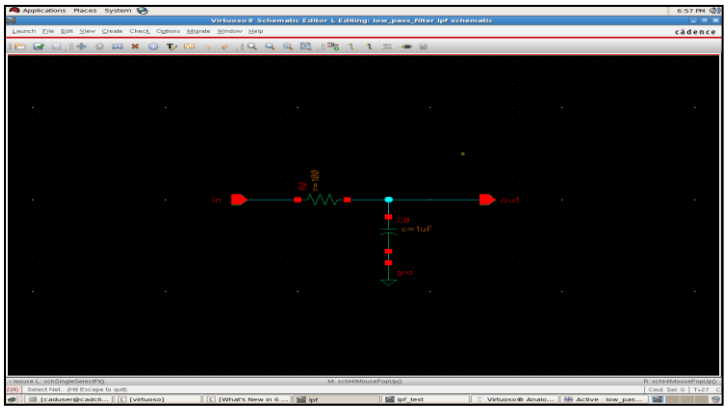

Figure 15. Schematic of Loop Filter

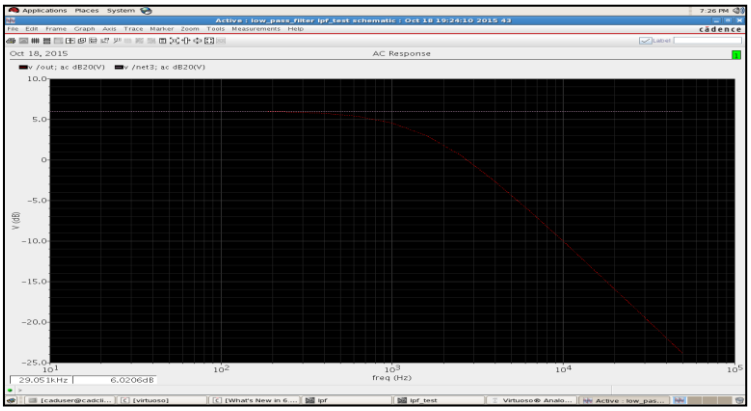

Figure16. Output of Loop Filter

5. Discussion and Conclusion

Comparison of maximum operation frequency between conventional PFD and PFD with GDI cell shows the variations of the maximum operation frequency with supply voltage. At 1.8V voltage supply the maximum operation frequency of the conventional PFD is 500 MHz whereas proposed PFD is 4.5 GHz .This indicates that proposed PFD is reliable in high speed applications. The switching mismatch between NMOS and PMOS does not affect the overall performance substantially in charge pump circuit. The matching requirement between NMOS and PMOS transistors are relaxed to the matching between NMOS or between PMOS transistors respectively. The differential CP uses switches using NMOS and the inverter delays for UP and DN signals do not generate any offset due to its fully symmetric operation. This configuration doubles the range of output voltage compliance compared to single ended charge pump. Differential stage is less sensitive to the leakage current since leakage current behaves as common mode offset with the dual output stages.Though differential CP has many advantages listed above, they suffer from critical drawbacks. They require two loop filters and common mode feedback circuitry. Since more number of transistors are required, with two or more current sources, they occupy large silicon area. This also leads to higher power consumption.

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