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Low Power FGSRAM Cell Using Sleepy and LECTOR Technique

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Abstract

In this paper floating gate MOS (FGMOS) along with sleep transistor technique and leakage control transistor (LECTOR) technique has been used to design low power SRAM cell. Detailed investigation on operation, analysis and result comparison of conventional 6T, FGSRAM, FGSLEEPY, FGLECTOR and FGSLEEPY LECTOR has been done. All the simulations are done in Cadence Virtuoso environment on 45 nm standard CMOS technology with 1 V power supply voltage. Simulation results show that FGSLEEPY LECTOR SRAM cell consumes very low power and achieves high stability compared to conventional FGSRAM Cell.

Keywords*: leakage power, power gating, mtcmos, sleepy stack, zigzag*

1. Introduction

Recently numerous techniques have been reported in the literature to design low power VLSI circuits. Some of the most widely used techniques for low power Static Random Access Memory (SRAM) design are as follows. In power gating technique the unused components of the circuit are temporarily disconnected to reduce leakage current [1]. Sleep transistor technique uses PMOS sleep transistors in between supply power and pull up network and NMOS sleep transistors in between pull down network and ground to cut the supply power and ground when the device is in standby mode [2]. MTCMOS technique introduced in 1995 uses both high and low threshold transistors to achieve low leakage power. Low Vt is used where switching speed is more important than leakage dissipation and high Vt is used where we need to compress the leakage dissipation. In sleepy keeper technique both sleep and keeper techniques are used. Here high threshold NMOS keeper transistor is added in parallel with sleep PMOS transistor and high threshold PMOS transistor is added in parallel with sleep NMOS transistor to reduce the leakage power [3]. Sleepy stack introduced in 2005 by Park uses both sleep transistor technique and forced stack techniques are used here. The sleepy stack technique can keep the original state than the sleep transistor technique [4]. Zigzag technique is introduced in 2005. Here, in each logic stage either in NMOS or PMOS one sleep transistor is used in this technique in accordance with the input vector to achieve the lowest possible leakage power consumption [5] but amongst them LECTOR is the most efficient technique because it reduces the leakage current without affecting the dynamic power dissipation [6].

This paper focuses on the problem area of low power to implement the SRAM which is one of the basic memory elements in the field of processors and controllers of the computers and mobile applications for better longevity of the battery life. Section 2 describes various low power techniques and their implementation on CMOS process. In this section, a hybrid technique SLEEPY- LECTOR has been proposed which shows better performances as well as reduces more leakage power than other techniques in various mode of operation. Results and analysis have been discussed in section 3.

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2. Research Method

2.1. Conventional 6T SRAM cell

The conventional 6T SRAM cell as shown in Figure 1 can be built using two cross coupled CMOS inverters. It can store a single bit either '0' or '1'. M3 and M4 are two pass transistors which are also known as access transistors. There are also word line 'WL' and bit lines 'BL' and 'BL_bar'. WL is used to turn on the access transistors and connects the cell with the BL and BL_bar during 'read', 'write' and 'standby' operation.

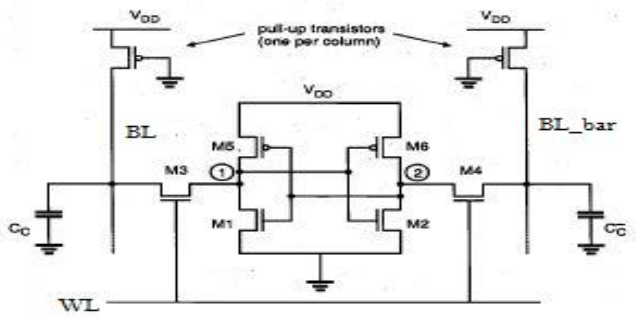

Figure 1. Conventional 6T SRAM cell

2.1.1. Read Operation

Let us assume that a "0" is stored in the cell as shown in Figure 2. PMOS M5 and NMOS M2 are turned off whereas PMOS M6 and NMOS M1 are still operating in the active mode. At the beginning of the read operation the internal node voltages V_1 is 0V and V_2 is Vdd. Both bit lines are pre-charged to high value i.e., the values of both bit lines will be same during the read operation. Now M3 and M1 will conduct a nonzero current when M3 and M4 pass transistors are turned on. Hence, the voltage level of BL will start to go down slightly whereas, no significance change will occur on BL_bar. During the read operation voltage V_1 should not exceed the threshold voltage of M2, because if M2 is turned on during the read operation then the node voltage at V_2 will be discharged through M2. Hence, during the read operation two conditions are to be taken care of [7]

$$V_1 < V_{T,2} \tag{1}$$

$$\frac{k_{n,3}}{k_{n,1}} = \frac{\frac{W3}{L3}}{\frac{W1}{L1}} < \frac{2\left(V_{dd} - 1.5V_{T,n}\right)V_{T,n}}{\left(V_{dd} - 2V_{T,n}\right)^2} \tag{2}$$

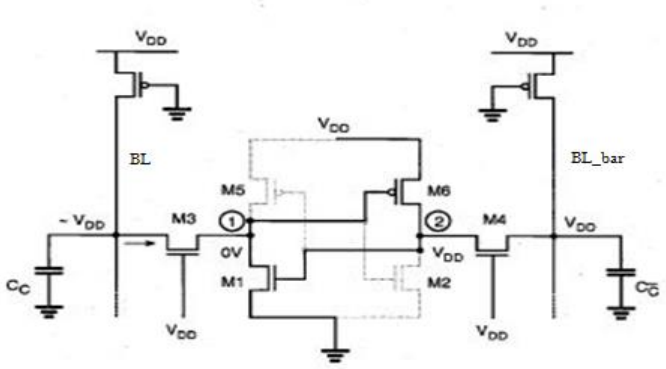

Figure 2. SRAM During Read Operation

2.1.2. Write Operation

Assume that "1" is stored in the cell shown in Figure 3. The transistor M5 and M2 will operate in the active mode and transistor M6 and M1 will be turned off. Thus at the beginning the internal node voltages are V_1=Vdd and V_2=0 V. Now to perform a write "0" operation, cell access transistor M3 and M4 are turned on and BL is set low and BL_bar is set high. The node 2 voltage level should not be large enough to turn on NMOS M1; otherwise the node voltage at V_1 will be discharged through M1. So the following two conditions must be satisfied [7]:

$$V_1 < V_{T,1} \tag{3}$$

$$\frac{k_{p5}}{k_{n,3}} = \frac{\frac{W5}{L5}}{\frac{W3}{L3}} < \frac{\mu_n}{\mu_p} \frac{2\left(V_{dd} - 1.5V_{T,n}\right)V_{T,n}}{\left(V_{dd} + 2V_{T,p}\right)^2} \tag{4}$$

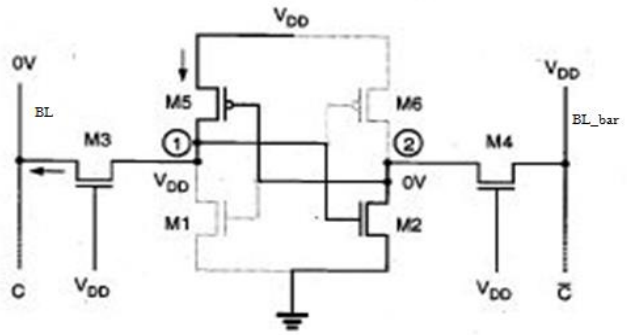

Figure 3. SRAM During Write "0" Operation

Opposite action should be taken for write "1" operation.

2.1.3. Standby Operation

If the word line is not asserted, both NMOS M3 and M4 pass transistors disconnect the cell from the bit lines. The NMOS transistor M1 and PMOS transistor M6 formed two inverters which are cross coupled each other keep on to strengthen themselves as long as they are cut off from the outer side of the world.

2.2. Static Noise Margin (Snm)

At a storage node, the highest reasonable DC noise voltage which does not affect the read disturbance is called SNM. It is the distance end to end of the diagonal of the largest square which can fit into the "eyes" of the butterfly curves, is known as the read voltage transfer characteristics (VTC) of the cell. This is metric to measure the performance of the SRAM cell design. The Supply voltage (Vdd), Cell Ratio (CR) and Pull-up Ratio (PR) are the major factors of SNM. Permanence of the SRAM cell requires high-quality SNM [8]. 70 % value of the SNM depends on the driver transistors.

2.2.1. Cell Ratio (CR)

The ratio which is defined as the ratio between the sizes of the driver transistor (M1) and pass transistor (M3) during the read operation is called Cell Ratio. For Figure 1 Cell Ratio can be expressed as:

Cell Ratio = (W1/L1) / (W3/L3) (5)

2.2.2. Pull-up Ratio (PR)

The ratio which is defined as the ratio between sizes of the load transistor (M6) and the pass transistor (M4) during the write operation is called Pull-up Ratio. For Figure 1 Pull-up Ratio can be expressed as:

Pull-up Ratio = (W6/L6) / (W4/L4) (6)

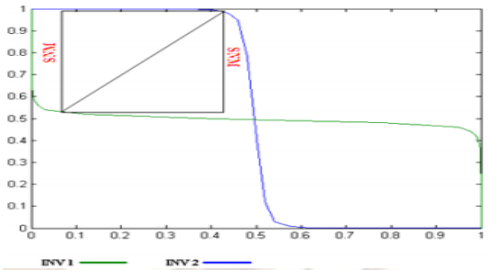

Figure 4. “Butterfly” Curve of Conventional 6T SRAM

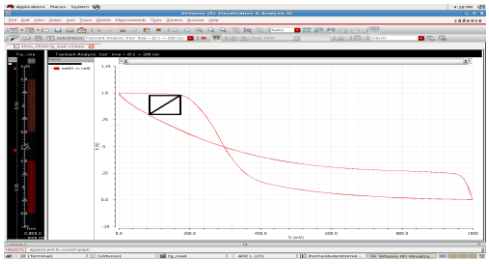

Figure 5 (a). “Butterfly” curve of FGSRAM

SNM = ‘Maximum length between the corner of the square’.

Maximum length between the corner of the square = Greatest length of the diagonal of Square / Square Root of 2 [9].

Butterfly curve of FGSRAM (Figure 4) and FGSLEEPY LECTOR SRAM is shown in Figure 5(a) and 5(b) during Read operation.

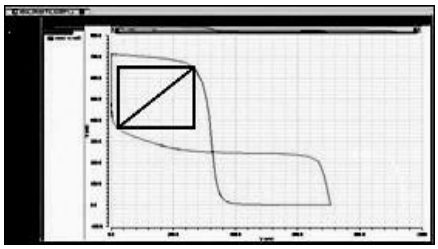

Figure 5 (b). “Butterfly curve” of FGSLEEPY LECTOR SRAM

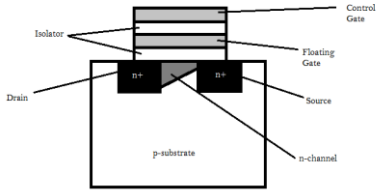

Figure 6. Floating Gate MOS

2.3. Floating Gate MOSFET

Figure 6 shows the structure of FGMOS. It is used in a flash memory to store bits. Register capacitor logic is used here as shown in Figure 7. If the floating gate is not charged then the FGMOS acts almost similar to the MOS transistor. FGMOS acts like a non-volatile memory. Secondary gates are used here which are mainly electrically isolated, so inputs are act like floating inputs. Using FGMOS, SRAM cell has been designed as shown in Figure 8.

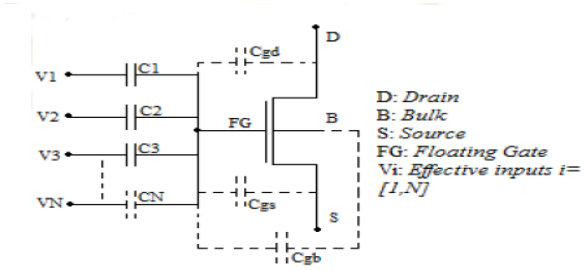

Figure 7. N-Channel N-input FGMOS Transistor [10]

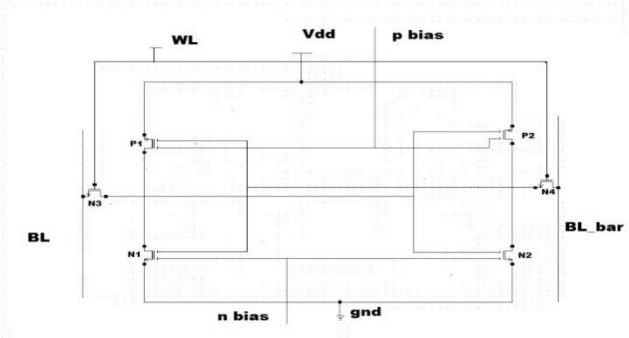

Figure 8. FGSRAM

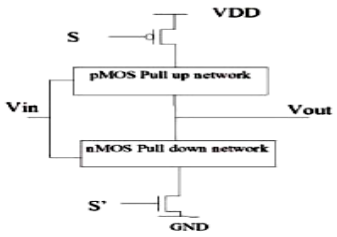

Figure 9. SLEEPY Transistor Technique

2.4. Sleepy Technique

Sleep transistors as shown in Figure 9 are very useful for reducing the leakage current. During the standby mode the leakage transistors are turned off and cut off the supply rails. The sleep transistors provide a very high impedance path between ground and power supply and a minimum amount of subthreshold leakage current flows. Normal SRAM Cells have lower threshold voltages but the sleep transistors have higher threshold voltages, the low leakage PMOS transistor is used as a header switch (S) to shut-off power supply & footer (S') NMOS transistor is used to control the power supply in the Figure 9. The sleep transistors(S and S') are switched off when at rest and can help to accumulate about 40% leakage power as they formulate virtual ground and virtual power circuits. Figure 10 shows the FGSRAM using sleepy technique.

2.5. Lector Technique

Figure 11 shows the LECTOR [11] technique that gives the effective transistor stacking from supply voltage to ground. It is a very effective technique for leakage reduction. It is observed that leakage current is less if there are more than one transistors are OFF in a path from supply voltage to ground compared to only one transistor OFF in any supply to ground path [12-16].

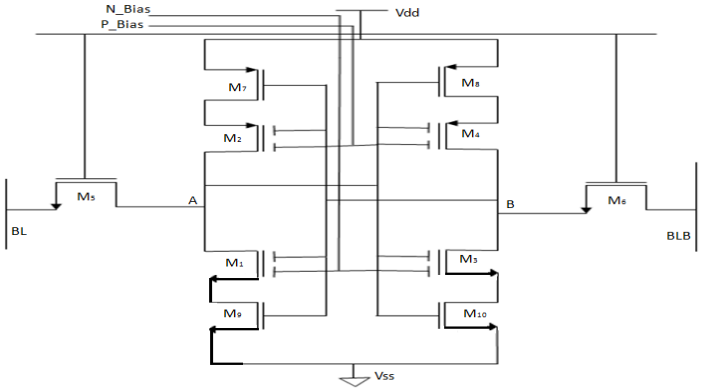

Figure 10. FGSLEEPY SRAM

In Figure 11, two transistors LC2 and LC1 are connected in between the pull down and pull up network reduces the leakage current. So, the two transistors LC1 and LC2 used in Figure 11 are called leakage control transistor. In the figure, X1 and X2 are internal nodes. The switching of the two transistors LC1 and LC2 are controlled by the potential at node X1 and X2. The drain of LC1 PMOS and LC2 NMOS are connected together and the output is taken from the common drain. Due to this setup among the two LCs one is always nearly in the cut off region increasing the resistance from supply voltage to ground and in turn causing reduction of subthreshold leakage current, there by the static power. It doesn't affect the dynamic power. Figure 12 shows the topology of FGSRAM using Lector technique.

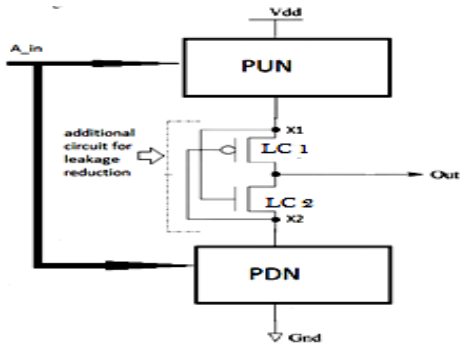

Figure 11. LECTOR Technique

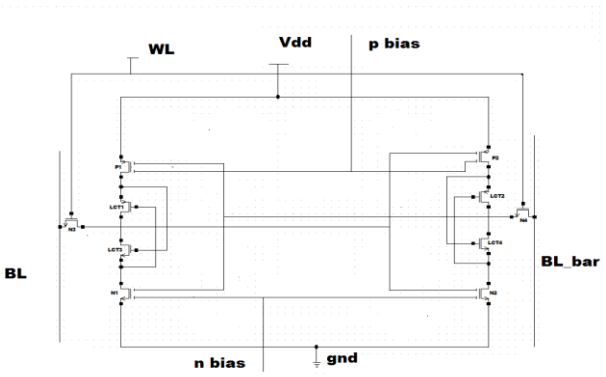

Figure 12. FGLECTOR SRAM

2.6. Fgsram Using Sleepy and Lector Technique

Figure 13 shows the proposed FGSRAM using sleepy and lector techniques. Sleepy technique in when used in FGSRAM cell, it is observed that leakage power; delay and power consumption is reduced due to sleepy effect [17]. Lector technique when used in FGSRAM cell it is observed that leakage power and delay is increased than FGSLEEPY SRAM but overall power consumption is reduced due to lector effect. Again it is observed that all the parameters like leakage power, delay and power consumption is reduced than FGSRAM cell due to effect of lector technique. So, both sleepy and lector technique are combined to reduce leakage power, power consumption and to make the cell faster than FGSRAM Cell. The simulation results of all SRAM Cells are given below in Table 1 to Table 5.

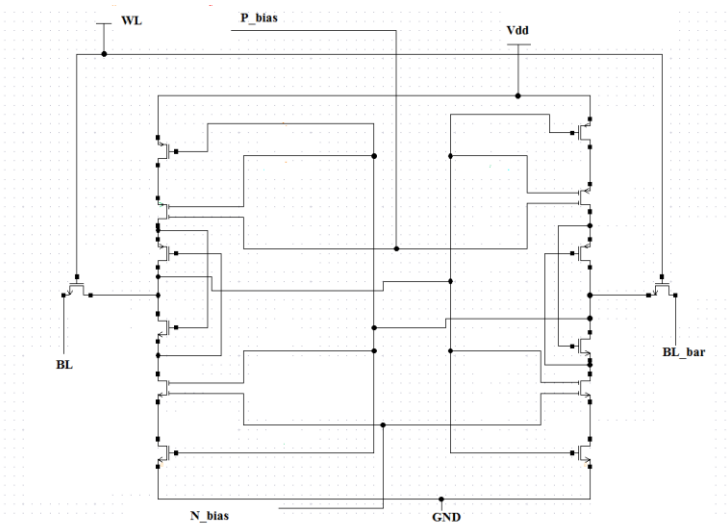

Figure 13. FGSLEEPY LECTOR SRAM

Table 1. Write 1 Operation

SRAM cell	LEAKAGE POWER	DELAY	POWER CONSUMPTION	SNM
6T	7.4 pW	137.2 ps	13.8 uW	84.8 mV
FGSRAM	3.7 nW	152.6 ps	228.5 nW	424.2 mV
FGSLEEPY	1.7 pW	95.5 pS	102.6 nW	636.3 mV
FGLECTOR	318.6 pW	125.7 ps	85.4 nW	395.9 mV
FGSLEEPY LECTOR	1.5 pW	139.6 ps	16.1 nW	424.2 mV

3. Results and Analysis

The various low power technique based circuits which have been discussed in the previous section (research method) has been implemented in GPDK 45 nm technology in Cadence Virtuoso Environment with a supply voltage of 1 V. In this section, simulation results of different types of SRAM with applied technique has been discussed in the below mentioned tables.

Table 2. Write 0 Operation

SRAM cell	LEAKAGE POWER	DELAY	POWER CONSUMPTION	SNM
6T	16.2 pW	137.6 ps	13.9 uW	84.8 mV
FGSRAM	3.4 nW	296.9 ps	228.5 nW	424.2 mV
FGSLEEP	1.2 pW	210.7 pS	102.6 nW	636.3 mV
FGLECTOR	318.6 pW	278.5 ps	85.4 nW	395.9 mV
FGSLEEPYLECTOR	1.1 pW	300.3 ps	16.1 nW	424.4 mV

Table 3. Read 1 Operation

SRAM cell	LEAKAGE POWER	DELAY	POWER CONSUMPTION	SNM
6T	7.4 pW	138.4 pS	17.5 uW	84.5 mV
FGSRAM	3.4 nW	153.2 pS	4.0 uW	247.4 mV
FGSLEEPY	1.7 pW	95.9 pS	3.8 uW	707.1 mV
FGLECTOR	318.6 pW	126.1 pS	3.8 uW	395.9 mV
FGSLEEPYLECTOR	1.5 pW	139.5 pS	3.7 uW	424.3 mV

Table 4. Read 0 Operation

SRAM cell	LEAKAGE POWER	DELAY	POWER CONSUMPTION	SNM
6T	16.2 pW	138.8 pS	17.5 uW	84.5 mV
FGSRAM	3.4 nW	297.6 pS	4.0uW	247.4 mV
FGSLEEPY	1.2 pW	211.3 pS	3.8uW	707.1 mV
FGLECTOR	318.6 pW	282.1 pS	3.8 uW	395.9 mV
FGSLEEPYLECTOR	1.1 pW	300.1 pS	3.7uW	424.3 mV

Table 5. Hold Operation

SRAM cell	LEAKAGE POWER	POWER CONSUMPTION
6T	798.5 nW	5.5 uW
FGSRAM	88.2 nW	24.8 nW
FGSLEEP	1.7 nW	1.7 nW
FGLECTOR	37.6 nW	9.0 nW
FGSLEEPYLECTOR	2.6 pW	75.2 pW

In the above tables, Floating Gate Sleepy Lector based SRAM has been compared with other available techniques like standard 6T SRAM cell, FGSRAM cell, FGSleepy based SRAM and FGLector based SRAM.

From Table 1 for WRITE 1 operation it is observed that by applying sleepy lector technique on FGSRAM cell leakage power reduced 99.8%, delay decreased by 11.1% & power consumption reduced by 93% than the FGSRAM cell.

From Table 2 for WRITE 0 operation it is observed that by applying sleepy lector technique on FGSRM cell leakage power reduced 99.7%, delay increased 1.14% & power consumption is reduced by 93% than the FGSRAM cell.

From Table 3 for READ 1 operation it is observed that by applying sleepy lector technique on FGSRAM cell leakage power reduced by 99.8%, delay decreased by 8.9% & power consumption reduced by 7.5% than the FGSRAM cell.

From Table 4 for READ 0 operation it is observed that by applying sleepy lector technique on FGSRM cell leakage power is reduced by 99.7%, delay increased 0.8% & power consumption is reduced by 7.5% than the FGSRAM cell.

From Table 5 it can be observed using FGSLEEPY LECTOR during HOLD operation 97% leakage power is reduced and 99.97% total power consumption is reduced than the FGSRAM cell.

4. Conclusion

Simulation results shows that proposed FGSLEEPY LECTOR SRAM consume 99.9% less power, dissipates 93% less leakage compare to conventional FGSRAM Cell. It can also be found that by using FGSLEEPY LECTOR technique read stability increases by 41.7%. Only drawback of this is that 0.98% delay is increased in WRITE 0 and READ 0 operation compare to FGSRAM Cell which is tolerable as power consumption and leakage is highly reducing.

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