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Comparison of DSTATCOM Performance for Voltage Sag Alleviation

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Abstract

This paper describes the comparative analysis of three different control techniques of distributed flexible AC transmission system (DFACTS) controller called as distributed static synchronous compensator (DSTATCOM), aimed at power quality (PQ) enhancement in terms of voltage sag mitigation in a three-phase four-wire (3p4w) distribution system. A DSTATCOM is one of the major power quality improvement devices which consist of a DC energy source, a voltage source inverter (VSI), a filter, a coupling transformer and the control system. The control strategy based on synchronous reference frame (SRF) theory, instantaneous active and reactive current (IARC) theory and propositional-integral (PI) controller has been used for reference current generation of voltage source inverter (VSI) based DSTATCOM. The SRF, IARC and PI control based DSTATCOM is validated through dynamic simulation in a MATLAB\SIMULINK environment under linear as well as nonlinear loads.

Keywords: *power quality, voltage sag, distributed static compensator, voltage source inverter, and synchronous reference frame*

1. Introduction

Recent work on worldwide power distribution shows a substantial growing number of sensitive loads such as hospital equipment, industry automation, semiconductor device manufacturer. The most common characteristics of these loads in modern industry and commercial applications are their ability to produce voltage sags and swells. According to an Electric Power Research Institute (EPRI) report, the economic losses due to poor power quality are $400 billion, a year in the U.S alone [1-2].

Voltage sags are a momentary decrease in root mean square (RMS) voltage between 10 % to 90 % at the power frequency [3]. Voltage sags are usually caused by faults [4], energization of heavy loads, starting of large induction motors and load transferring from one power source to another [5-6]. Voltage sags are characterized by their magnitude and duration [7].

There, are many different solutions have been proposed to eliminate voltage sags [8], conventionally the passive filters are used for power quality issues. But nowadays power electronics based on new kinds of emerging custom power devices such as Dynamic voltage restorer [9], Distributed static compensator [10], and unified power quality conditioner have been more popular because they offer the advantages of flexibility and high performance to improve the controllability of power distribution network [11].

The DSTATCOM is one of the solid-state shunt connected CPD, which is one of the victorious solutions to enhance different significant aspects of power quality [12-16]. The performance of DSTATCOM depends upon the control algorithm used for reference current calculation and firing pulse generation strategy. Most common and popularly used control strategies for 3p4w DSTATCOM are an instantaneous active power theory, symmetrical component theory, improved instantaneous active and reactive current component theory [17], p-q and p-q-r theory [18] hysteresis current controller technique [19], d-q reference frame or synchronous reference frame theory [20], etc.

In this work, synchronous reference frame theory, instantaneous active and reactive current theory and propositional-integral controller are used for the control of VSI based DSTATCOM. A new configuration of DSTATCOM is proposed for a three-phase four-wire power distribution system, which is based on six-leg VSI. The DSTATCOM is modulated and simulated

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using time-domain MATLAB\Simulink platform to mitigate voltage sags under linear and nonlinear load. Comparative analysis of the control strategies under linear and nonlinear loads in between without compensator and with compensator is presented.

2. Description OF DSTATCOM Configuration

Figure 1 shows a schematic diagram of a shunt connected power electronic based DSTATCOM with balance resistive-capacitive (R-C) and a diode-rectifier load connected to a three-phase four-wire distribution network having a source resistance and inductance. The DSTATCOM produces suitable compensating currents (i_{Ca}, i_{Cb}, i_{Cc}) and injected into each phase of the system to eliminate voltage sags. To filter high-frequency components of compensating currents, an interfacing inductance L_f is used at AC side of the voltage source inverter based DSTATCOM.

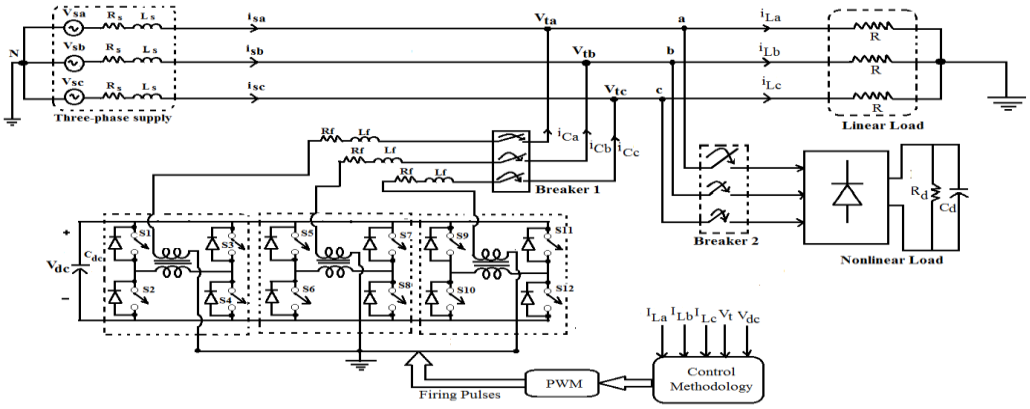

Figure 1. Schematic Diagram of VSI-Based DSTATCOM

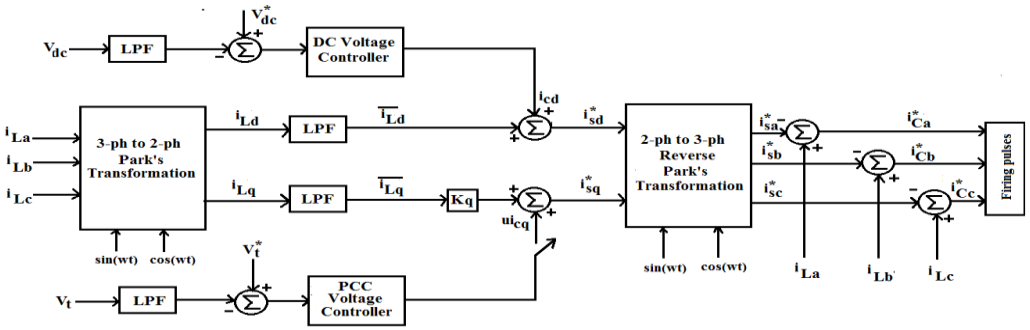

Figure 2. Block Diagram of SRF Controller

3. DSTATCOM Control Strategiey

Control strategy plays the most important role in any custom power devices (CPDs). The performance of a DSTATCOM system solely depends upon its control technique for generation of reference signals (current and voltage). For this purpose, there is several control algorithms are presented in literature, and some commonly used control techniques are Synchronous Reference Frame (SRF) theory [21], Sinusoidal Pulse Width Modulation (SPWM) technique [22], Adaptive Neuro Fuzzy interface system (ANFIS) technique [23], Instantaneous Active and Reactive Current (IARC) theory and PID control technique [24]. Among these control approaches, SRF, IARC, and PI control techniques are popularly used.

3.1. Synshronous Reference Frame (SRF) Theory

This control scheme is based on the transformation of load currents (i_{La}, i_{Lb}, i_{Lc}) from a-b-c frame to the synchronous rotating reference frame to extract the direct, quadrature and zero-sequence components is given in the equation (1). A block diagram of the control topology is shown in Figure 2.

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \\ i_{Lo} \end{bmatrix} = (2/3) \begin{bmatrix} \cos\theta & -\sin\theta & 0.5 \\ \cos(\theta - 120^0) & -\sin(\theta - 120^0) & 0.5 \\ \cos(\theta + 120^0) & -\sin(\theta + 120^0) & 0.5 \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (1)$$

The desired source currents in d-q components are obtained in equation (2) and (3).

$$i_{sd}^{*} = \overline{i_{Ld}} + i_{Cd} \quad (2)$$

$$i_{sq}^{*} = K_q \overline{i_{Lq}} + u i_{Cq} \quad (3)$$

where, $\overline{i_{Ld}}$ and $\overline{i_{Lq}}$ are the average values of the d- axis and q-axis components of the load currents, i_{Cd} is the output voltage of the DC voltage controller and i_{Cq} is the output of the AC voltage controller. u is the logical variable and its value equal to (i) zero if the power factor is to be regulated and (ii) one if bus voltage is to be regulated. Kq=1 in the latter case. The average values of i_{Ld} and i_{Lq} is obtained as the output of two identical low pass filters (LPFs) is given in equation (4).

$$\begin{bmatrix} \overline{i_{Ld}} \\ \overline{i_{Lq}} \end{bmatrix} = G(s) \begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} \quad (4)$$

where $G(s)$ is the transfer function of a 2nd order low pass filter with a corner frequency of 50 Hz. The reference for the source current is the d-q frame and first converted to the α-β frame and then to the a-b-c frame using the equations (5) and (6).

$$\begin{bmatrix} i_{s\alpha}^{*} \\ i_{s\beta}^{*} \end{bmatrix} = \begin{Bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{Bmatrix} \begin{bmatrix} i_{sd}^{*} \\ i_{sq}^{*} \end{bmatrix} \quad (5)$$

$$\begin{bmatrix} i_{sa}^{*} \\ i_{sb}^{*} \\ i_{sc}^{*} \end{bmatrix} = \sqrt{(2/3)} \begin{Bmatrix} 1 & 0 \\ -1/2 & -\sqrt{3}/2 \\ -1/2 & \sqrt{3}/2 \end{Bmatrix} \begin{bmatrix} i_{s\alpha}^{*} \\ i_{s\beta}^{*} \end{bmatrix} \quad (6)$$

Hence

$$\begin{bmatrix} i_{sa}^{*} \\ i_{sb}^{*} \\ i_{sc}^{*} \end{bmatrix} = \sqrt{(2/3)} \begin{Bmatrix} \cos(\omega t) & \sin(\omega t) \\ \cos\left(\omega t-(2\pi/3)\right) & \sin\left(\omega t-(2\pi/3)\right) \\ \cos\left(\omega t+(2\pi/3)\right) & \sin\left(\omega t+(2\pi/3)\right) \end{Bmatrix} \begin{bmatrix} i_{sd}^{*} \\ i_{sq}^{*} \end{bmatrix} \quad (7)$$

The reference for the source current vectors ($i_{sa}^{*}, i_{sb}^{*}, i_{sc}^{*}$) are compared and the desired compensator currents ($i_{Ca}^{*}, i_{Cb}^{*}, i_{Cc}^{*}$) are obtained as the difference between the load and the source currents are represented in equation (8).

$$\left.\begin{aligned} i_{Ca}^{*} &= i_{La} - i_{sa}^{*} \\ i_{Cb}^{*} &= i_{Lb} - i_{sb}^{*} \\ i_{Cc}^{*} &= i_{Lc} - i_{sc}^{*} \end{aligned}\right\} \quad (8)$$

3.2. Instantaneous Active and Reactive Current (IARC) Ttheory

A block diagram of the control approach is shown in Figures 3a and b is used for determination of the reference current vector.

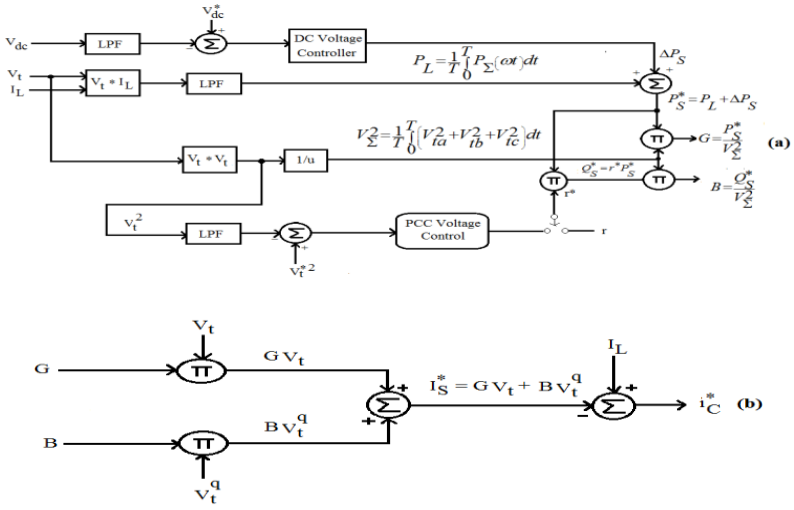

Figure 3. Block Diagram of IARC Controller (a) Computation of G and B (b) Generation of Reference Compensator Current

In this method, the vector reference source currents are represented in equation (9).

$$I_{s}^{*} = GV_{t} + BV_{t}^{q} \quad (9)$$

where 'G' and 'B' are defined in the equation (10).

$$G = P_{s}^{*}/V_{s}^{2}, \; B = Q_{s}^{*}/V_{s}^{2} \quad (10)$$

where P_S^* and Q_S^* are the average power and reactive power supplied by the source and are expressed in equation (11).

$$\left.\begin{aligned} P_S^* &= P_L + \Delta P_S \\ Q_S^* &= r^* P_S^* \end{aligned}\right\} \quad (11)$$

P_L and V_Σ^2 are defined by using equation (12).

$$P_L = \frac{1}{T}\int_0^T P_\Sigma(t)\,dt \quad (12)$$

$$P_L = \frac{1}{T}\int_0^T \left(V_t^T i_L\right)dt \quad (13)$$

$$V_\Sigma^2 = \frac{1}{T}\int_0^T \left(V_{ta}^2 + V_{tb}^2 + V_{tc}^2\right)dt \quad (14)$$

The voltage vector V_t^q is a unit vector that is orthogonal to V_t and thus satisfies the equation (15).

$$V_t^T V_t^q = 0 \quad (15)$$

There are two options for the choice of the reactive power or the ratio 'r' (i) Reactive power or power factor control. Here the reference value of 'r' is specified as

$$r^* = \tan\Phi_S^* \quad (16)$$

For unity power factor control, $r^* = 0$ (ii) PCC voltage control. Thus

$$r^* = \frac{KI}{s}\left[\left(V_t^*\right)^2 - V_t^2\right] \quad (17)$$

3.3. Proportional–Integral (PI) Controller

Block diagram of PI controller is depicted in Figure 4. Three-phase source voltage (V_{abc_s}) is continuously measured the control system and is compared with a reference voltage (V_{ref}) and generates a voltage error (V_{error}) signal. This error signal is given to the PI controller as an input, the PI controller process this error signal and produces an angle δ to drive the error to zero. From the phase-shift angle δ, the three-phase sinusoidal signal $V_{control}$ is obtained as:

$$V_{Control} = \left.\begin{aligned} V_a &= \mathrm{Sin}(\omega t + \delta) \\ V_b &= \mathrm{Sin}\left(\omega t + \delta - 2\pi/3\right) \\ V_c &= \mathrm{Sin}\left(\omega t + \delta + 2\pi/3\right) \end{aligned}\right\} \quad (18)$$

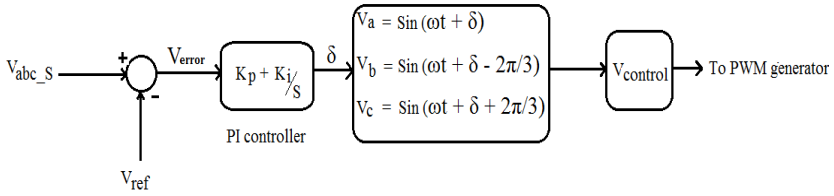

Figure 4. Block Diagram of PI Controller

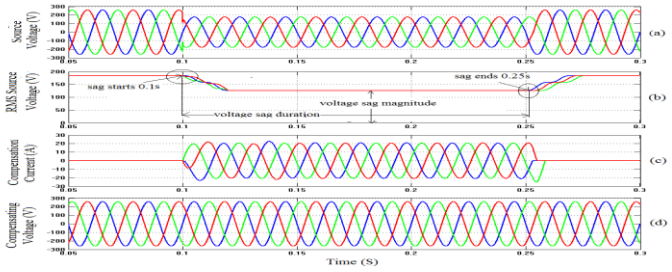

Figure 5. Voltage Sag under Linear Load with SRF Controller

In PWM generator, a sinusoidal signal is compared with a carrier signal and generates triggering pulses. This triggering or firing pulses are given to the gate terminal of the insulated gate bipolar transistor (IGBT) switches to switch on the VSI based DSTATCOM under voltage swell condition.

4. Simulation of DSTATCOM

Figure 1 shows the proposed configuration of the test system used to carry out the transient modeling and simulation of the DSTATCOM with the associated control strategies. This DSTATCOM model is simulated with the SRF, IARC and PI control techniques with simulation period 0.3 s.

5. Simulation Results and Discussion

In this section, simulation results of three control topologies used in three-phase four-wire DSTATCOM supplying two loads are presented. Load1 is considered as fixed resistive load (R-load) and load2 is considered as variable linear and nonlinear load. The variable linear load is taken as three-phase resistive-capacitive (R-C) whereas nonlinear load is realized by three-phase diode-rectifier with R-C load. Breaker 1 is used to control the period of operation of VSI-based DSTATCOM and breaker 2 is used to control the connection of a variable load to the distribution network. Initially, load 1 is connected to the network, but after a certain period of time load2 is switched on by closing the breaker2. Due to sudden addition of heavy load, voltage sag occurs in the source voltage. The objective of the simulation is to study three different performance aspects for voltage source inverter based DSTATCOM: (i) Voltage sag mitigation, by SRF control based DSTATCOM under linear and nonlinear load and (ii) Voltage sag mitigation, by IARC control based DSTATCOM under linear and nonlinear load and (iii) Voltage sag mitigation, by PI control based DSTATCOM under linear and nonlinear load.

5.1. Performance of SRF Controlled DSTATCOM for Voltage Sag Mitigation under Linear Load

Due to sudden addition of heavy load by closing breaker2, a three-phase voltage sag occurs in the source terminal of the distribution network. For balanced voltage sag of 60%, the source voltage signal before compensation, the compensation current, the load voltage after voltage sag compensation is depicted in Figures 5a to c. As Figure shows, the proposed SRF

control based voltage sag compensator restore the voltage on the load side by injecting proper compensating current in each phase so that the load voltage remains at the desired level.

The performance of SRF control based uncompensated and compensated load voltages under linear load are shown in Figure 6. As the Figure shows when the compensator is connected, it minimizes the effect of voltage sag so that voltage at the load terminal reaches rapidly to the normal level.

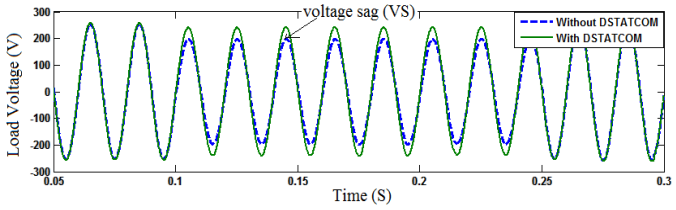

Figure 6. Load Voltage without and with DSTATCOM

6.2. Performance of SRF Controlled DSTATCOM for Voltage Sag Mitigation under Nonlinear Load

Figures 7a to c depicts the simulation results of SRF controlled DSTATCOM under voltage sag condition with a nonlinear load. In this case, the three-phase source voltage magnitude decreased to 34% of the normal level for the duration of 0.24 s. Then voltage recovers to its normal level. As it can be observed from the simulation results, the SRF control based DSTATCOM is able to generate the desired current components for three-phases rapidly and helps to maintain load voltage sinusoidal at the normal value.

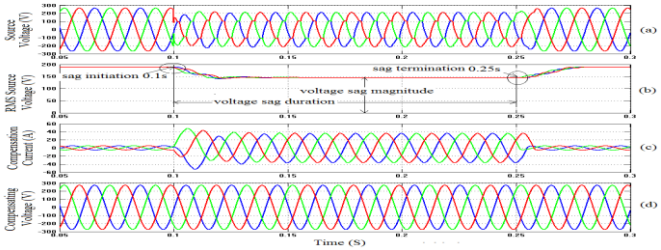

Figure 7. Voltage Sag under Nonlinear Load with SRF Controller

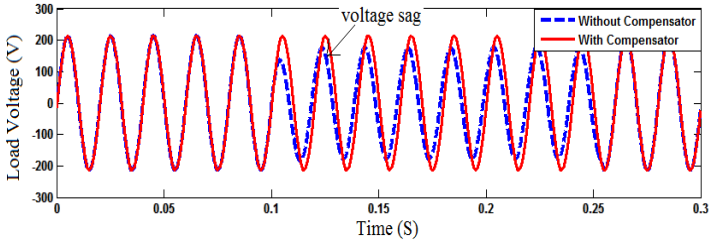

Figure 8. Load Voltage with and without Compensator with SRF Controller

Figure 8 shows the load voltages with and without the compensator. As the graph shows when the compensator is connected, voltage sag has totally eliminated. This can be resolved by injecting the appropriate amount of current to the distribution network under voltage sag conditions.

6.3. PerformancE of IARC Controlled DSTATCOM for Voltage Sag Mitigation under Linear Load

A three-phase balanced voltage sag of magnitude 60% occurs in the source terminal of the distribution network from 0.01 to 0.25s. Then the source voltage signal recovers to its normal levels. For balanced voltage sag of 60%, the source voltage signal before compensation, the compensation current, the load voltage after voltage sag compensation is depicted in Figures 9a to c. As Figure shows, the proposed IARC control based DSTATCOM restore the voltage on the load side by introducing the exact amount of compensating current in each phase so that the load voltage remains at the acceptable level.

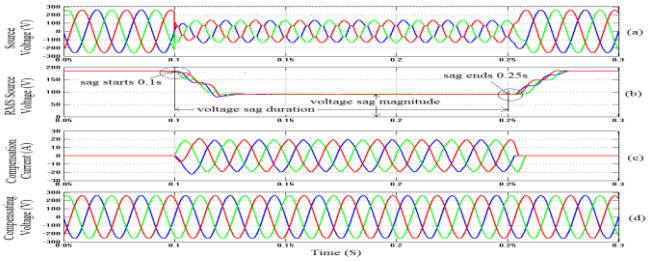

Figure 9. Voltage Sag under Linear Load with IARC Control

Figure 10 shows the load voltages under nonlinear load conditions with and without voltage sag compensator. As the graph shows when SRF controlled DSTATCOM is added to the distribution system, it produces required amount of compensation current in each phase rapidly, so that voltage sag is totally disappeared and load voltage becomes sinusoidal.

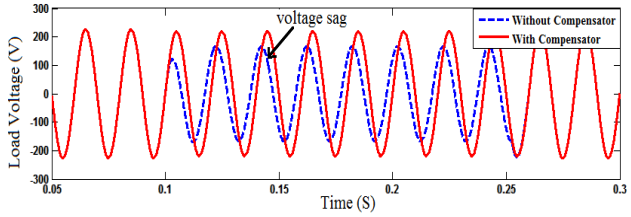

Figure10. Load Voltage with and without DSTATCOM by IARC Controller

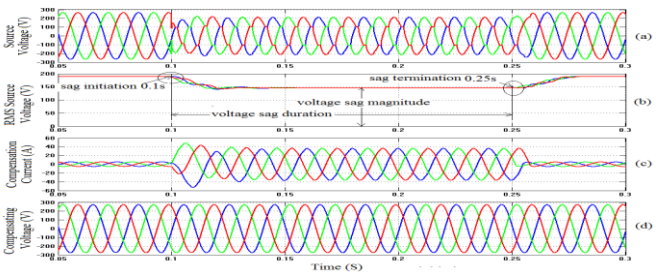

Figure 11. Voltage Sag under Linear Load with IARC Control Scheme

6.4. Performance of IARC Controlled DSTATCOM for Voltage Sag Mitigation under Nonlinear Load

Figures 11a to c shows the simulation results of IARC control based voltage sag compensator with a nonlinear load. In this case, the three-phase voltage sag of magnitude 54% has happened in all phases at 0.15 s duration. Then the voltage recovers to its normal level. As

it can be observed from the simulation results, the IARC control based voltage sag compensator is able to produce the required current components for three-phases rapidly and helps to maintain load voltage balance and sinusoidal at the normal value.

The performance of IARC control based uncompensated and compensated load voltages under linear load are depicted in Figure 12. As the Figure shows when the DSTATCOM is connected, it produces compensating current so that voltage sag is completely eliminated and load voltage becomes normal level.

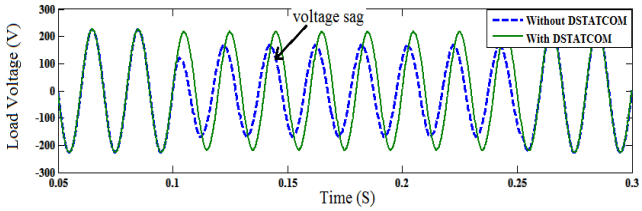

Figure12. Load Voltage with and without Compensator by IARC Controller

6.5. Performance OF PI Controlled DSTATCOM for Voltage Sag Mitigation under Linear Load

Figures 13a to c shows the simulation results of PI controller based DSTATCOM with a linear load. In this case voltage sag of 45% has happened in all the three-phases, which starts at t=0.10 s and ends at t=0.25 s. From the Figures 13b and c it is observed that PI controller based DSTATCOM is able to produce the required current components for three-phases and helps to maintain load voltage sinusoidal at the normal level.

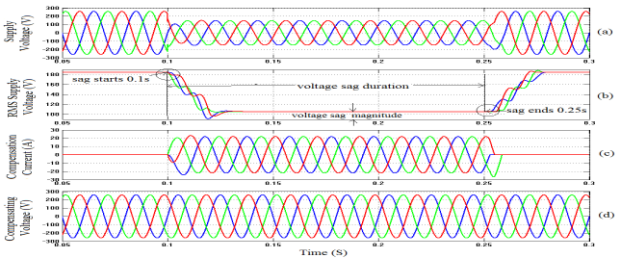

Figure 13. Voltage Sag under Linear Load with PI Control Scheme

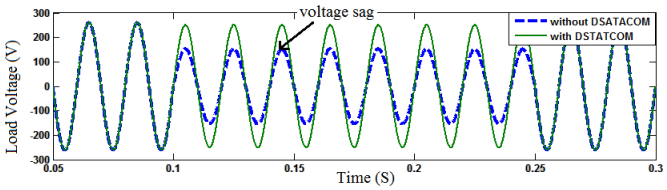

Figure 14. Load Voltage with and without DSTATCOM

Figure 14 shows the compensating voltages under linear load with and without voltage sag compensator. As it can be seen, after the voltage sag compensator connected, voltage sag totally disappears and load voltage recovers their normal value.

6.6. Performance of PI Controlled DSTATCOM for Voltage Sag Mitigation under Nonlinear Load

A three-phase balanced voltage sag of magnitude 52% occurs in the source terminal of the system from 0.10 to 0.25s. For balanced voltage sag of 52%, the source voltage signal

before compensation, the compensation current, the load voltage after voltage sag compensation is depicted in Figures 15a to c. As Figure shows, the proposed PI control based DSTATCOM restore the voltage on the load side immediately by injecting required amount of compensating current in each phase so that the load voltage remains at the acceptable level.

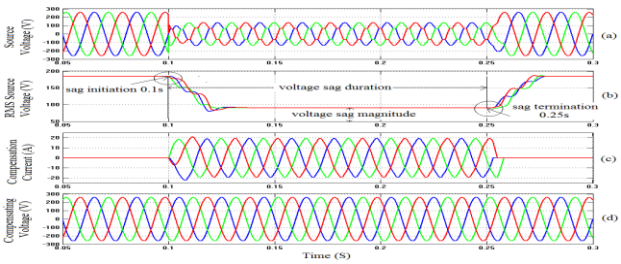

Figure15. Voltage Sag under Nonlinear load with PI Control Scheme

Compensated and uncompensated load voltages under nonlinear load are depicted in Figure 16. As the graph depicts when the voltage sag compensator is connected, voltage sag at the load terminal completely mitigated and load voltage becomes normal level.

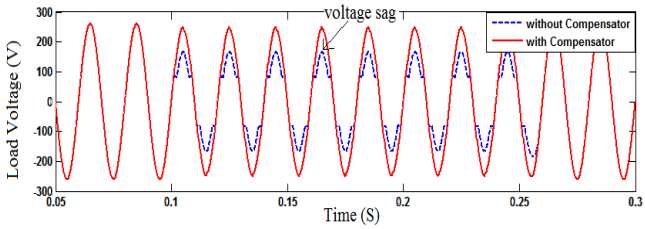

Figure 16. Load Voltage with and without Compensator under Nonlinear Lload with PI Controller

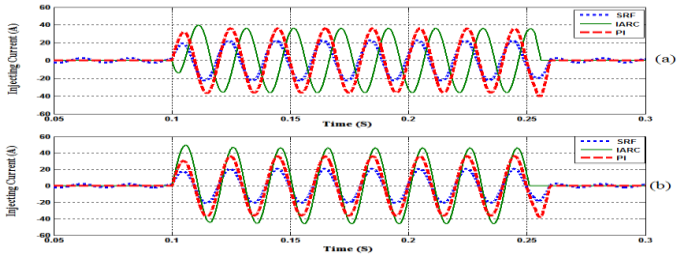

Figure 17. Comparison of Compensation Current under SRF, IARC and PI control techniques (a) Linear Load and (b) Nonlinear Load

Figures 17a and b show the performance comparison of SRF, IARC and PI control based DSTATCOM for generation of compensation current under linear as well as nonlinear loads. The short duration voltage sag alleviation capability of the DSTATCOM depends on current injection capability of the device during the voltage sag period. From the graph, it is highlighted that, during the voltage sag IARC and PI control based DSTATCOM generates the highest amount of compensation current compared to the SRF controller during linear load, but in the case of nonlinear load only IARC controller produces the highest amount of compensation current compared to SRF and PI controller.

7. Analysis of Simulation Results

Comparative evaluations of three different control schemes are shown in table 1. It can be noted from table 1 that IARC and PI control methods are simple with respect to computational complexity because it does not require any transformation (Parks and Clarks). The IARC control method shows excellent performance to mitigate the voltage sag of magnitude 60% and 54% under linear as well as nonlinear load conditions. On the other hand SRF and PI control based DSTATCOM mitigate voltage sag of magnitude 60% and 45% under linear load and 34% and 52% under nonlinear load.

Table 1. Comparison of SRF, IARC and PI Control Strategies

Parameters	Various Control Techniques		
	SRF Controller	IARC Controller	PI Controller
Computational complexity	It requires complex transformation	It does not require complex transformation	It does not require complex transformation
Phase locked loop (PLL)	It requires PLL	It does not require PLL	It does not require PLL
Voltage Sag mitigation	Good	Excellent	Good
Injecting Current	Small	High	Small compar to IARC

8. Conclusion

In this work, a comparative analysis of three different control schemes for DSTATCOM installed in three-phase four wire distribution systems has been presented. The performance of these control techniques has been analyzed for voltage sag mitigation using time-domain MATLAB/Simulink software under three-phase linear and nonlinear load conditions. In contrast, SRF theory needs additional PLL circuit for calculation of angle 'θ 'whereas in IARC and PI control method angle 'θ' is directly calculated from main voltages. IARC and PI controllers are simple as it does not require Clarks or Parks transformation. The obtained simulation results from SRF, IARC and PI control schemes are excellent or even slightly better in IARC control in compared with SRF and PI control.

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