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A Novel Generalized Topology for Multi-level Inverter with Switched Series-Parallel DC Sources

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Abstract

This paper presents a novel topology of Single-phase multilevel inverter for low and high power applications. It consists of polarity (Level) generation circuit and H Bridge to generate both positive and negative polarities. The proposed topology can produce more output voltage levels by switching dc voltage sources in series and parallel. The proposed topology utilizes minimum number of power electronic devices which leads to the reduction of cost, size, and weight low and consumes low power which improves the efficiency. Switching pulses are generated using Phase disposition (PD) pulse width modulation technique. Finally the effectiveness of the proposed topology is verified using MATLAB/SIMULINK software tool. 7level asymmetrical multilevel inverter prototype hardware is prepared to support the proposed topology to verify the effectiveness and its validity.

Keywords: *multi-level Inverter, series-parallel switches, isolated DC sources, phase disposition (PD) PWM*

1. Introduction

Introduction of the multilevel inverters was done in 1975 and initiated with three level inverter [1]. Many sources of dc voltage are synthesized to obtain a staircase identical to sinusoidal output voltage waveform. In the recent day MLI is gaining much fame in the field of DC/AC conversion due to less THD, better power quality and good electromagnetic compatibility.

Even after having many merits MLI has few demerits that is to maximize output voltage levels semiconductor switch requirements with peripheral devices like protection circuits, gate driver circuits used extensively .Due to more device count the overall system becomes expensive ,stupendous and complicated and minimizes the quality and competency of the converter [2].

MLI are grouped into Cascaded H Bridge, Flying capacitor and Neutral point Clamped traditionally. Cascaded H Bridge is popular due its coherence and easy operation but the limitation of the topology is requirement of isolated dc power supplies [3]. CHB is arranged as asymmetric and symmetric configuration based on magnitude of the dc voltage sources. If Vdc1≠Vdc2≠Vdc3 is asymmetric vice versa. For the same number of power switches the asymmetric configuration of CHB generates more number of voltage levels as compared with symmetric configuration.

The requirement of large number of bidirectional switches is a major issue in asymmetrical topologies. An effort has been attempted to reduce bidirectional switches in asymmetrical topology by proposing a new topology in this paper.

The possibility of connecting two or more sources in series and parallel gives enough flexibility for meeting voltage/power requirements in the vehicle drive systems [4].

In this paper the concept of series/parallel connected dc voltage sources based on the basic topology presented in [12] is extended. The proposed topology requires only one bidirectional switch.

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Batteries, capacitors and isolated dc voltage supplies can be used as dc voltage sources in the proposed topology [5]. When ac voltage sources are available using rectifiers and isolated transformers multiple dc voltage sources can be produced [6]. The problem of voltage balancing is eliminated by employing fixed dc voltage source [7].

2. Cascade H Bridge Multi-Level Inverter Topology

In the family of Multi level inverter conventional cascaded multi-level inverter is the most influencing topology [8]. The cascade topology allows several dc voltage sources to synthesize a desired ac voltage, which require least number of components as compared to diode clamped and flying capacitor multi level inverters and no specially designed transformer is needed as compared to multi pulse inverter [9]. A cascade multi level inverter consist of number of H bridge inverter units with separate DC voltage sources for each unit. The full bridge topology is shown in Figure 1. is used to synthesize three unique output voltages (+V_{dc}, -V_{dc} and zero) by connecting dc voltage source to ac output side by different combination of the four switches S_{11}, S_{12}, S_{13} and S_{14} .

The overall output voltage given by:

$$V_0 = V_{dc1} + V_{dc2} + \ldots\ldots\ldots\ldots + V_{dcn} \quad (1)$$

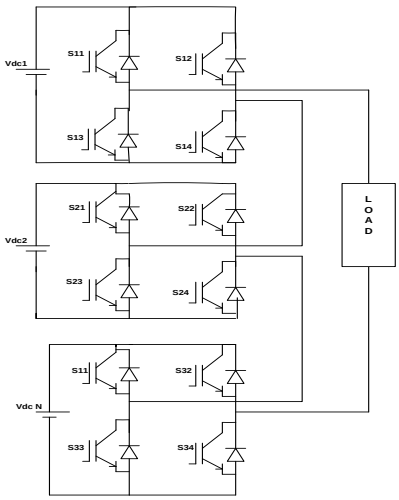


Figure 1. Conventional cascaded multi-level inverter

If all the voltage sources are equal then is referred as symmetrical ($V_{dc1} = V_{dc2} = V_{dcn}$) otherwise known as asymmetrical ($V_{dc1} \neq V_{dc2} \neq V_{dcn}$) cascaded multi-level inverter.

2.1. For Symmetrical Cascaded Multi-level Inverter

The number of output voltage steps (Nsteps) for “m” number of separate dc voltage sources (batteries or PV cells) in symmetrical cascaded MLI is given as:

$$Nstep = 2 \times m + 1 \quad (2)$$

For m = 1; 3steps
m = 2; 5steps.

The attained maximum output voltage with ‘m’ number of dc voltage sources in symmetrical cascaded multi level inverter is equal to m*V_{dc}.

2.2. Asymmetric Cascaded Multi level Inverter

For asymmetric cascaded MLI, the dc voltage sources of different cells are not equal. Asymmetrical cascaded H Bridge MLI produces more output voltage levels for the equal number cells than its symmetric.

If the separate dc voltage sources shown Figure 1 are chosen according to a geometric progression with the factor of 2 or 3.

For “n” cascaded H Bridge MLI the number of voltage steps in asymmetrical cascaded H Bridge MLI is given as:

$$Nstep = 2^{m+1} - 1 \quad if\ Vj = 2^{j-1} Vdc \quad for\ j = 1,2,...m \tag{3}$$

$$Nstep = 3^{m+1} - 1 \quad if\ Vj = 3^{j-1} Vdc \quad for\ j = 1,2,...m \tag{4}$$

The maximum output voltages of these ‘m’ cascaded multi-level inverter.

$$Vo\max = (2^m - 1) Vdc \quad if\ Vj = 2^{j-1} Vdc\ for\ j = 1,2,3..m \tag{5}$$

$$Vo\max = \left(\frac{3^m - 1}{2}\right) Vdc\ if\ Vj = 3^{j-1} Vdc\ for\ j = 1,2,3..m \tag{6}$$

Comparing the equation (2)-(6) it can be observed that asymmetrical cascaded H Bridge multi level inverters can produce more output voltage steps and higher maximum output voltage with the same number of bridges.

3. Basic Topology

The recommended basic structure in [10] shown in Figure 2. Consist of three power switches Sa1, Sb1,Sc1 and two dc voltage sources every switch is composed with an IGBT with anti parallel diode. When switch sc1 is ON the output voltageV0=V1, when switch Sb1 is ON output voltage Vo=V2, when Sa1 is ON output voltage Vo=V1+V2 and when Sb1 and Sc1 is ON output voltage Vo=V1-V2, if V1≠V2 due to short circuit of dc voltage sources huge value of circulating current will be circulated, to avoid this the dc voltage sources magnitudes should be identical (V1=V2).Care must be taken when sa1 is conducting Sb1 or Sc1 should not turn ON vice versa.

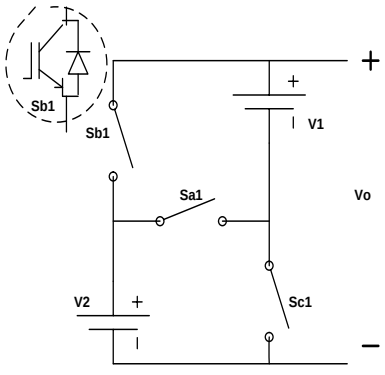


Figure 2. Basic Cell proposed in [10]

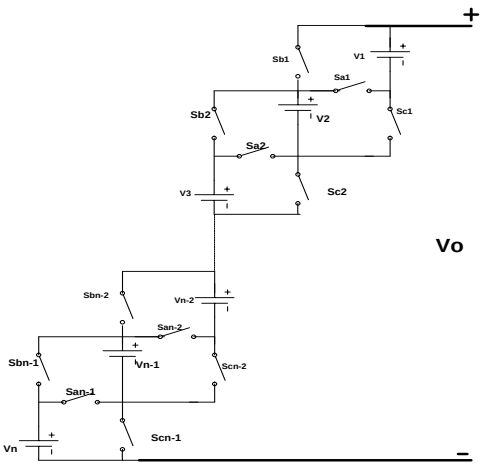


Figure 3. Extended Unit proposed in [10]

In the Figure 3 the switching devices should be selected carefully due to voltage across each switch is selected differently. The voltage across the switchesSa1-San-1, Sb1-Sbn-1 and Scn-Scn-1 during their OFF state are VSa1-VSan-1, VSbn-VSbn-1 and VSc1-VScn-1, which satisfy:

VSa1 =VSa2=……VSan-1
VSb1 =VSb2=……VSbn-1
VSc1 =VSc2=……VScn-1

These switches voltages will come to lesser and lesser comparing with the output voltage when number of steps increased. The IGBTS and MOSFETS are sufficient for these switches because these switches are operated at twice the frequency of the reference waveform.

The Voltages of the switches in H Bridge during OFF state are Vs1-Vs4 which satisfy:

$$VS1 = VS2 = VS3 = VS4 = \sum_{k=1}^{m} Vk \quad (7)$$

The voltage of the above switches becomes approximately equal to the output voltage therefore the switching frequency these switches becomes equal with the reference waveform. Therefore insulated Gate Bipolar transistors (IGBT) can be preferred for these switches.

4. Proposed Topology

The basic cell of proposed topology [10] is modified to generate more output voltage steps with minimum switches, a new topology is proposed in this paper and verified by implementing prototype hardware 7level asymmetrical topology. The proposed topology shown in Figure 4. The topology is composed with two dc voltage sources V1 and V2 along with level generation circuit ,it consist high frequency switches and should withstand to high switching frequency to produce required voltage levels and H Bridge circuit, is responsible for the conversion of the polarity of the output voltage, is the low frequency part operating at line frequency. Using basic cell positive voltages are generated shown in Figure 5(a). S1, S2,S3 and S4 forms the H Bridge which gives both positive and negative pulses shown in Figure 5(b). The proposed topology can be easily extended by connecting basic cells in series and connected across the H Bridge. A 16 level asymmetrical cascaded H Bridge shown in Figure 6(a) of the proposed topology. Generalized topology of the proposed topology shown in Figure 6(b).

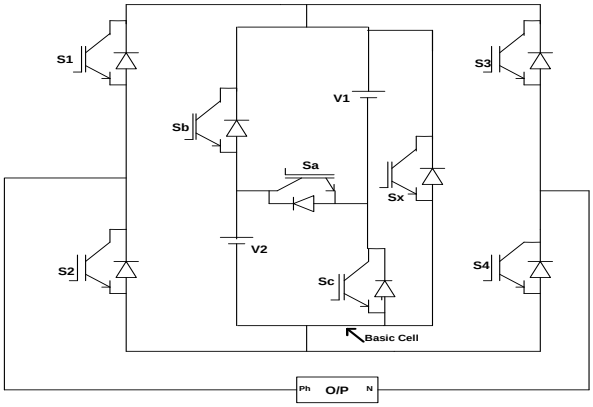


Figure 4. Proposed Topology

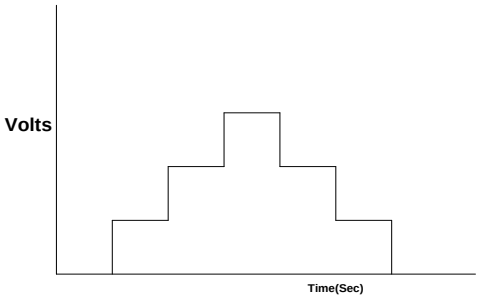


Figure 5(a). Basic Cell Output

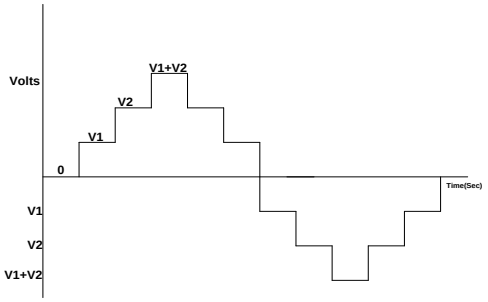


Figure 5(b). Output voltage waveform

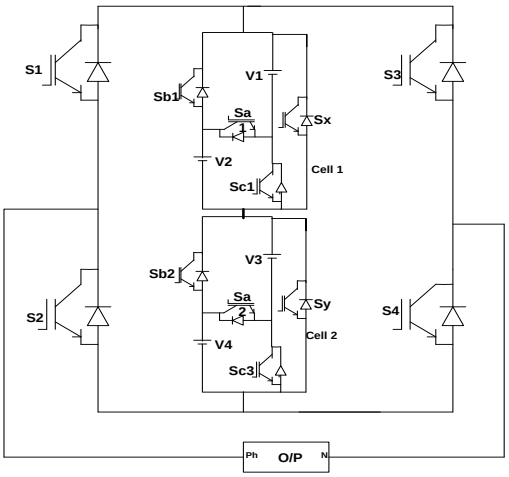


Figure 6(a). Proposed 16Level Asymmetrical Cascaded H Bridge MLI Topology

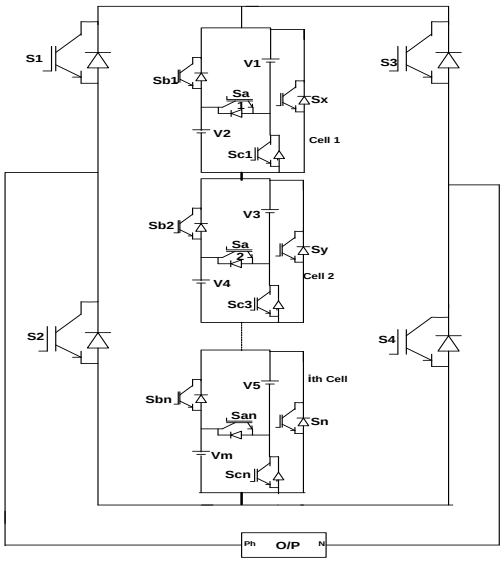


Figure 6(b). Generalized Topology of the proposed Cascaded Bridge MLI Topology

The proposed method is different from the methods presented in [1]-[8].

The values of the dc voltage sources employed in the asymmetrical MLI are assumed differently in the different cells such that maximum output voltage levels can be produced using lesser switching devices.

1) The magnitude of the dc voltage sources can be selected using following equation, For the i_{th} cell, the value of the m_{th} dc voltage source.

$$Vdcm,i = 2^{(m-1)}Vdc \quad (8)$$

For cell 1 consisting of 2 voltage sources Vdc1&Vdc2.

ie i=1, m=1 ;Vdc1,1 = Vdc

For i=1, m=2 ; Vdc2,1 = 2Vdc

For cell 2contains Vdc3 &Vdc4

For i=2 , m=3 Vdc3,2= 2^2Vdc= 4Vdc

For i=2 , m=4, Vdc4= 2^3Vdc= 8Vdc

2) For the i^{th} cell The output voltage levels(N_{level})can be determined by the following equation:

$$N\,level = 2^{2i} \quad ; \quad where\,'i'\ is\ cell\ number \quad (9)$$

$$N\,level = 2^{2i} \quad ; \quad where'i'\ is\ \ cell\ \ number \tag{9}$$

For i=1 ; 2^2 =4 levels
i=2 ; 2^4=16levels
i=3 ; 2^6=64 levels.

c) The total number of IGBTs (N_{IGBT}) required calculated using the following equation:

$$NIGBT = 4i + 4\ ; \tag{10}$$

For, i=1; 4+4=8 IGBTs
i=2; 4*2+4=12
i=3; 4*3+4=16,

d) The maximum output voltage is obtained by the i^{th} cell of the proposed topology can be determined as follows;

$$The\ MaxmumOutputVoltageVo\max = (2^{2i} - 1)Vdc \tag{11}$$

For cell 1 i.e. i=1; 3Vdc
i=2; 15Vdc
i=3; 65Vdc.

Switching States of the proposed 7 level asymmetrical cascaded MLI shown in Table1.

Table 1. Output Voltages and Switching Sequence of the Proposed 7 Level Inverter

Level	**0**	**1**	**2**	**3**
Switching Sequence	Sx	Sc	Sb	Sa
Output voltage	0	V_1	V_2	V_1+V_2

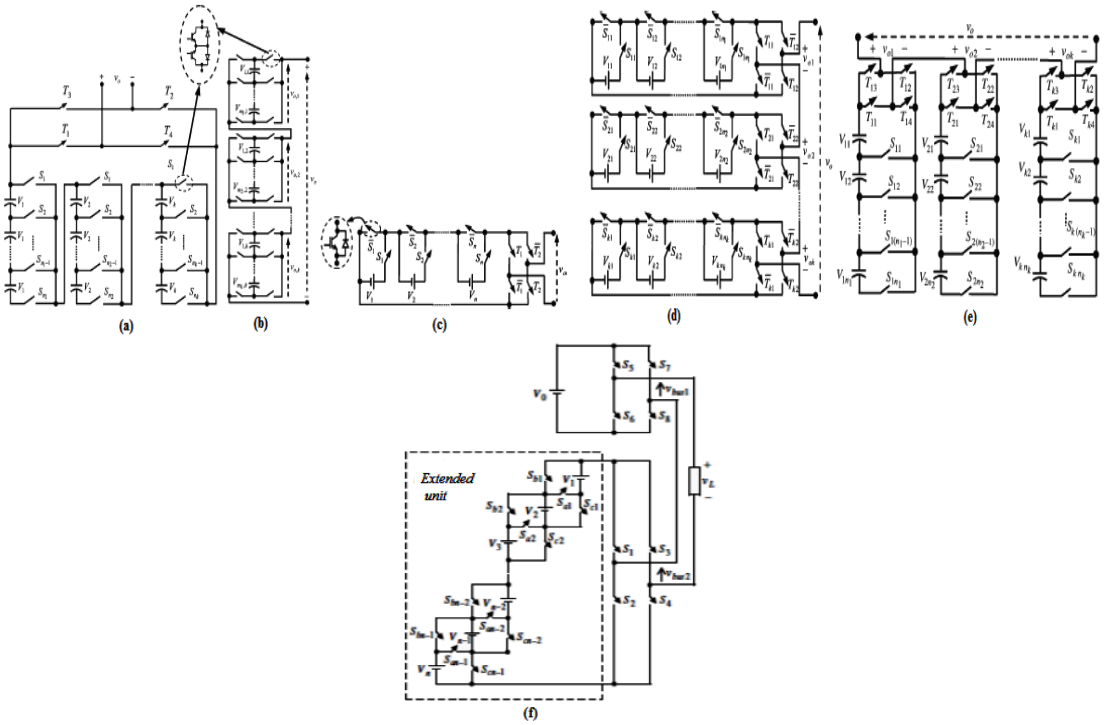


Figure 7. Various Topologies presented in a[3], b[4], c[5], d[6], e[7], f[8]

5. Modulation Methods

Many modulation strategies are possible for multi level inverters. Phase disposition (PD) PWM technique is employed for generating switching pulses .This technique is derived from the triangular carrier that has individually the lowest switching frequency among the multi level PWM method and it provides low harmonic distortion and can be easily extended to any level.

5.1. Phase Disposition (PD) PWM Method

In Phase disposition (PD) pulse width modulation technique all carriers are arranged in phase. Figure 8 illustrates reference and carrier wave forms for the 7 level asymmetrical cascaded H Bridge of the proposed topology. Phase disposition modulation has lowest line to line harmonic voltages [11]. Phase disposition modulation places significant harmonic energy in to a carrier component in each phase leg and then relies on common mode cancellations between the phase legs to eliminate this harmonics from the line to line output voltage. Figure 8 shows carrier and reference wave arrangements in PD modulation technique. Switching pulses generated using simulink shown in Figure 9.

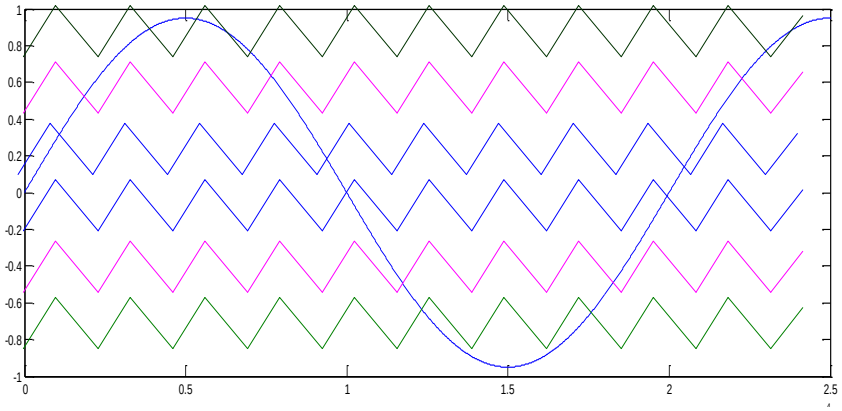


Figure 8. Carriers arrangement in phase Disposition PWM

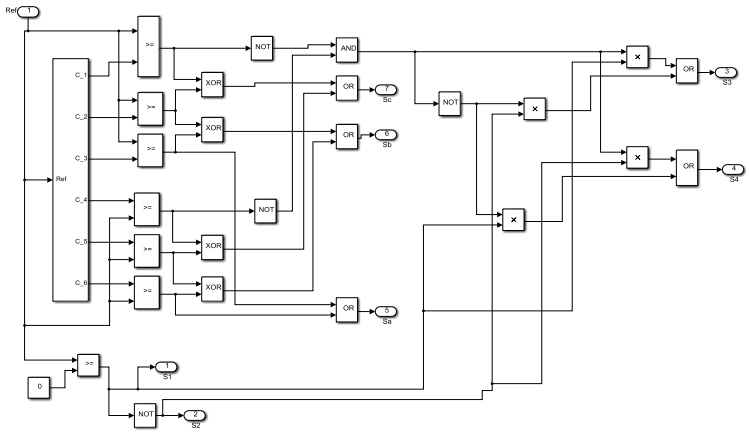


Figure 9. Simulation circuit for generating Switching pulses

6. Comparison of the other Topologies with the Proposed Topologies

To investigate the performance analysis it is also compared with other different multi-level inverter topologies presented in [3-8]. As the number of switches used in generating voltage levels plays vital role in determining the complexity, cost of the multi-level inverter and efficiency. A comparison is made on the basis of number of switches used against output voltage levels produced.

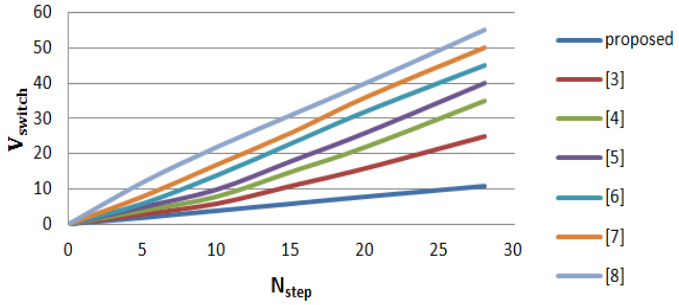


Figure 10. Copmarision of Switches against output voltage steps of proposed topology with topologies presented in [3]-[8]

It shows from the Figure 10 that the topologies presented [3-8] have the almost equal number of switches but they produce unequal number of voltage steps this is due to their arrangement of dc voltage sources and are considered only series and in some topologies both series and parallel connection also considered. In the proposed topology the basic cell is connected in such way that more number of output voltage levels can be generated dc voltage sources connected in series with all possible combinations of other voltage sources, results in increased voltage levels causing waveforms to look like discrete sinusoidal waveform of very low THD.

7. Simulation Results

To conform and validate the effectiveness of the proposed topology simulation has been carried out using matlab/simulink. Phase disposition(PD) Pulse width modulation techniques is employed for switching pulse generations with carrier frequency of 5KHz and 10KHz, where as reference signal frequency is kept at 50Hz.

The proposed topology is simulated using matlab/simulink by constructing 7 level asymmetrical topology. The simulated output voltage and current waveforms shown in Figure 10.

FFT analysis of the voltage and current wave forms of the proposed topology shown in Figure 11. It was observed that the total harmonic distortion for the voltage is 21% and for the current wave form is 3.41%.

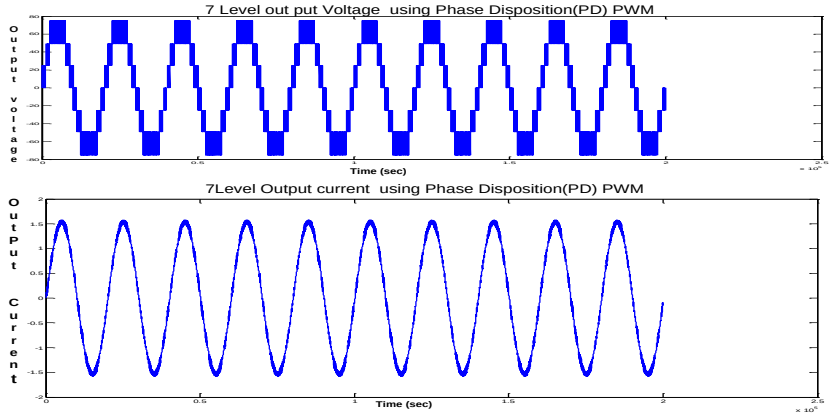


Figure 10. Simulated output voltage and current waveforms of the proposed topology 7level cascaded H bridge MLI

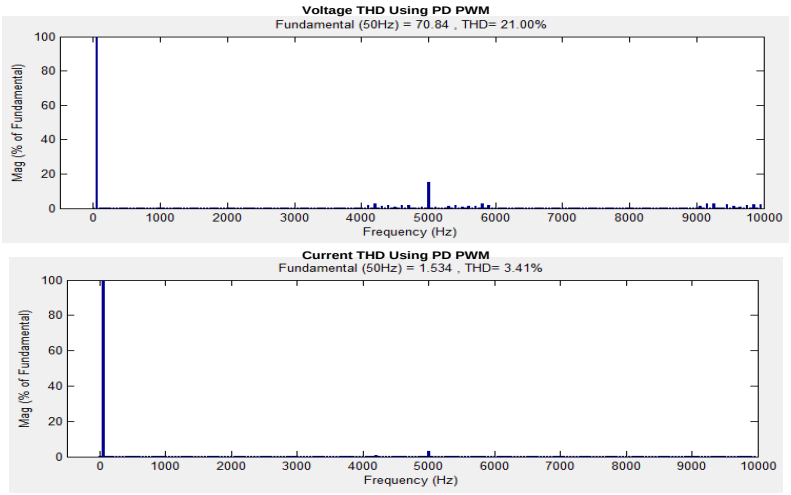


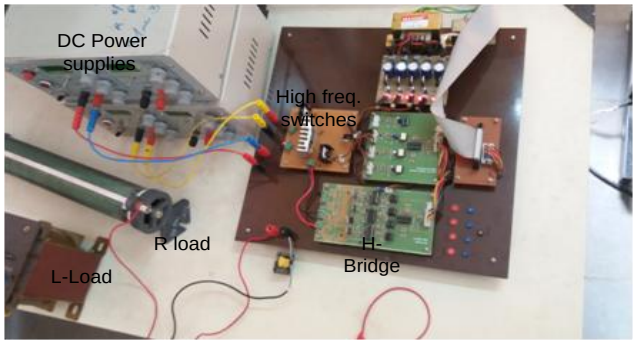
Figure 11. FFT analysis of Voltage and Current wave forms of the Proposed topology for 7 level asymmetrical cascaded H Bridge MLI

8. Experimental Results

To approve and ensure the concept and feasibility of the proposed topology experimental setup has been prepared for 7 levels of output voltage and validated experimentally with R-L load (R=50Ω and L=55mH) shown in Figure 12. Switching pulses for H Bridge (S1 & S4) shown in Figure 13, for high frequency switches (Sa, Sb,Sc &Sx) are generated using Phase Disposition (PD) shown in Figure 14.

An IRF840 MOSFETS, FIO5012Bidirectional IGBT is used for high frequency switching, IRF840 MOSFETS for H-Bridge is used for low frequency switching, IR2110 ICs are used in Driver circuit, 4584 ICs for NOT gate and 4081 ICs for AND gate are used for Boolean operations. Each switch requires an isolated driver circuit 6N137, TLP250 Opto isolators used as isolated driver circuit for each switch and it can work in a wide range of pulse width but isolated power supply is required for each switch. 7815, 7805 regulator ICs are used for 15Volts and 5Volts supply, 2W10 bridge rectifier is to convert AC into DC, SPARTRAN 3A DSP trainer is used for driving the gate signals.

The experimentally obtained voltage and current wave forms for the proposed 7 level asymmetrical topology using PD modulation shown in Figure 15 & Figure 16. It was observed that simulated and experimentally obtained results are matching with each other.



Hardware implementation of proposed 7level asymmetric MLI

Figure 12. Experimental setup for the 7 level asymmetrical cascaded H bridge MLI of the proposed topology

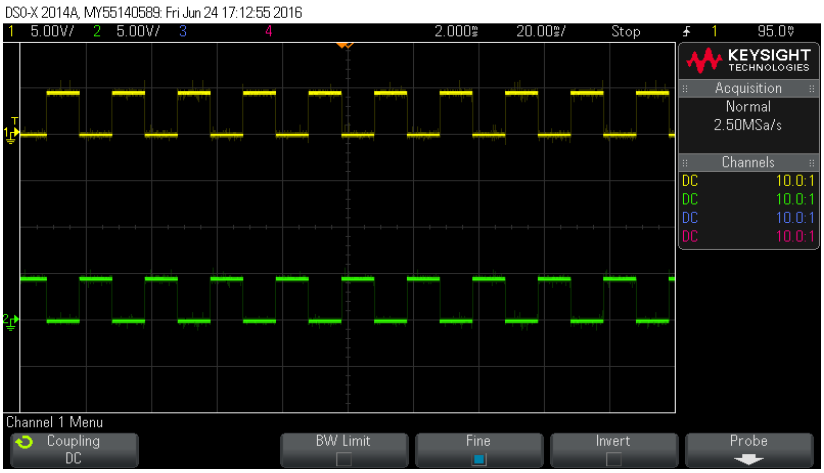


Figure 13. Switching Pulses for S1 and S4

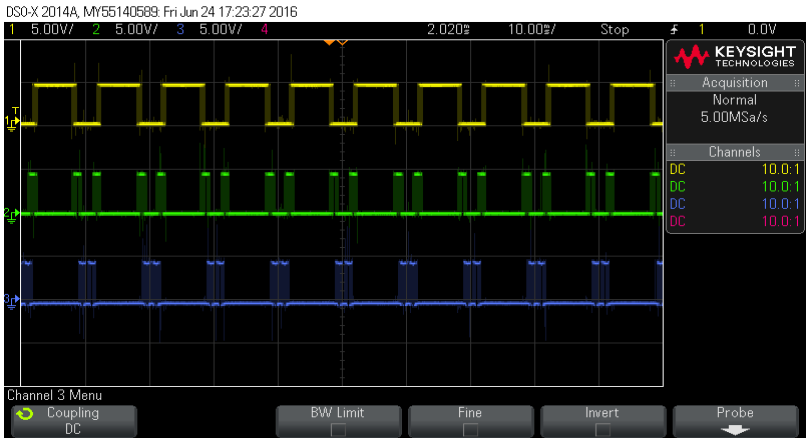


Figure 14. Switching pulses for switches Sa, Sb, Sc, & Sx

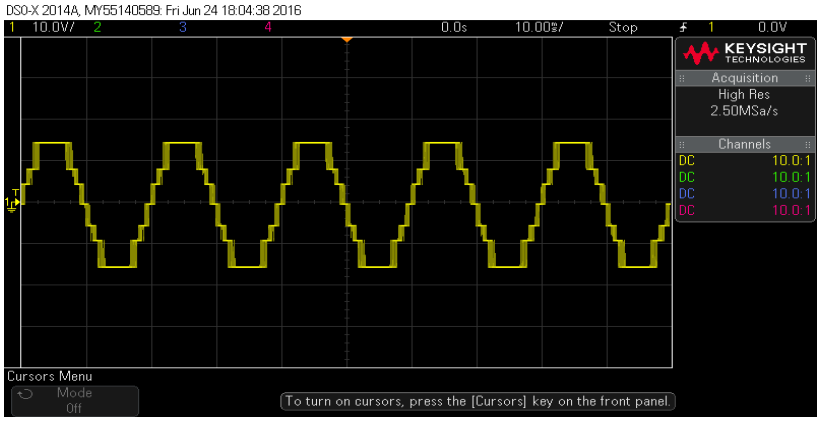


Figure 15. Experimental output voltage of the 7 level cascaded H Bridge MLI of proposed topology

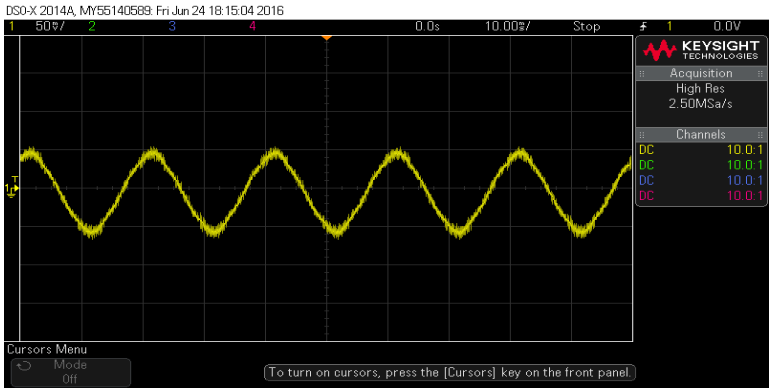


Figure 16. Experimental output current of the 7 level cascaded H Bridge MLI of proposed topology

9. Conclusion

In this paper a new structure for the improvement of the cascaded H bridge multilevel inverter presented in [10] that operates on the base of the series and parallel connections of the dc voltage sources was presented. In the proposed topology the series connection of the basic cell and capability of the series connection of the dc voltage sources increase the number of voltage levels. The ability of the proposed topology was tested by simulation and experimental of a 7 level inverter based on proposed topology.

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