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Design procedure and digital control of a DCM flyback converter: component sizing and experimental validation

Nabil Abouchabana, Mohammed Benmiloud, Khaled Ameur, Aboubakeur Hadjaissa
LACoSERE laboratory, Faculty of Technology, Amar Telidji University of Laghouat, Laghouat, Algeria

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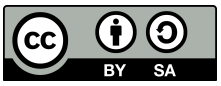
ABSTRACT

Flyback converters are widely used in low-power switch-mode power supplies (SMPS) due to their simple structure, galvanic isolation capability, and cost-effectiveness. This paper presents a systematic design methodology and digital Proportional–Integral (PI) control implementation for a discontinuous conduction mode (DCM) flyback converter using a dSPACE 1104 control platform. The proposed approach integrates magnetic component sizing, semiconductor stress evaluation, and RCD snubber design into a unified workflow. A 30 W prototype operating at 30 kHz with an input range of 20–30 V and a regulated 12 V output was developed and experimentally validated. The digital PI controller was tuned using Takahashi's method to ensure stable voltage regulation. Experimental results demonstrate proper DCM operation and stable output regulation under input voltage variation (20–30 V), load variation (48 Ω–12 Ω), and reference changes (10–14 V). The measured efficiency exceeded 90% at nominal operating conditions. The results confirm the effectiveness of the proposed design methodology for low-power isolated DC–DC applications.



Corresponding Author:

Nabil Abouchabana
LACoSERE laboratory, Faculty of Technology, Amar Telidji University of Laghouat
37G Ghardaia Road, 03000, Laghouat, Algeria
Email: n.abouchabana@lagh-univ.dz

1. INTRODUCTION

Flyback converters are widely used in low-power switch-mode power supplies (SMPS) when galvanic isolation and, in some cases, multiple isolated outputs are required [1]-[3]. They are commonly employed in battery-powered systems, industrial control electronics, and auxiliary power supplies [4], [5]. Various DC–DC converter topologies such as buck, boost, SEPIC, and flyback are extensively employed in renewable energy harvesting and power conditioning applications, where trade-offs between efficiency, complexity, and isolation must be considered [6], and specialized control methods, such as pulse density modulation in DCM flyback designs, have been explored in practical electronics applications [7].

Flyback converters operate either in continuous conduction mode (CCM) or discontinuous conduction mode (DCM), depending on whether the magnetizing current reaches zero during the switching period [5]. For low-power applications, DCM is often preferred because it can offer improved efficiency at light load, reduced magnetic component size, and simplified control design under certain operating conditions [4], [5], [8], [9]. In addition, DCM operation avoids the right-half-plane zero associated with CCM operation and is therefore attractive for digitally controlled implementations and compact power supplies [1]-[5], [8]-[10].

Although the theoretical analysis of flyback converters is well documented in the literature [1], [2], [5], these works mainly provide theoretical analysis and general design guidelines [11]. For example, DCM flyback converter designs with specific modulation strategies for automotive LED drivers have been reported [7], but comprehensive design workflows integrating transformer design, snubber design, and digital control validation remain limited [11]. In contrast, the present study focuses on a complete and experimentally validated design workflow for a DCM flyback converter, integrating magnetic component sizing, semiconductor stress analysis, RCD snubber design, and digital PI control implementation.

In particular, leakage inductance can generate significant voltage stress across the switching device, which motivates the use of RCD snubber circuits as discussed in application-oriented design guidelines [12]. Furthermore, while digital control of DC–DC converters has been widely investigated, including efficiency optimization in digitally controlled flyback converters [9], many existing studies address either theoretical modeling or individual design aspects without presenting a complete experimentally validated workflow. Therefore, there is a need for a practical design methodology that links analytical design procedures with full hardware implementation of DCM flyback converters. In such converters, the transformer plays a central role in determining efficiency and output regulation performance [1], [8], [10].

A successful implementation requires careful parameter calculation and component selection, including the MOSFET, rectifier diode, magnetizing inductance, turns ratio, winding turns, and snubber elements [2], [10], [13].

This paper presents a systematic design methodology and a digital voltage-mode PI control implementation using a dSPACE control board for a 30 W flyback converter operating in DCM. The proposed workflow combines analytical design, component sizing, and experimental validation under variations of input voltage, load, and reference.

The main contributions of this work are summarized as follows:

- A structured end-to-end design methodology for a DCM flyback converter including magnetic component sizing, switch and diode stress analysis, and leakage energy management through RCD snubber design.
- Practical implementation of a digital voltage-mode PI controller tuned using Takahashi's method [14], [15], demonstrating stable regulation in DCM operation.
- Experimental validation of the complete system, including steady-state waveforms, transient response analysis, and efficiency evaluation.
- Quantitative comparison between theoretical calculations and measured hardware results, highlighting practical implementation constraints and non-ideal effects.

This paper is organized as follows. Section 2 presents the converter model in DCM. Section 3 details the design procedure and component selection. Section 4 discusses the experimental results. Finally, section 5 concludes the paper.

2. ELECTRICAL CIRCUIT AND MODELING IN DCM

The studied flyback converter provides a single isolated output voltage, as shown in Figure 1. The converter operates in discontinuous conduction mode (DCM), where the magnetizing current becomes zero during part of the switching period [5], [8]. In DCM, three operating intervals occur within one switching cycle:

- Mode 1 (Switch ON, Diode OFF): the input voltage Vg is applied to the primary winding, and energy is stored in the magnetizing inductance.
- Mode 2 (Switch OFF, Diode ON): the stored magnetic energy is transferred to the secondary winding and delivered to the load through the rectifier diode.
- Mode 3 (Switch OFF, Diode OFF): the magnetizing current decreases to zero, and no energy transfer occurs during this interval.

The equivalent circuits corresponding to these operating modes are illustrated in Figure 1.

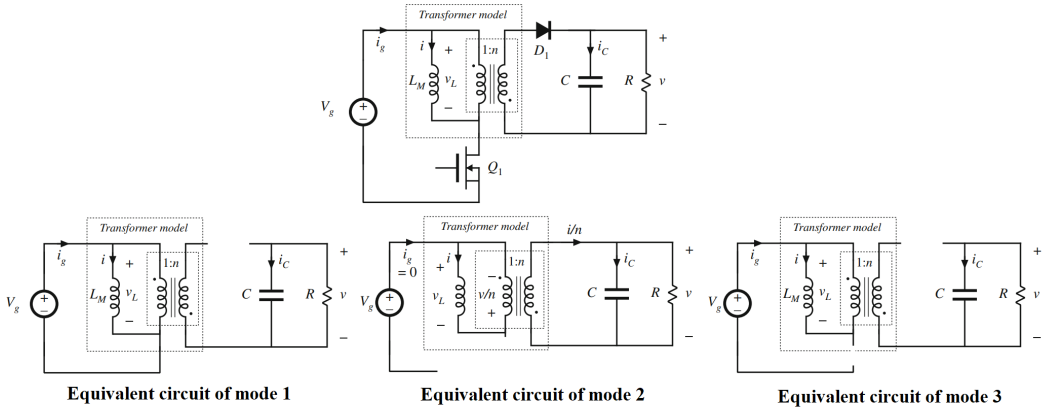


Figure 1. Flyback converter circuit with equivalent modes

2.1. Averaged modeling

To describe the dynamic behavior of the converter, the magnetizing current I_L and the output capacitor voltage V_c are selected as state variables:

$$x(t) = \begin{bmatrix} i_L \\ V_c \end{bmatrix} \tag{1}$$

Using Kirchhoff's voltage and current laws for each sub-interval and applying the state-space averaging method [16]-[19]. Table 1 presents modeling of the three operating modes of the converter.

Table 1. Three operating modes of the converter

Mode 1	Mode 2	Mode 3
$\begin{cases} V_L = V_g \\ i_c = -\dfrac{V(t)}{R} \\ i_g = i \\ V = V_c(t) \end{cases}$	$\begin{cases} V_L = V_g \\ i_c = -\dfrac{V(t)}{R} \\ i_g = i \\ V = V_c(t) \end{cases}$	$\begin{cases} V_L(t) = -\dfrac{V(t)}{n} \\ i_c(t) = \dfrac{i(t)}{n} - \dfrac{V(t)}{R} \\ i_g(t) = 0 \\ V(t) = V_c(t) \end{cases}$
$\begin{cases} \dot{x} = A_1 x + B_1 V_g(t) \\ y = C_1 x \end{cases}$	$\begin{cases} \dot{x} = A_2 x + B_2 V_g(t) \\ y = C_2 x \end{cases}$	$\begin{cases} \dot{x} = A_3 x + B_3 V_g(t) \\ y = C_3 x \end{cases}$
$\mathbf{A}_1 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{R_c C} \end{bmatrix}$, $\mathbf{B}_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$, $\mathbf{C}_1 = \begin{bmatrix} 0 & 1 \end{bmatrix}$	$\mathbf{A}_2 = \begin{bmatrix} 0 & -\frac{n}{L} \\ \frac{n}{c} & -\frac{1}{R_c C} \end{bmatrix}$, $\mathbf{B}_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$, $\mathbf{C}_2 = \begin{bmatrix} 0 & 1 \end{bmatrix}$	$\mathbf{A}_3 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{R_c C} \end{bmatrix}$, $\mathbf{B}_3 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$, $\mathbf{C}_3 = \begin{bmatrix} 0 & 1 \end{bmatrix}$

The flyback converter can be represented by the following averaged state model over one switching period:

$$\begin{cases} \dot{x} = Ax + BV_g(t) \\ y = Cx \end{cases} \tag{2}$$

where $V_g(t)$ is the input voltage and $y = V(t)$ is the output voltage.

The averaged system matrices are obtained from the weighted contribution of the three operating modes according to their respective duty ratios. The explicit expressions of A_1, A_2, and A_3 follow directly from the circuit equations of the three DCM operating intervals [16]-[19] are omitted here for brevity.

$$A = A_1 D_1 + A_2 D_2 + A_3 D_3, \quad B = B_1 D_1 + B_2 D_2 + B_3 D_3, \quad \text{and } C = C_1 = C_2 = C_3 \tag{3}$$

The control-to-output transfer function is expressed as:

$$F(p) = C(pI - A)^{-1} B \tag{4}$$

This averaged model provides the theoretical foundation for controller tuning and performance evaluation presented in section 4. The averaged model is used to represent the dynamic behavior of the converter and to guide the tuning of the voltage-mode PI controller implemented in the digital control platform.

3. FLYBACK CONVERTER DESIGN AND COMPONENT SELECTION

The design of the proposed 30 W DCM flyback converter is based on the specifications summarized in Table 2. The overall design procedure is illustrated in Figure 2.

Table 2. Design input summary

Design parameters	Value	Design parameters	Value
Input voltage (V_g)	20–30 V	Output voltage (V)	12 V
Output current (I_{OUT})	2 A	Switching frequency (f)	30 kHz
Estimated efficiency (η)	90–100 %	Maximum duty cycle (D_{max})	0.5
Operation mode	DCM		

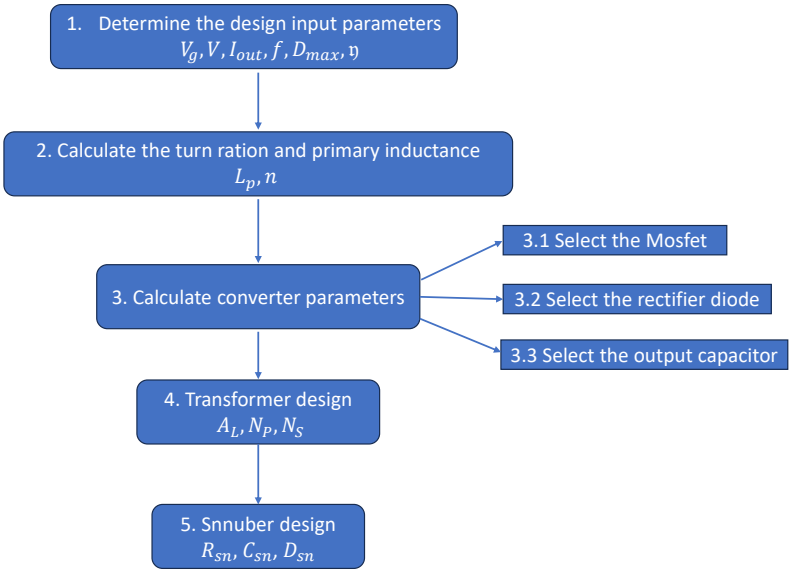


Figure 2. Flyback converter design flowchart

3.1. Primary inductance and turns ratio

In DCM operation, the primary inductance L_p is determined from [2], [12]:

$$L_p = \frac{(\eta D_{max}^2 V_g^2)}{(2fK_{rf}P_o)} \tag{5}$$

D_{max} represents the maximum duty cycle, $V_g(t)$ denoting the input voltage, P_o, representing the output power, f signifying the switching frequency, and K_{rf} is the ripple factor. DCM means that the ripple factor (K_{rf}) equal to 1 . The required turns ratio n is calculated as [2], [12]:

$$n = \frac{V_g D_{max}}{(1 - D_{max})(V + V_d)} \tag{6}$$

V_d: is the diode forward voltage, and $V$is the output voltage.

3.2. MOSFET selection

The MOSFET must withstand the maximum drain-source voltage and peak current. The maximum drain-source voltage is given by:

$$V_{DS_{max}} = V_{in} + \frac{D_{max} V_g}{1 - D_{max}} \tag{7}$$

the peak current is:

$$I_{pk} = \frac{P_{in}}{D_{max} V_g} + \frac{D_{max} V_g}{2 f L_p} \tag{8}$$

a safety margin of 20% in voltage and at least twice the calculated peak current is considered for reliable operation [2], [20].

3.3. Diode selection

The rectifier diode must withstand the peak inverse voltage:

$$V_{d_{pk}} = V_{out} + \frac{V_{in}}{n} \tag{9}$$

for safety reason we add a 40% to $V_{d_{pk}}$ A 40% voltage margin is applied to ensure safe operation [2], [20]. The current rating is selected above twice the maximum output current.

3.4. Output capacitor

The output capacitor is selected based on the allowable output voltage ripple:

$$C = \frac{D \times I_o}{f \times \Delta V} \tag{10}$$

3.5. Core selection

Core selection is based on the frequency and the power(30 Khz, 30 W in our case). The first step is to go to the magnetic ferrite core catalog [21], [22] and consulting the power-handling chart in the ferrite core catalog, then selecting the frequency and the power needed for the application. We found that the E25/13/7 core is the perfect core for our application also ETD49 is suitable for our converter. ETD 49 is used for our application. Once the core has been selected, the next crucial step involves calculating the number of turns for each winding, starting with the secondary winding [2], [10], [23]. The number of turns for the secondary winding (Ns) is determined by (11).

$$N_s = \sqrt{\frac{L_p}{A_L}} \tag{11}$$

A_L value refers to the inductance factor of a magnetic component, such as an inductor or transformer, that is constructed with a ferrite core. The A_L value is a measure of the inductance per turn squared (inductance per square of the number of turns) and is typically expressed in units of nanohenries per square turn ($nH/turn^2$). This value is given by the manufacturer in the datasheet of the used magnetic core. With 20 turns in the secondary winding, the calculation of the primary winding (N_p) is determined by the turn ratio (n), where n equals 2.

$$N_p = \frac{Ns}{n} \tag{12}$$

In addition, the maximum magnetic flux density was verified to ensure that the core operates below the saturation limit of the ferrite material. The estimated peak flux density remained within the safe operating range recommended by the core manufacturer. A basic estimation of magnetic losses based on manufacturer data confirmed that the selected core is suitable for the operating frequency and power level of the converter. The maximum magnetic flux density of the transformer core can be estimated using Faraday's law as presented in (13), which is commonly used in the design of flyback transformers.

$$B_{\max} = \frac{V_{\text{in}}\, D_{\max}}{N_p\, A_e\, f_s} \tag{13}$$

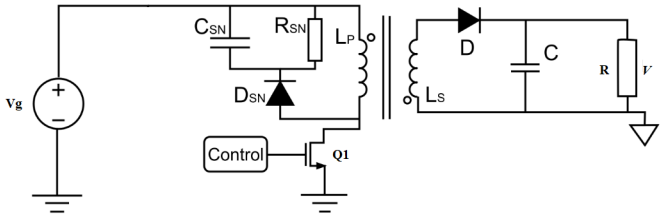


Figure 3. Flyback circuit with snubber circuit

3.6. Snubber components selection

Due to a resonance between the MOSFET's output capacitor (C_{OSS}) and the leakage inductor (L_{Lk}) of the main transformer, a high-voltage spike appears on the drain pin when the MOSFET turns off. An avalanche breakdown could result from the drain pin's increased voltage, which would ultimately damage the MOSFET. As a result, in order to clamp the voltage, another circuit must be added. To guarantee this we include a snubber circuit, as shown in Figure 3 [13], [24].

When calculating the values of the snubber components, we assume that the snubber voltage (V_{sn}) is equivalent to twice the product of the turn ratio (n) and the output voltage (nV).

$$V_{sn} = 2nV \tag{14}$$

The leakage inductance L_{Lk} is estimated to be $2\%$of the primary inductance L_p.

$$L_{Lk} = 0.02L_p \tag{15}$$

we calculate the resistance R_{sn} of the snubber circuit as presented in equation [5], [12]:

$$R_{sn} = \frac{V_{sn}^2}{\left(\frac{1}{2}L_k I_{pk}^2\right)\left(\frac{V_{sn}}{V_{sn}-nV_{out}}\right)f} \tag{16}$$

The maximum ripple of the snubber capacitor voltage is 10% of V_{sn}. Snubber capacitance C_{sn} is obtained as follows [5], [12]:

$$C_{sn} = \frac{V_{sn}}{\Delta V_{sn}.R_{sn}.f} \tag{17}$$

3.7. MOSFET driving circuit

The MOSFET is driven using an HCPL-3120 optocoupler to provide galvanic isolation and adequate gate drive voltage.

4. EXPERIMENTAL RESULTS

After component selection and hardware realization, the 30 W DCM flyback converter prototype was experimentally validated. The calculated component values are summarized in Table 3. The experimental setup is shown in Figure 4.

Table 3. Components values

Parameters	Value	Parameters	Value
Primary inductance (L_p)	100 μH	Turn ratio (n)	2
Drain-source voltage ($V_{DS_{max}}$)	48 V	Peak current (I_{pk})	4 A
Turns of secondary winding (N_s)	20	Turns of Primary winding (N_p)	10
Snubber voltage (V_{sn})	48 V	Snubber resistor (R_{sn})	2.35 $k\Omega$
Snubber capasitance (C_{sn})	141 nF		

Two configurations were tested:

- Open-loop operation.
- Closed-loop digital PI control.

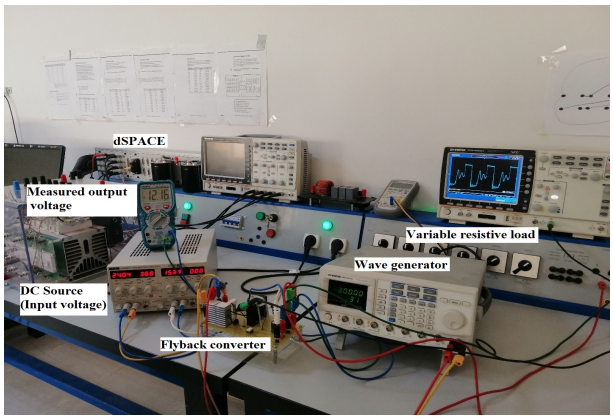
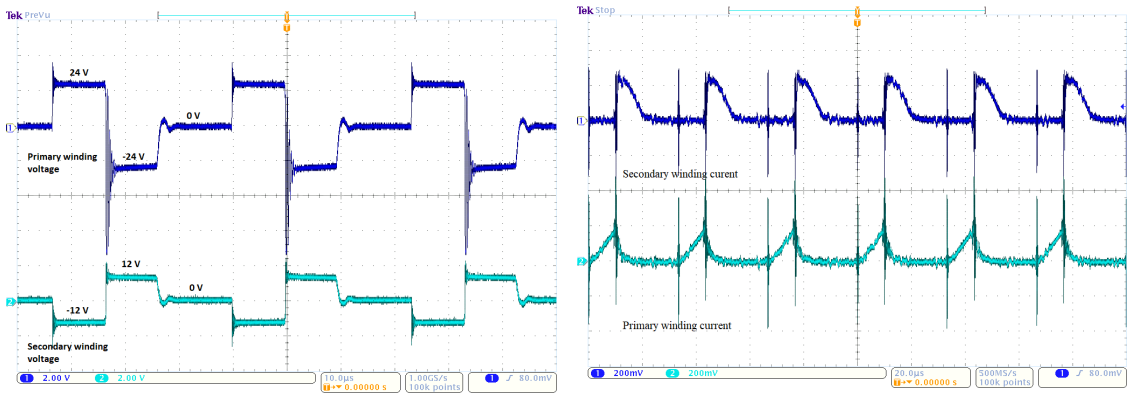


Figure 4. Experimental setup

4.1. Open-loop operation

In the open-loop configuration, the PWM signal was generated using an external waveform generator. The objective was to verify the expected DCM behavior. Figure 5 presents the experimentally measured transformer waveforms under open-loop operation. Figure 5(a) shows the primary and secondary voltages. Figure 5(b) shows the corresponding primary and secondary currents. The experimental waveforms confirm proper DCM operation, where the magnetizing current reaches zero before the next switching cycle. The measured results are consistent with theoretical predictions reported in [1]-[3], [5]-[25], with the magnetizing current reaching zero before the next switching cycle as expected in DCM operation, confirming the validity of the analytical design.

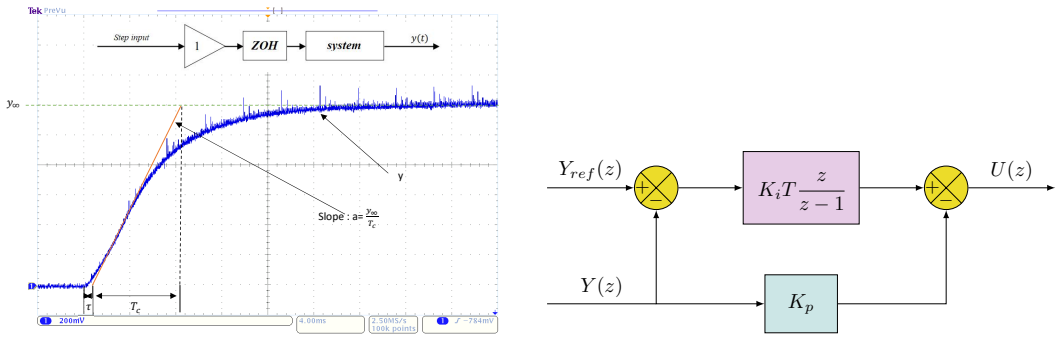


(a) (b)

Figure 5. Primary and secondary transformer waveforms,
(a) Primary and secondary winding voltage and (b) Primary and secondary winding current

4.2. Closed-loop digital control

A digital PI controller was implemented using the dSPACE 1104. The controller parameters were determined using Takahashi's tuning method [14], [15], which is a practical tuning approach derived from the Ziegler–Nichols method for discrete-time controllers [26]-[28]. Figure 6 presents the experimental step response used for parameter identification and the corresponding Takahashi PI control structure. Consequently, similar to the continuous case, it is necessary to subject the discrete system to an open-loop (OL) test as presented in Figure 6(a). This method is based on three parameters the slope (a), the rise time (T_c), and the delay time (τ) of the resulting step response from an open-loop (OL) test, as shown in Figure 6(a). The form of the PI controller used by Takahashi is summarized in Figure 6(b).



(a) (b)

Figure 6. Step response of a PID tuning with Takahashi rules and takhahashi control diagram
(a) step response of a PID tuning with Takahashi rules and (b) control diagram

Table 4 presents the empirical expressions of the parameters for digital P/PI/PID controllers proposed by Takahashi based on the open-loop response. The overall closed-loop control implementation and the corresponding experimental validation results are presented in Figure 7.

Table 4. Parameters of digital P/PI/PID controllers proposed by the Takahashi

Controller type	Controller parameters
Proportional (P)	$K_p = \frac{1}{a(\tau+T_c)}$
Proportional-Integral (PI)	$K_p = \frac{0.9}{a(\tau+0.5T_c)} + 0.5K_iT_c$ $K_i = \frac{0.27}{a(\tau+0.5T_c)^2}$
Proportional-Integral-Derivative (PID)	$K_p = \frac{1.2}{a(\tau+0.5T_c)} + 0.5K_iT_c$ $K_i = \frac{0.6}{a(\tau+0.5T_c)^2}$ $K_d = \frac{0.5}{a}$

Where $Y_{ref}(z)$, E(z), U(z), and Y(z) are, respectively, the setpoint, error, control input, and output of a closed-loop control system. K_p, and K_i, represent the proportional, and integral gains, respectively. The closed-loop architecture, facilitated by the PI controller in the DSpace environment, aims to enhance the overall stability and responsiveness of the system. Figure 7(a) illustrates the block diagram of the closed loop implementation.

4.2.1. Input voltage variation

The input voltage was varied from 20 V to 30 V while maintaining a reference output of 12 V. The maximum steady-state deviation was less than 2% of the nominal output voltage.

The results are presented in Figure 7(b). The output voltage remains regulated around 12 V despite input variations, demonstrating effective voltage regulation with the expected closed-loop performance. The duty cycle automatically adjusts to compensate for input changes. Figure 8 presents the experimental responses of the proposed controller under load variation and reference voltage variation tests.

4.2.2. Load variation

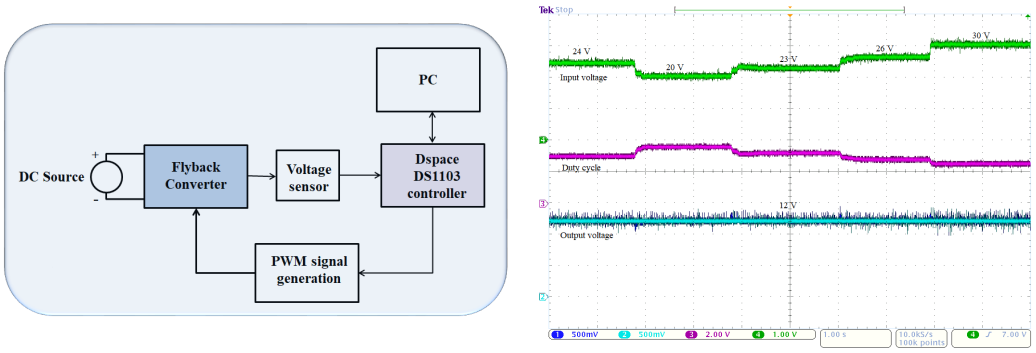
The load was varied from 48 Ω to 12 Ω while maintaining constant reference voltage. The experimental results are shown in Figure 8(a). The converter maintains stable output voltage under load variations. The maximum transient deviation during load step was 0.6 V with settling time below 8 ms during load transitions, indicating good dynamic performance consistent with the controller design.

4.2.3. Reference variation

The reference voltage was varied from 10 V to 14 V. The results in Figure 8(b) show accurate tracking performance, confirming that the digital PI controller ensures stable and responsive output regulation. Overall, the experimental results validate the proposed design methodology. The converter demonstrates stable operation, effective voltage regulation, and satisfactory dynamic performance under varying input, load, and reference conditions.

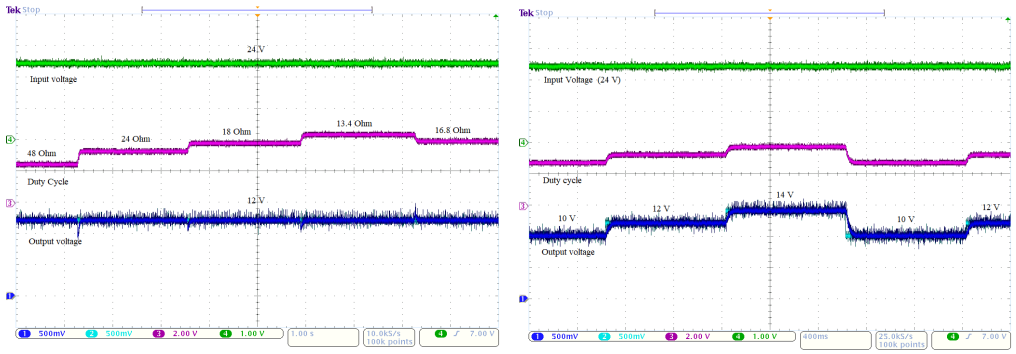
4.2.4. Efficiency evaluation

The converter efficiency was evaluated at nominal conditions (Vin = 24 V, Vout = 12 V, Iout = 2 A). The measured efficiency exceeded 90%, at nominal conditions, which is consistent with the expected performance based on the selected components and operating conditions. As expected in DCM operation, efficiency decreases at light load due to increased switching losses.



(a) (b)

Figure 7. Closed loop diagram and results under input voltage variation,
(a) closed loop diagram and (b) results under input voltage variation



(a) (b)

Figure 8. Results under load variation and reference changing,
(a) results under load variation and (b) results under reference changing

5. CONCLUSIONS

This paper presented the design, implementation, and experimental validation of a 30 W flyback converter operating in discontinuous conduction mode (DCM). A systematic design methodology was developed, covering magnetic component sizing, semiconductor stress evaluation, and RCD snubber design. A digital voltage-mode PI controller was implemented using a dSPACE 1104 platform and tuned according to Takahashi's method. Experimental results demonstrated proper DCM operation and stable output voltage regulation under variations of input voltage (20–30 V), load (48 Ω–12 Ω), and reference voltage (10–14 V). The measured waveforms confirmed agreement with theoretical predictions, and the controller ensured satisfactory dynamic performance with minimal transient deviations. The proposed methodology provides a practical and reliable framework for the design and implementation of low-power DCM flyback converters intended for regulated power supply applications.

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AUTHOR CONTRIBUTIONS

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Nabil Abouchabana	✓	✓		✓					✓					
Mohammed Benmiloud		✓								✓		✓		
Khaled Ameur			✓	✓	✓					✓				
Aboubakeur Hadjaissa				✓		✓								

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal Analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject Administration
Fu : **Fu**nding Acquisition

CONFLICT OF INTEREST STATEMENT

The authors state no conflict of interest.

DATA AVAILABILITY

Data availability is not applicable to this paper.

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BIOGRAPHIES OF AUTHORS

Dr. Nabil Abouchabana he received the engineer degree in Electronics in 2006 from the University of Laghouat, Algeria, the Magister degree in Electronics in 2009, and the Ph.D. degree in Electronics in 2022 from the National Polytechnic School of Algiers, Algeria. He is currently an assistant professor in the Department of Electronics at the University of Laghouat, Algeria. He is a member of the LACOSERE Laboratory, where he is actively involved in research on power systems and control systems. His current research interests include renewable energy generation systems, with particular emphasis on photovoltaic systems. He can be contacted at email: n.abouchabana@lagh-univ.dz.

Dr. Mohammed Benmiloud is an assistant professor in the Department of Electronics at Amar Telidji University of Laghouat, Algeria. He received the Ph.D. degree in Control Engineering in 2017 through joint supervision between the University of Laghouat and Université Polytechnique Hauts-de-France. He completed postdoctoral research at École Centrale de Nantes and later served as a research associate at the University of Cambridge. His research interests include advanced control systems, nonlinear dynamics, renewable energy systems, power electronics, and microgrids. He can be contacted at email: med.benmiloud@lagh-univ.dz.

Dr. Khaled Ameur he received the Engineer degree in Electronics from Laghouat University in 2005, the Magister degree in Instrumentation from the University of Science and Technology Houari Boumediene, Algiers, in 2009, and the Ph.D. degree in Electrical Engineering from Laghouat University in 2018. He is currently an associate professor in the Department of Electronics at Laghouat University. His research interests include renewable energy systems, electric vehicle chargers, power electronics, control systems, and battery management. He can be contacted at email: kh.ameur@lagh-univ.dz.

Pr. Aboubakeur Hadjaissa is a full professor at the Department of Electronics, University of Laghouat from 2012. He holds a Doctorate in Science from National Polytechnic School, Algiers, in 2016, with expertise in renewable energy systems, particularly photovoltaic and hybrid energy systems. His research focuses on power electronics, control systems, and optimization techniques. He can be contacted at email: b.hadjaissa@lagh-univ.dz.