

# Power-aware design-for-test: a survey of DFT techniques and scan chain reordering approaches

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## ABSTRACT

The rapid scaling of semiconductor technologies has significantly increased the integration density and introduced new categories of manufacturing defects, thereby increasing the test complexity and time. Scan-based design-for-test (DFT) architectures remain the most widely adopted method for digital IC testing, where test vectors are shifted serially into and out of scan chains. Because shift operations dominate the overall test time, reducing power during scan shifting is essential to prevent IR-drop, thermal issues, reliability degradation, and potential yield loss, and to enable higher shift frequencies. A higher shift frequency directly reduces the test application time and, consequently, the overall test cost. Excessive switching during scan shift remains a significant challenge, particularly in today's low-power devices, prompting extensive research on low-power DFT. This paper presents a structured survey of recent advancements in shift-power reduction, covering automatic test pattern generation (ATPG)-based low-power test pattern generation, built-in self-test (BIST)-based low-transition pattern generation, and modern scan-chain optimization and reordering strategies. The survey highlights that among various solutions, scan chain reordering stands out as one of the most effective and scalable power-aware DFT techniques, due to its minimal implementation overhead, seamless integration with existing ATPG/BIST flows, and significant ability to reduce 20–50% scan-shift power without requiring pattern regeneration.

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## 1. INTRODUCTION

With continuous advances in semiconductor fabrication, modern complementary metal–oxide–semiconductor (CMOS) integrated circuits (ICs) now contain billions of transistors. Simultaneously, constraints such as limited battery capacity, high cooling costs, and strict reliability requirements have made power consumption a critical consideration throughout the IC design and test processes. In full-scan designs, every functional flip-flop is replaced with a scan flip-flop that operates in two distinct modes: shift and capture. During the shift mode, these scan flip-flops are connected to form one or more scan chains that interface directly with an external tester. The test vectors are serially shifted into the scan chains, and the captured responses are shifted out in the same manner. During the capture mode, the scan flip-flops behave as functional elements, capturing the circuit's response to the applied test vector before it is shifted out.

Test power during scan mode is significantly higher than in functional operation for several reasons [1]: (i) large portions of scan logic that remain inactive in functional mode toggle heavily during scan shifting

[2], (ii) high shift frequencies are typically used to reduce test application time, and (iii) parallel activation of multiple scan chains further increases switching activity. As a result, both average and peak test power must be carefully controlled.

The industry commonly employs several techniques to keep the test power within safe limits, although each introduces penalties in terms of cost, test time, or hardware overhead.

- Increasing the power supply, packaging, or cooling capacity: This approach mitigates excessive test power but significantly increases hardware and test infrastructure costs [3], [4].
- Partitioning the design and testing one region at a time: This reduces instantaneous switching activity and preserves the detection of dynamic faults, but it requires additional hardware support, increases the test duration, and leads to higher overall energy consumption [5], [6].
- Reducing the test frequency: Lowering the frequency decreases the instantaneous power but proportionally increases the test time and may mask certain dynamic faults, reducing the defect coverage [7].

In contrast to prior low-power design-for-testability (DFT) surveys that broadly classify scan power reduction techniques, this paper presents a focused and unified treatment of scan chain optimization and reordering as a central strategy for shift-power reduction. It integrates classical pattern reordering, graph-based methods (MST/TSP), metaheuristics, and emerging machine learning and reinforcement learning approaches within a single comparative framework. The survey further highlights quantitative power-reduction trends, test-time implications, and fault-coverage preservation, offering practical insights applicable to automatic test pattern generation (ATPG)-based, built-in self-test (BIST)-based, and mixed-mode test environments.

The rest of this paper is organized as follows. Section 2 presents a comprehensive literature survey, summarizing major advancements in low-power DFT techniques and reviewing state-of-the-art methods for reducing test-mode power. Section 3 provides a detailed review of scan-chain optimization research, including classical algorithms, heuristic approaches, and recent machine-learning-based solutions. Section 4 discusses the Results and how scan-chain reordering is an effective low-power DFT strategy. Finally, section 5 concludes the paper with key observations and outlines potential directions for future research in low-power scan-based testing.

## 2. LITERATURE SURVEY: OVERVIEW OF LOW-POWER DFT TECHNIQUES

For scan-based testing, test patterns are typically generated either by an ATPG tool or by a BIST pattern generator. Shift-mode power can be reduced through structural modifications to the design or by optimizing the test patterns themselves. Numerous techniques have been proposed in the literature to effectively minimize shift power during scan operations. The following subsections delve into these distinct approaches, starting with ATPG-based methods.

Scope of survey: Timeframe (1998–2025), focus on power-aware DFT and scan reordering.

### 2.1. Scan power reduction techniques in DFT (ATPG-based methods)

ATPG-based low-power DFT techniques focus on strategies applied during or after generating deterministic test patterns. These methods reduce the switching activity when externally applied test patterns are shifted to the scan chains.

#### 2.1.1. Scan architecture-level techniques

##### A. Use of special scan cells

Special scan flip-flops are designed to block or gate unnecessary transitions during the scan shift. They prevent transitions from propagating into combinational logic while maintaining standard scan functionality. Representative works include modified scan flip-flops, gated or isolation scan cells, and trimodal scan cells [3], [4]. Figure 1 shows a cell that uses separate latches. This technique significantly reduces shift-induced toggles; however, it introduces additional area and delay overhead.

##### B. Scan chain segmentation and staggered clocking

Segmentation divides a long scan chain into smaller segments that are clocked separately or in a non-overlapping manner, as shown in Figure 2. This ensures that not all the scan cells switch simultaneously, thereby lowering the instantaneous peak power. Examples include skipping inactive segments or frequency-scaled segmented architectures [5]–[8]. This technique reduces the peak shift power and mitigates the IR-drop; however, it requires additional control logic and the use of multiple clock phases.

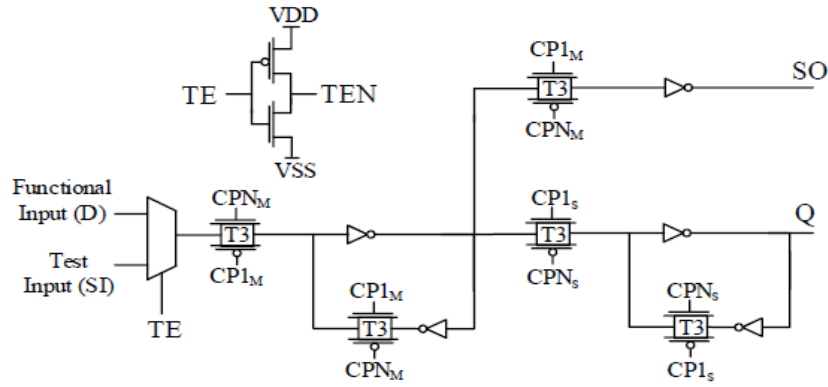


Figure 1. Scan cells with gated functional output during shifting, cells with separate latches for functional and scan path [4]

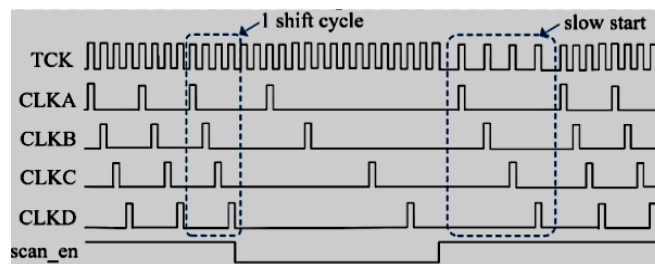


Figure 2. Staggered clock operation [6]

**C. Scan path modification (Reconfigurable scan architecture)**

Modifying the scan path structure allows for the decoupling of the scan chain sections or the selective activation of portions of the chain. Reconfigurable scan architectures and clock-gated scan groups fall under this category [9], [10]. This approach provides direct control over switching propagation; however, its routing overhead demands careful integration.

**D. Scan chain ordering based on logic connectivity**

Scan cells are stitched based on logic connectivity or topology, such that transitions in one cell do not propagate excessively into highly active logic cones, as shown in Figure 3. LoCCo-based and topology-based chain stitching demonstrate this principle [11]–[14]. This method reduces unnecessary internal toggles during the shift; however, it requires a detailed gate-level connectivity analysis.

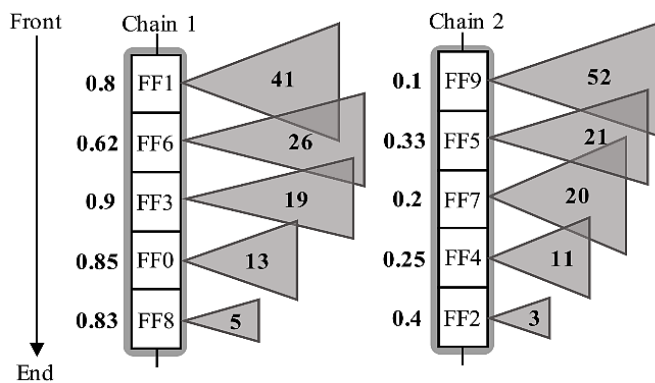


Figure 3. Scan stitching proposed in [12] analyzes the fanout of cells and puts flops with greater influence at the front of scan chains and lower influence values at the end of the scan chain

### E. Scan chain ordering based on pattern content

The order of the scan cells is optimized using the expected test pattern contents, such as the care bit density or expected transition sequences [15]. This technique is highly effective when the pattern contents are known, but it is pattern-dependent and requires access to ATPG-generated patterns.

### F. Scan cell reordering based on transition weights

After low-transition patterns are generated, the scan cells are reordered based on the “scan influence” or transition weight metric, ensuring minimal propagation of toggles into combinational logic [16]–[19]. This technique is highly effective within the BIST because of the predetermined pattern order; however, it requires a detailed analysis of the transition weights.

#### 2.1.2. ATPG-level techniques

##### A. pattern modification via X-filling

The don't-care bits in ATPG patterns can be filled in ways that minimize shift toggles. Techniques such as correlation-based fill, weighted fill, and power-aware fill reduce the transitions between successive bits [20]. This method incurs no hardware cost and works with existing patterns, but its impact is limited when the X-bit density in patterns is low.

##### B. Pattern reordering for shift-power reduction

Test vectors can be reordered to minimize toggles between consecutive patterns based on hamming distance minimization or energy-aware heuristics [21]–[26]. This approach reduces the aggregate shift power across the test sessions; however, its effectiveness may interact with pattern compaction or compression techniques.

##### C. Low-transition test pattern generators (TPGs)

Low-toggle TPGs, such as bit-swapping LFSRs, Johnson counters, and single input change (SIC) pattern generators, reduce the number of transitions between patterns [27]–[29]. This technique reduces both the shift and capture power in BIST but offers limited control over fault coverage unless additional enhancement mechanisms are applied.

#### 2.1.3. BIST-based low-power techniques

##### A. Low-power techniques in BIST architectures

BIST architectures generate patterns on-chip using LFSRs or other pseudo-random pattern generators. Their naturally high toggling rate requires specialized low-power patterns and scan organization [30]. While various techniques contribute to low-power DFT, scan chain optimization and reordering stand out due to their significant impact on shift power, with often minimal hardware overhead. The following section provides a detailed examination of the key research advancements in this specific domain, exploring how different algorithmic approaches have tackled the challenge of efficient scan chain configuration.

### 3. DETAILED REVIEW OF SCAN CHAIN OPTIMIZATION RESEARCH

Scan chain optimization is an evolving research area that includes pattern reordering, graph-based scan reordering, metaheuristics, and ML/RL-based strategies. Existing scan chain reordering approaches are largely heuristic-driven and static, with limited scalability, adaptability, and generalization across diverse circuit structures. They typically optimize a single objective without explicitly modeling physical effects such as interconnect delay or enabling dynamic power–wirelength trade-offs. Moreover, the absence of learning and feedback mechanisms prevents knowledge transfer and continuous improvement across designs.

#### 3.1. ATPG-level techniques: pattern/vector reordering and X-Fill

1. P. Girard, C. Landrault, S. Pravossoudovitch, D. Severac, “Reducing power consumption during test application by test vector ordering,” *Proc. IEEE ISCAS*, 1998 [31].

An early influential paper formalized the idea of minimizing switching during scan shifts by reordering the test vectors [32], [33]. They considered the Hamming distance between consecutive vectors and proposed heuristics to reduce the number of transitions. Results showed that ordering can significantly reduce switching and peak current in benchmarks.

Pros/Cons/Relevance: Foundational; demonstrates basic effectiveness of ordering. It does not explore advanced graph/metaheuristic seeding and ignores the don't-care filling. It serves as a useful baseline and historical anchor.

2. D. Song *et al.*, “MTR-fill: simulated annealing-based x-filling to reduce test power dissipation,” *IEICE Trans.*, 2008 [34], [35].

Proposes a simulated annealing approach to fill in the don't-care bits (X) in ATPG patterns to minimize transitions (both shift and capture). Formulates cost and uses SA search to set Xs. Results show a significant reduction in capture and shift power when many Xs are present.

Pros/Cons/Relevance: X-fill is very effective when ATPG yields many Xs; SA yields better solutions than greedy X-fills but is computationally heavier. This is highly relevant when you want to combine ordering with X-fill.

3. C. R. Supreta Devi *et al.*, "A novel approach for x-filling and reordering test vectors for power reduction," *Research Journal of Applied Sciences*, 2012 [36].

Combines X-fill and reordering heuristics to jointly reduce shift and capture transitions.

Pros/Cons/Relevance: Practical approach; shows joint optimization is beneficial. This method was used as a practical comparative method.

### 3.2. Graph-based ordering (MST/Kruskal, TSP approximations)

4. Cluster-MST approaches-(representative) M. Navin Kumar *et al.*, "Cluster-based test vector re-ordering for reduced power dissipation in digital circuits," *Automatika*, 2023 [37].

Two-stage method-cluster test vectors by similarity, then compute MST (via Kruskal) inside clusters and linearize MST to obtain an ordering. Edge weights use the Hamming distance (optionally weighted by bit significance). Results report  $\approx 10\text{--}12\%$  reduction in switching on ISCAS'89 benchmarks without changing patterns or coverage.

Pros/Cons/Relevance: MST/Kruskal provides a fast, deterministic, high-quality backbone; clustering scales to large pattern sets. This is the main candidate for the MST choice.

### 3.3. Metaheuristics (GA, SA, PSO, ACO)

5. S. Alam and R. Roy, "Genetic algorithm based optimization of test vectors for low power testing," *Microelectronics Journal*, 2020 [38].

GA to evolve permutations of the test vectors by minimizing the average Hamming cost and optionally the peak transitions. Chromosome = vector ordering; fitness = power metric. Results show GA often outperforms greedy heuristics on small to medium pattern sets.

Pros/Cons/Relevance: Good solution quality but high runtime for large sets; useful as a gold-standard baseline or refinement stage seeded by MST.

6. Balwinder Singh *et al.*, "Particle swarm optimization framework for low power testing of VLSI circuits," (arXiv:1111.1564), 2011 [39].

PSO for ordering; particles represent permutations encoded via continuous vectors mapping to the permutation via sorting.

Pros/Cons/Relevance: Simpler to implement than GA; variable performance. It offers an alternative metaheuristic baseline.

7. Hybrid ant colony + MST (recent works/representative: 2024–2025 ACO+MST papers).

S. Asha Pon and V. Jeyalakshmi, "Test pattern optimization scheme based on hybrid ant colony optimization," *Scientific Reports*, vol. 15, Article no. 34453, 2025 [40], [41].

Use MST to seed pheromone initialization; ACO refines ordering by pheromone updates driven by transition cost.

Pros/Cons/Relevance: High-quality results in experiments, but computational cost and tuning required; shows good synergy with MST seeding.

### 3.4. Simulation-based and RPRF analysis (LBIST)

8. Y. Sun, "Novel test point insertion applications in LBIST," PhD Thesis, Auburn University, 2018 [30].

Detailed study of RPRFs and TPI targeted for LBIST; includes probabilistic analysis of random detectability and TP selection to improve LBIST coverage.

Pros/Cons/Relevance: RPRF work is the go-to reference for LBIST-oriented TPI; if you target LBIST or random patterns, RPRF TPI is essential.

9. Simulation-based TPI works (various academic flows)

R. S. Vethamuthu and S. Sivanantham, "Novel test point insertion mechanism using timing-aware analysis to target challenges in high-complexity SoC designs," *International Journal of Innovative Science and Advanced Engineering (IJISAE)*, Jul. 2023 [42].

It presents a timing-aware TPI method [43]–[46] that uses post-synthesis timing and fault-coverage analysis to insert only highly effective points, minimizing area overhead while retaining coverage. It reports large reductions in the TPI area overhead and vector count. Good reference for practical, low-overhead TPI for large SoCs.

Pros/Cons/Relevance: Captures sequential dynamics missed by static SCOAP; expensive and sensitive to vector quality-useful when dynamic behavior dominates.

**3.5. Machine learning and deep reinforcement learning (TPI and scan optimization)**

10. Z. Shi *et al.*, “Deep TPI: test point insertion with deep reinforcement learning,” arXiv/IEEE, 2022 [47].

The model circuit is a directed graph that uses a graph neural network (GNN) for node embeddings and deep Q-learning (DQN) [45], [48] as the value estimator. Figure 4 shows the overview of the deep TPI RL agent. The agent sequentially inserts CP/OP to maximize the coverage gain minus the cost. It includes testability-aware attention and pretrained embeddings. Results show that these methods outperform baseline commercial heuristics on several benchmarks in terms of coverage improvement and pattern reduction under an area budget. Pros/Cons/Relevance: Strong evidence that learning jointly selects TPs better than greedy rules; baseline for your TPI RL choice. Cost: training complexity and engineering integration issues.

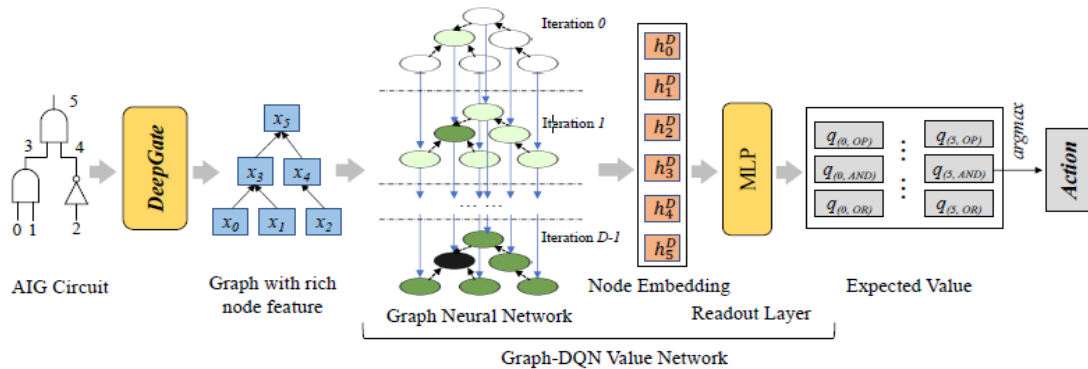


Figure 4. The overview of deep TPI agent [47]

11. J. Zhang *et al.*, “GNN-TPI: Graph neural network based test point optimization,” DAC, 2023 [49].

GNN applied to TPI as a supervised or reinforcement scheme shows an improved selection of nodes with a better coverage-overhead tradeoff.

Pros/Cons/Relevance: Reinforces the GNN+RL direction; provides architecture and scaling insights likely useful if adapting to scan reordering.

12. RL for scan ordering & pattern scheduling-e.g., RL-based BIST pattern generation (Rahman *et al.*, VTS 2021) [50]–[54].

Use RL agents (DQN/PPO) to schedule patterns or activate chains to minimize toggles/peak power subject to coverage constraints

Pros/Cons/Relevance: Demonstrates that RL is applicable when the action space is large (sequence building); provides benchmarks for reward shaping and environment modeling.

**4. RESULTS AND DISCUSSION**

Table 1 summarizes the existing methods for scan power optimization, considering various parameters.

**4.1. Scan chain reordering as an effective low-power DFT strategy**

Scan chain reordering is a low-power DFT technique that is advantageous for several reasons.

- No impact on fault coverage: reordering does not modify test patterns or fault activation paths; it only changes the shift behavior. Thus, the coverage remained unaffected.
- Minimal hardware overhead: unlike special scan cells or segmentation, reordering requires no additional gates or clocks when implemented logically at the stitching time.
- Complementary to all other techniques: reordering can be combined with X-fill (pattern modification), low-transition TPGs (BIST), segmentation, clock gating, and learning-based scheduling.
- Scales easily to large designs: graph-based or heuristic reordering operates efficiently on designs with tens of thousands of scan cells.
- Significant reduction in shift power: Studies consistently report 20–50% shift power reduction using reordering alone, and up to 60–70% when combined with X-fill or low-transition patterns.

- Works for ATPG, BIST, and mixed-mode test flows: this makes reordering a universal solution adaptable across industrial DFT flows.

Table 1. Summary of existing methods for scan power optimization

S.No	Technique (representative refs)	Test time	Switching activity	Power consumption	Area overhead	Complexity	Coverage impact	Advantages	Disadvantages/Notes
1	Vector reordering (Girard <i>et al.</i> )-Hamming-distance ordering [31]	Neutral (ordering only)	10–25%	10–20%	None	Low	No impact	Simple; no HW changes; good baseline	Limited when X-density is low; does not address capture power
2	X-Fill (SA, MTR)-Simulated annealing X-fill [34]	Slight ↑ (preproc) / Neutral at test	20–50%	20–45% (shift + capture)	None	Medium–High (SA runtime)	Potential risk if the care bits are changed incorrectly	Strong when ATPG produces many Xs; works with existing flow	Computationally heavy; effectiveness depends on X-density
3	Joint X-fill + Reordering (Devi <i>et al.</i> ) [36]	Neutral	30–60%	30–55%	None	Medium	Low risk if applied carefully	Synergistic gains vs. separate methods	Higher tool/runtime complexity than single methods
4	Cluster + MST ordering (Navin Kumar) clustering then MST/Kruskal [37]	Neutral	12–30%	10–25%	None	Low–Medium	No impact	Fast, deterministic; scales to many vectors	Gains modest vs. heavy metaheuristics; depends on clustering quality
5	Genetic Algorithm (GA)-ordering by GA [38]	Neutral / Possible ↑ (search time)	25–55%	25–50%	None	High	No impact	High-quality solutions; flexible objective design	High runtime, poor scalability to huge pattern sets
8	RPRF / LBIST-oriented TPI (Sun, thesis) [30]	May ↑ (extra patterns)	15–35%	15–30%	Small–Moderate	High (analysis)	Potentially improves random-fault coverage	Improves LBIST detectability; theory-backed	Complex probabilistic analysis, specialized to LBIST
9	Timing-aware simulation-based TPI (Vethamuthu <i>et al.</i> , 2023) [42]	Test time neutral / may ↑ (TPI tests)	20–40%	20–35%	Small	High	Low risk (timing-aware preserves coverage)	Targets high-complexity SoCs; low overhead TPI	Expensive simulation; sensitive to vector quality
10	DeepTPI (GNN + DQN) [47]	Neutral / Training time ↑	30–60%	25–50%	Small (points inserted)	High (ML training + infra)	Typically improves coverage under budget	Learns nuanced trade-offs; outperforms heuristics	high development/training cost; reproducibility concerns
11	GNN-TPI (DAC 2023) [49]	Neutral / Training ↑	25–50%	20–45%	Small	High	Improves trade-off coverage/overhead	Scalable learning approach; good empirical results	Complexity and toolchain integration required
12	RL for scan ordering AND scheduling (VTS/DAC workshop) [40], [51], [53]	Can reduce test time	30–65%	30–60%	None–Small	High	Must be validated	Flexible online/adaptive control; handles large action spaces	Requires environment modeling; reward shaping is hard

## 5. CONCLUSION AND FUTURE RESEARCH DIRECTIONS

Low-power DFT techniques are crucial for modern VLSI designs due to their increasing complexity and power sensitivity. Among these, scan chain reordering is a highly effective, low-overhead, and scalable solution. It preserves fault coverage, requires minimal hardware, and complements other power-reduction strategies, such as X-fill, segmentation, clock gating, low-transition TPGs, and learning-based scheduling. Studies have shown a 20–50% shift power reduction with reordering alone, and up to 60–70% when combined with pattern modifications or low-transition patterns. Applicable across ATPG, BIST, and mixed-

mode test flows, scan chain reordering is a versatile architecture-agnostic approach and remains an active research focus in low-power DFT methodologies, due to its minimal implementation overhead, seamless integration with existing ATPG/BIST flows, and significant ability to reduce scan-shift power without requiring pattern regeneration.

Despite significant progress, several promising research directions remain open:

- Hybrid graph- and learning-based reordering: Integrating deterministic graph-based techniques such as clustering and MST with reinforcement learning or metaheuristics can further improve optimization quality while maintaining scalability.
- Joint test power and test time optimization: Future methods should jointly optimize shift power, test application time, and scan scheduling, particularly in multi-chain and compressed scan architectures.
- Scalability to complex SoCs: Scan optimization techniques must evolve to handle large heterogeneous SoCs with multiple power domains and embedded IPs efficiently.
- interactions between scan reordering, test compression, and automated DFT insertion tools will be key to broader industrial adoption.

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C : **C**onceptualization  
 M : **M**ethodology  
 So : **S**oftware  
 Va : **V**alidation  
 Fo : **F**ormal analysis

I : **I**nvestigation  
 R : **R**esources  
 D : **D**ata Curation  
 O : Writing - **O**riginal Draft  
 E : Writing - Review & **E**ditng

Vi : **V**isualization  
 Su : **S**upervision  
 P : **P**roject administration  
 Fu : **F**unding acquisition

**CONFLICT OF INTEREST STATEMENT**

The authors declare that there are no known competing financial interests or personal relationships that could have appeared to influence the work.

**DATA AVAILABILITY**

Data availability does not apply to this paper as no new data were created or analyzed in this study.

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