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Predictive control strategy for a novel 15-level inverter with reduced power components

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ABSTRACT

This paper proposes a novel fifteen-level H-PTC inverter topology controlled by model predictive control (MPC), which reduces the number of components. The design employs only two DC sources, nine switches, including one bidirectional switch, and a single capacitor. The system's performance is validated through MATLAB/Simulink simulations under various scenarios, such as steady-state operation, load variations, nonlinear loads, and sudden supply voltage disturbances. Compared to existing topologies, the proposed inverter demonstrates hardware simplicity, high output quality, and enhanced dynamic robustness. Notably, it features very low total standing voltage (TSV) and a minimized cost function value of 2.05. For a load characterized by R = 20 Ω and L = 20 mH, the total harmonic distortion (THD) of the load current is 0.88%, confirming excellent power quality without the need for output filters. The MPC controller ensures a fast dynamic response and strong adaptability, making this topology ideal for modern energy conversion applications.

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1. INTRODUCTION

Over the past few years, power converters, particularly inverters, have become essential components across many modern applications, like electric vehicles [1], [2]. Compared to traditional inverter designs, multilevel inverters exhibit superior performance characteristics, including minimized harmonic distortion in the output waveform, enhanced amplitude of the fundamental component, improved energy conversion efficiency, reduced voltage stress on power switches, and decreased filter size requirements due to improved waveform quality. The multilevel topology generates stepped voltage waveforms that closely approximate sinusoidal outputs. This approach significantly reduces the required filter components. The improved output quality minimizes electromagnetic interference and enhances system compatibility. These characteristics enable successful operation in sensitive applications while meeting regulatory standards. The voltage distribution across multiple switching devices reduces individual component stress. This design permits the use of lower-rated semiconductor devices with improved availability. The distributed architecture enhances overall system reliability through inherent redundancy. High-quality power delivery reduces stress on connected loads and equipment. This performance extends operational lifetime in industrial and renewable energy applications.

Conventional multilevel inverter topologies include the floating capacitor (FC) [3], neutral point clamped (NPC) [4], and cascaded H-bridge (CHB) [5]. These configurations are employed in power conversion systems; nonetheless, these architectures suffer from notable limitations, particularly the use of

many components, which increases design complexity and system bulk. Multilevel converters present challenges related to DC sources [6], modulation techniques [7], and capacitor voltage control [8]. On the other hand, multilevel inverters often face a key challenge linked to the high voltage stress on their switches. This stress can be understood through two important concepts: the total standing voltage (TSV) [9], which is the highest voltage each switch needs to handle when it's off, and the total blocking voltage (TBV), which is essentially the total voltage that all the switches together must block.

When designers attempt to simplify the inverter by using fewer switches, typically to reduce costs or complexity, each switch ends up taking on a larger share of the voltage. That means the TSV on each switch goes up, and they might need to be rated for higher voltages. At the same time, the overall TBV also increases, especially if the switches are connected in series or if the voltages across capacitors aren't perfectly balanced. Higher voltage stress creates hardware challenges and increases switching losses, reducing inverter efficiency and long-term reliability. The researchers must balance the benefits of fewer components against voltage stress. This balance is essential to maintain performance while controlling costs and preventing failure.

Various topologies have been suggested in previous research to address the challenges mentioned previously. Among them, the packed U-Cell (PUC) topology [10] emerges as an innovative solution in power converter design. This topology stands out as a practical and efficient choice for renewable energy conversion systems. One of its key strengths is its ability to produce Several voltage levels using just a single isolated DC source and fewer components, which simplifies the overall circuit design. This not only helps reduce installation costs but also makes the system more compact and easier to control. Moreover, the PUC design helps improve power quality by minimizing total harmonic distortion (THD) and lowering voltage stress on the components, which can lead to better performance and longer-lasting equipment [11].

Indeed, specific applications of PUC converters have demonstrated their capability to produce high voltage levels using a single DC source, whether isolate [12]-[14] d or derived from photovoltaic arrays [15]. Generating multiple voltage levels in PUC inverters relies on smart control strategies, which can be either open-loop or closed-loop. Open-loop methods use fixed switching patterns, while closed-loop strategies actively adjust based on real-time feedback [16], [17].

To address the limitations of conventional multilevel inverters, this paper introduces a new fifteen-level hybrid H-PTC inverter topology combining a PTC structure based on the PUC topology with an H-bridge inverter. This work makes the following main contributions:

– A simplified design leads to a more compact and cost-effective architecture
– Achieving reduced TSV and TBV

The implementation of a robust model predictive control (MPC) strategy that ensures precise capacitor voltage balancing and an output voltage of excellent quality, characterized by minimal THD under various operating conditions.

2. METHOD

2.1. Proposed topology and switching states

The reference PTC topology [18], illustrated in Figure 1, uses five power switches (IGBTs), including one bidirectional switch, and a single DC source, combined with a single capacitor to generate a five-level output voltage. This structure is derived from the SPUC5 inverter [19], which relies on two capacitors, whereas the PTC topology operates with only one, simplifying the configuration. Building on this architecture, we propose a new topology called H-PTC, shown in Figure 2. This design combines the original PTC converter with an H-bridge inverter. It incorporates nine power switches (IGBTs), two DC sources, and a single capacitor. The H-PTC inverter generates a fifteen-level output voltage while minimizing electronic components compared with other multilevel structures.

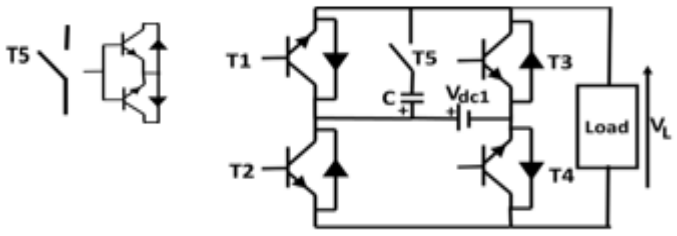

Figure 1. PTC inverter

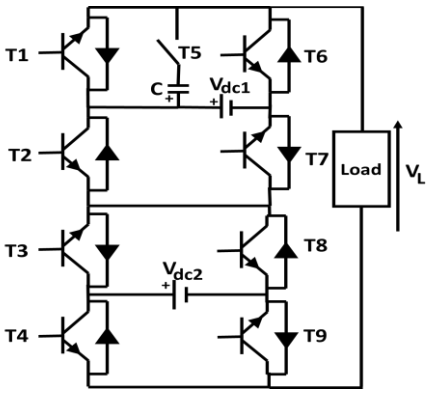

Figure 2. Proposed H-PTC inverter

Table 1 presents the various switching combinations related to the proposed inverter, which enable the generation of 15 distinct output voltage levels by choosing V_{dc1}=6 V_{dc}=360 V, V_{dc2}=V_{dc}=60V, and considering V_C=V_{dc1}/2=3 V_{dc}=180 V. These levels result from the superposition of the voltage supplied by the power tapping converter (PTC) and the output of the H-bridge inverter. It is worth noting that two redundant switching states in Table 1 result in a zero output voltage, providing additional flexibility in selecting the switching state. Figure 3 illustrates the specific switching sequences associated with the null and positive voltage levels at the output. In these diagrams, the switches conducting the current are highlighted in red to facilitate visualization of the current path.

- In Figure 3(a), the null voltage is obtained through the activation of switches T_1, T_2, T_3, and T_4.
- Figure 3(b) shows the generation of the first positive level, equal to V_{dc}, achieved via switching on T_1, T_2, T_3, and T_9.
- Figure 3(c) illustrates the generation of the second level (2 V_{dc}), resulting from the combination of the capacitor voltage with the DC sources, through the activation of switches T_4, T_5, T_7, and T_8. In this configuration, the capacitor charges if the load current is greater than zero (i_L > 0) and discharges if the current is negative. The capacitor is pre-charged to a voltage equal to half of the main DC source, serving as an energy buffer to support the generation of intermediate voltage levels.
- Figure 3(d) shows the generation of the 3 V_{dc} level, obtained by combining the capacitor voltage with the main DC source, through switches T_5, T_7, T_8, and T_9.
- In Figure 3(e), the 4 V_{dc} level is produced by combining the capacitor with both DC sources, via switches T_3, T_5, T_7, and T_9.
- Figure 3(f) highlights the generation of the 5 V_{dc} level, resulting from the direct combination of the two DC sources, achieved by turning on switches T_1, T_4, T_7, and T_8.
- In Figure 3(g), the 6 V_{dc} level is achieved by activating switches T_1, T_7, T_8, and T_9.
- Finally, Figure 3(h) demonstrates the generation of the maximum output level (7 V_{dc}), obtained by combining both DC sources through switches T_1, T_3, T_7, and T_9.
- Table 1 also shows the negative voltage levels with their asymmetric switching arrangements.

Table 1. Commutation states for the H-PTC multilevel inverter

State	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	Capacitor	Interconnexion	V_L(V)
1	1	0	1	0	0	0	1	0	1	---	V_{dc1}+V_{dc2}	420
2	1	0	0	0	0	0	1	1	1	---	V_{dc1}	360
3	1	0	0	1	0	0	1	1	0	---	V_{dc1}-V_{dc2}	300
4	0	0	1	0	1	0	1	0	1	---	-Vc+V_{dc1}+V_{dc2}	240
5	0	0	0	0	1	0	1	1	1	---	-Vc+V_{dc1}	180
6	0	0	0	1	1	0	1	1	0	charge	-Vc+V_{dc1}-V_{dc2}	120
7	1	1	1	0	0	0	0	0	1	charge	V_{dc2}	60
8	1	1	1	1	0	0	0	0	0	charge	0	0
8’	0	0	0	0	0	1	1	1	1	---	0	0
9	0	0	0	1	0	1	1	1	0	---	-V_{dc2}	-60
10	0	1	1	0	1	0	0	0	1	---	-Vc+V_{dc2}	-120
11	0	1	1	1	1	0	0	0	0	---	-Vc	-180
12	0	1	0	1	1	0	0	1	0	discharge	-Vc-V_{dc2}	-240
13	0	1	1	0	0	1	0	0	1	discharge	-V_{dc1}+V_{dc2}	-300
14	0	1	1	1	0	1	0	0	0	discharge	-V_{dc1}	-360
15	0	1	0	1	0	1	0	1	0	---	-V_{dc1}-V_{dc2}	-420

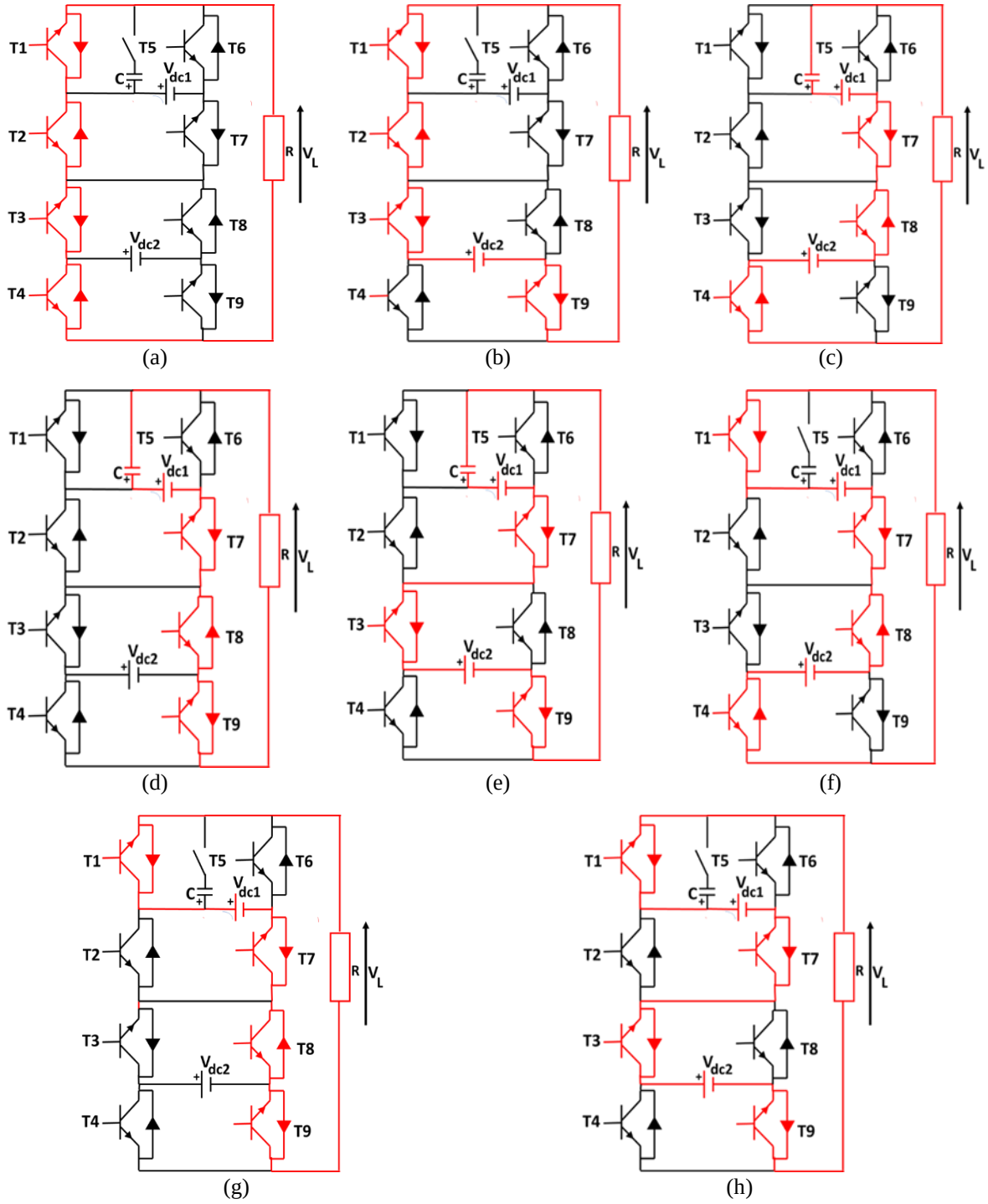

Figure 3. Switching configurations of the inverter corresponding to null and positive voltage states: (a) 0 V level, (b) V_{dc} level, (c) 2 V_{dc} level, (d) 3 V_{dc} level, (e) 4 V_{dc} level, (f) 5 V_{dc} level, (g) 6 V_{dc} level, and (h) 7 V_{dc} level

2.2. Mathematical model of the proposed topology

It is considered that the power switches of the proposed topology operate ideally.

$$Si\ is\ disabled\ if \quad S_i = 0 \tag{1}$$

$$Si\ is\ enabled\ if \quad S_i = 1 \tag{2}$$

for each switching configuration, the inverter output voltage is computed as a function of V_{dc1}, $V_{dc2,}$ and V_C from the topological structure as:

$$V_L = V_{dc2}(T_9 - T_8) + T_5 V_c + V_{dc1}(T_1 - T_2) \quad (3)$$

For a load (R–L), load voltage versus load current is expressed by (4):

$$V_L = Ri + L\frac{di}{dt} \quad (4)$$

Taking into account that V_C=3 V_{dc}, V_{dc1}=6 V_{dc}, and V_{dc2}=$V_{dc,}$ (5) becomes to generates the fifteen voltage levels:

$$\frac{di}{dt} = \frac{((T_9 - T_8) + 3T_5 + 6(T_1 - T_2))V_{dc} - Ri}{L} \quad (5)$$

2.3. Voltage stress

In the proposed 15-level inverter, the circuit comprises nine switches, including one bidirectional switch. The voltage blocking requirements for each device are determined based on the different operating states of the suggested inverter. The individual voltage stresses are as follows:

$$V_{T1}=V_{T2}=V_{T6}=V_{T7}=V_{dc1} \quad (6)$$

$$V_{T5}=V_C \quad (7)$$

$$V_{T3}=V_{T4}=V_{T8}=V_{T9}=V_{dc2} \quad (8)$$

The TBV experienced by the semiconductor devices is expressed by:

$$TBV=4V_{dc1}+V_C+4V_{dc2} \quad (9)$$

For the voltage ratios used in this work, V_{dc1}=6V_{dc}, V_C=3$V_{dc,}$ and V_{dc2}=V_{dc}, the TBV is calculated as:

$$TBV=31V_{dc} \quad (10)$$

This value is lower than in conventional asymmetric multilevel topologies with similar voltage levels, making the proposed inverter suitable for medium-voltage applications with reduced component voltage ratings. It must be used subsequently in the comparative study, which must be presented in the following part.

2.4. Comparative study

A detailed comparison is carried out between the proposed inverter and other recently introduced topologies. The evaluation focuses on crucial design parameters such as the number of DC sources (N_{dc}), capacitors (N_c), switches (N_{sw}), diodes (N_d), and the total standing voltage per unit (TSVpu) across all switching devices. To facilitate a fair and meaningful evaluation, a cost function (F_c) is introduced. This function reflects the economic impact of each topology by accounting for the quantity of power components. A weighting factor α is used within the cost function to emphasize the relative importance of TSV compared to the total component count. In the proposed cost function, the weighting factor α balances the impact of the TSVpu and the number of components. In this work, α is set to 1 to give them comparable importance while keeping the cost metric simple and consistent across the compared topologies. Additionally, TSVpu is used as a normalized index to evaluate the cumulative voltage stress. It is calculated by dividing the sum of voltage stresses across all switches by the peak output voltage of the inverter:

$$\text{TSVpu} = \frac{TBV}{V_{max}} = \frac{31V_{dc}}{7V_{dc}} = 4.43 \quad (11)$$

To quantify the economic impact of the design, the cost function is defined as:

$$F_c = \frac{(N_{sw} + N_d + N_c + (\text{TSVpu})\alpha)N_{dc}}{N_L} \quad (12)$$

An additional performance metric is the device-per-level ratio (F_L), which is formulated as:

$$F_L = \frac{N_{sw}+N_d+N_c+N_{dc}}{N_L} \quad (13)$$

This parameter reflects the number of active components required per output level and serves as a practical indicator of circuit complexity and implementation cost. Since each semiconductor switch typically requires additional support circuits, F_L becomes a crucial factor in evaluating and comparing the overall design efficiency of multilevel inverters.

Table 2 compares our new topology with other multilevel converter designs from recent studies. These previous designs, published between 2020 and 2024, all produce 7 voltage levels. What makes our design different is that it creates 15 voltage levels while keeping the circuit simple and practical.

Examining the performance numbers, our topology operates more efficiently than expected. It has an N_{sw}/N_L ratio of 0.66, which beats all the other designs we tested. This means we're getting better results with fewer switching components. Our topology delivers a cost function (F_c) of 2.05, the lowest value we achieved, far below the 2.30-2.85 range found in other topologies.

Our architecture establishes a unit blocking voltage (TSVpu) of 4.43, an appropriate value that ensures good operational reliability. Our design outperforms other topologies (range 1.70-2.14) with a component-to-level ratio (F_L) of 0.87, thus enabling minimal switch usage per level and substantially reducing associated switching losses.

Our topology takes a different path by employing two DC sources, where others typically use one. This strategic choice enables us to generate fifteen voltage levels while maintaining a low component count. We've essentially found the optimal middle ground between achieving excellent performance, maintaining design simplicity, and ensuring operational dependability.

Table 2. Comparison with other topologies

Topology	Year	N_L	N_{dc}	N_c	Nsw	N_d	F_L	N_{sw}/N_L	TSVpu	$F_C(\alpha=1)$
[20]	2023	7	1	2	8	1	1.7	1.14	5.30	2.3
[21]	2023	7	1	2	8	3	2	1.14	6	2.71
[22]	2021	7	1	3	11	0	2.14	1.57	6	2.85
[23]	2020	7	1	3	9	0	1.85	1.28	5	2.42
[24]	2020	7	1	2	10	0	1.85	1.42	6	2.57
[25]	2020	7	1	3	8	0	1.71	1.14	7.3	2.75
[26]	2024	7	1	2	7	2	1.70	1	5.33	2.45
Proposed	----	15	2	1	10	0	0.87	0.66	4.43	2.05

N_L: number of levels, N_{dc}: number of DC sources, N_c: number of capacitors, N_{sw}: number of switches, N_d: number of diodes, F_L: device-per-level ratio, TSVpu: Total Standing Voltage per unit, F_c: cost function.

2.5. Control strategy of H-PTC inverter

The proposed control, as shown in Figure 4, uses a predictive controller that processes voltage reference signals $V_L^*(k)$, along with feedback measurements of load voltage $V_L(k)$ and load current $i_L(k)$. Through discrete cost function minimization over a single prediction step, the controller determines the optimal switching sequence (S) for the inverter to supply the load, with both voltage and current measurements providing closed-loop feedback for system regulation. This methodology assesses all feasible switching combinations, eliminating the need for state observers and thereby achieving superior efficiency while maintaining excellent performance for real-time power electronic system applications. To simplify implementation, the inverter is considered a system with a limited number of switching state vectors S_i, each associated with a specific output voltage level. At each sampling instant k, all possible switching states are examined, and the most optimal one is selected based on a predefined cost function.

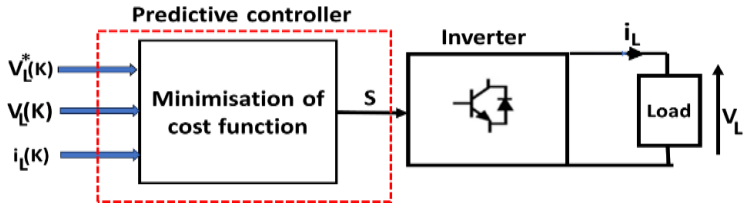

Figure 4. The block diagram of MPC

2.5.1. Cost function definition

At each sampling instant k, the control algorithm computes a cost function to evaluate the deviation between the reference voltage and the predicted voltage corresponding to each switching state. The cost function is expressed by (14):

$$g(k) = \left(V_{ref}(K) - V_i(k)\right)^2 \quad (14)$$

$V_{ref}(K)$ is the reference voltage at time k, $V_i(k)$ is the predicted inverter output voltage for the switching state (i), and g(k) is the scalar cost associated with state (i). This quadratic form ensures a minimum tracking error of the reference waveform.

2.5.2. Optimal switching low

The control objective is to select the switching state that minimizes the cost function and generates an output voltage close to the reference, and this can be expressed as:

$$S_{opt}(K) = \arg\min_{S(k)\in S}\left(\left(V_{ref}(K) - V_i(k)\right)^2\right. \quad (15)$$

2.5.3. Control low execution

The control strategy employs a predictive regulator using the voltage reference V_L*(k) and closed-loop measurements of output voltage $V_L(k)$ and load current $i_L(k)$. At each sampling instant, the future voltage $V_L(k+1)$ is predicted for all possible switching states (Table 1). A cost function is evaluated for each candidate state, and the one minimizing it is applied in the next period. The switching table links each configuration to a specific voltage level and indirectly governs the charging and discharging of the capacitor, enabling dynamic voltage balancing. This approach evaluates all feasible switching options directly, eliminating the need for observers and ensuring high dynamic performance. The proposed predictive controller is operated with a sampling period of Ts = 50 µs, which is consistent with the converter dynamics and the desired switching frequency. A single-step prediction horizon is adopted to limit the computational burden while preserving satisfactory dynamic performance. At each sampling period k, the MPC control loop operates as follows: (a) Measure the output voltage $V_L(k)$ and load current $i_L(k)$; (b) Predict the future output voltage $V_L(k+1)$ for all possible switching states (as listed in Table 1); (c) Calculate the cost function g(k) for each state; (d) Select the switching state that minimizes the cost for the next cycle.

3. RESULTS AND DISCUSSION

To validate the efficacy of applying MPC to the proposed inverter, several simulation scenarios were performed using MATLAB/Simulink. Initially, the inverter was tested under constant operating parameters to evaluate its baseline performance. Subsequently, its behavior was assessed under varying conditions to examine the robustness and adaptability of the control strategy.

3.1. Simulation under fixed parameters

The key simulation parameters are listed in Table 3. Figure 5 shows the waveforms of the load voltage V_L, the capacitor voltage V_C, and the load current. Figure 5(a) demonstrates the regulation of the capacitor voltage toward its desired value. The voltage V_C achieves steady-state operation at approximately half of V_{dc1}, validating the performance of the proposed control strategy. This figure also depicts the output voltage V_L waveform produced by the multilevel inverter topology. The H-PTC inverter successfully generates fifteen discrete voltage levels, as evidenced in the graphical representation. This multi-level approach yields an output waveform with near-sinusoidal characteristics. Figure 5(b) displays the load current waveform, exhibiting superior sinusoidal quality. This performance metric is substantiated by the remarkably low THD achieved in the simulation results. The harmonic spectrum analysis presented in Figure 6 validates the outstanding performance characteristics of the developed system. The output voltage THD measures 5.58% (Figure 6(a)), while the load current THD achieves an exceptional value of 0.88% (Figure 6(b)). These measurements verify the superior waveform quality and adherence to power quality standards.

Table 3. The simulation parameters

Parameters	V_{dc1}	V_{dc2}	R	L	Capacitor C	Switching frequency f
Values	360 V	180 V	20 Ω	20 mH	1000 uF	20 KHz

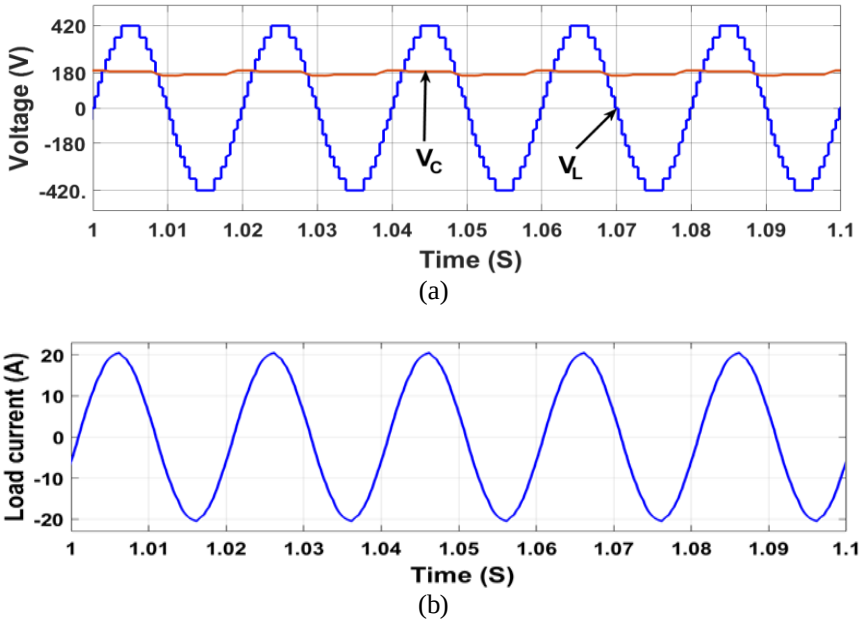

Figure 5. Waveforms of (a) load voltage V_L and capacitor voltage V_C and (b) load current

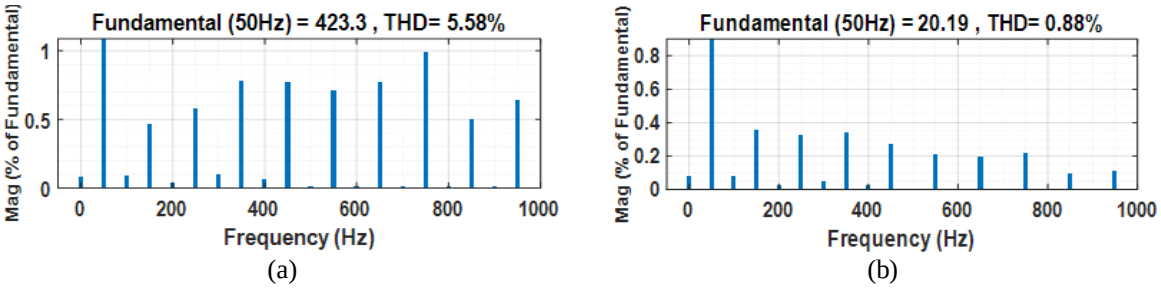

Figure 6. Fast fourier analysis of (a) the load voltage and (b) the load current

3.2. Changing load operation

To validate the dynamic behavior of the proposed fifteen-level H-PTC inverter, an additional simulation was conducted. At t=7 S, the load resistance was adjusted from 20 Ω to 50 Ω, while the load inductance was also increased from 20 mH to 50 mH. As shown in Figure 7, the capacitor voltage quickly rebalances after this load variation. The voltage V_c stabilizes at approximately half of the voltage V_{dc1}, enabling the generation of the fifteen-level output voltage, maintained before and after the load change, as illustrated in the same figure. Furthermore, Figure 8 shows the load current waveform, which remains nearly sinusoidal before and after this load variation.

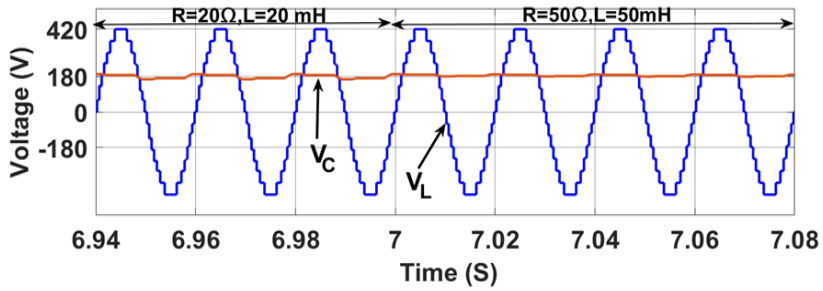

Figure 7. Waveforms of load voltage V_L and capacitor voltage V_C during load change

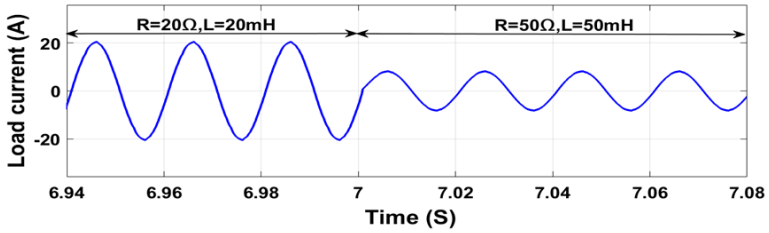

Figure 8. Waveform of load current during load change

3.3. Operation with a nonlinear load

The suggested inverter was examined under nonlinear load conditions. Initially, the load was purely resistive, consisting of a linear resistor. At t=7s, a nonlinear load, implemented as a diode H-bridge, was connected to the inverter output. As illustrated in Figure 9, the capacitor voltage remained balanced around the reference value despite the load transition. Moreover, the output voltage waveform remained largely unchanged during this transition, demonstrating the fifteen-level voltage generation.

Figure 10 presents the load current waveform, which, although slightly distorted due to the nonlinear nature of the connected load, retains a nearly sinusoidal shape. This observation is further supported by the THD values under resistive loading, which was 5.69%, and it slightly increased to 5.98% when the nonlinear load was applied. This minimal variation confirms the performance of the inverter's control approach, even in the presence of harmonics induced by nonlinear components.

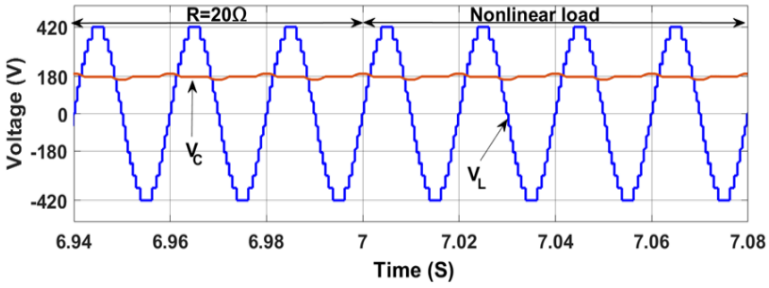

Figure 9. Waveforms of load voltage V_L and capacitor voltage V_C during nonlinear load operation

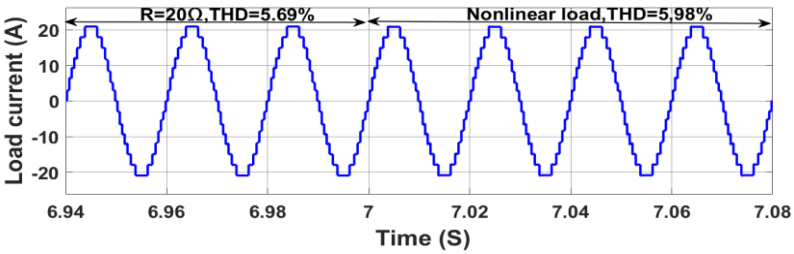

Figure 10. Waveform of load current during nonlinear load operation

3.4. Operation with DC source variation

The proposed concept is also validated under sudden variations of the DC source voltages, a change is applied at t = 7 s, where V_{dc1} drops instantly from 360 V to 180 V, while V_{dc2} decreases from 60 V to 30 V. The evolution of the capacitor voltage as well as the load voltage, before, during, and after this change, is illustrated in Figure 11. Before the change in the DC sources, the capacitor voltage is properly balanced around the desired value (Figure 11(a)), which corresponds to half of V_{dc1}. Following the change, a transient period is observed during which the capacitor voltage converges towards its new reference value. After a short duration, the capacitor voltage stabilizes around the new expected value (Figure 11(b)), thereby enabling the generation of a high-quality fifteen-level load voltage. Moreover, the load current remains sinusoidal during the variation of the DC sources. During the transient phase, a slight distortion appears in the current waveform due to the variation in the capacitor voltage during this period. However, after a few milliseconds, the current returns to a nearly sinusoidal shape, as illustrated in Figure 12.

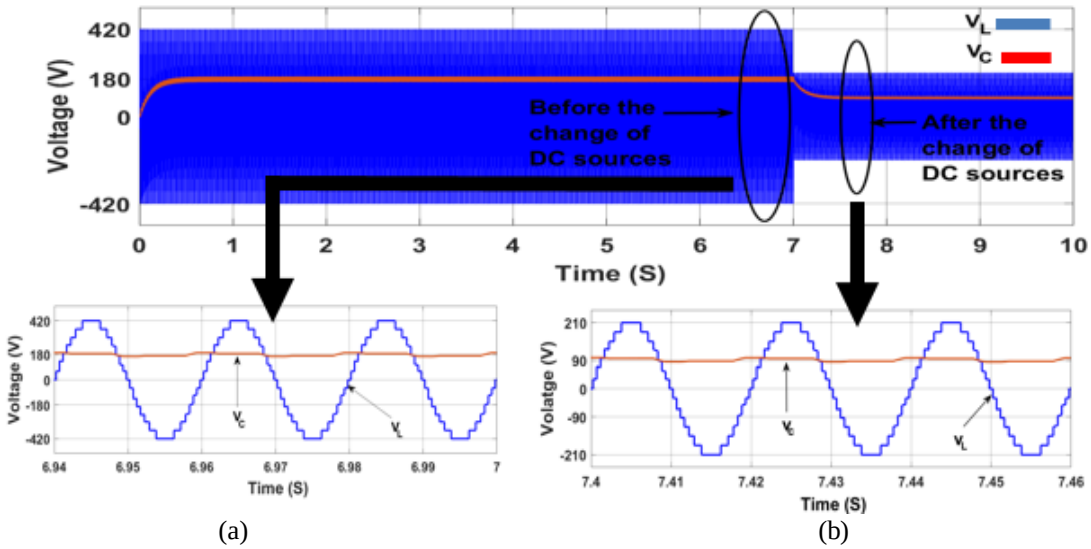

Figure 11. The waveforms of the load voltage V_L and capacitor voltage V_C (a) before the change of DC sources and (b) after the change of DC sources

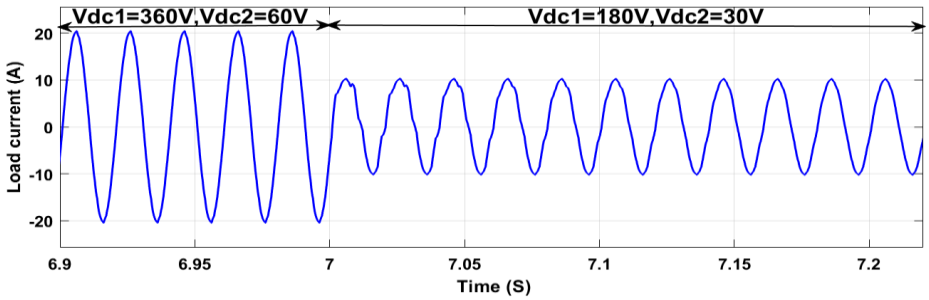

Figure 12. The waveform of the load current during the change of DC sources

4. CONCLUSION

This work presents a fifteen-level H-PTC inverter topology controlled by MPC with a reduced component count, lowering implementation cost and improving reliability compared to conventional multilevel inverters. Simulation results under various operating conditions show that the proposed scheme maintains capacitor voltage balance, produces low-distortion fifteen-level waveforms with fast transient response, and achieves lower TSV. Although we do not have experimental results or a detailed thermal analysis, a simplified loss estimation indicates the expected performance. The proposed topology, which uses only nine IGBTs and a single floating capacitor, mainly leads to three types of thermal losses: conduction losses in the switches, switching losses at an effective frequency close to 20 kHz, and losses associated with the current ripple in the capacitor (capacitor ripple losses). Based on the simulated current levels and realistic assumptions about the components, these losses are expected to remain at a few percent of the output power, suggesting a theoretical efficiency above 96%, pending confirmation through experimental or HIL validation.

While the proposed topology offers substantial benefits, it also has inherent limitations. The unity voltage gain may restrict its application in systems requiring significant voltage boosting. In addition, the absence of a common reference point can cause leakage and common-mode currents, especially critical in PV and grid-connected systems due to parasitic capacitances between the generator, cables, and ground. These effects can be mitigated through modulation or predictive control strategies that limit common-mode voltage, EMI filters with common-mode chokes, and, where appropriate, isolation transformers and suitable grounding. We view these challenges as opportunities for further refinement and practical optimization.

Future work will integrate the proposed topology into grid-connected renewable energy systems, where grid synchronization, PV leakage currents, and common-mode voltage mitigation are critical for stability and safety. Additionally, a real-time MPC prototype will be built to perform detailed analytical and numerical evaluation of conduction and switching losses.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

Simulation data related to this study are available from the corresponding author.

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