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Wirelength estimation for VLSI cell placement using hybrid statistical learning

Joyce Ng Ting Ming[1], Ab Al-Hadi Ab Rahman[1], Nuzhat Khan[1], Muhammed Paend Bakht[2], Shahidatul Sadiah[1], Mohd Shahrizal Rusli[3], Muhammad Nadzir Marsono[1]
[1]Faculty of Electrical Engineering, Universiti Teknologi Malaysia (UTM), Johor Bahru, Malaysia
[2]Department of Electrical Engineering, Balochistan University of Information Technology, Engineering and Management Sciences (BUITMS), Quetta, Pakistan
[3]Faculty of Artificial Intelligence, Universiti Teknologi Malaysia (UTM), Kuala Lumpur, Malaysia

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ABSTRACT

Optimizing wirelength involves predicting the total length of wires needed to connect different components within a chip during cell placement. It is a fundamental challenge in very-large-scale integration (VLSI) of integrated circuit (IC) design, as it directly impacts the overall performance and manufacturability of chips. Accurate wire-length estimation in the early stages of the design process is critical for guiding subsequent optimization tasks. This paper proposes a novel hybrid linear regression wirelength (hybrid-LRWL) method that combines the strengths of existing methods rectilinear Steiner minimal tree (RSMT) for low-degree nets and a statistical learning-based approach for high-degree nets. Additionally, it compares the performance of three well-established wirelength estimation techniques: half-perimeter wirelength (HPWL), rectilinear minimum spanning tree (RMST), and RSMT. The methods were evaluated using the International Symposium on Physical Design (ISPD) 2011 benchmark suite, considering accuracy and computational efficiency. The experimental results demonstrated that the proposed hybrid method achieves superior accuracy, with a mean error of less than 0.05% in total wirelength, closely approximating RSMT results. The proposed method reduces computational time up to 3.6 times faster than traditional RSM-based methods. The results establish a strong framework for accurate and efficient wirelength estimation in VLSI design for modern, high-performance ICs.

Corresponding Author:

Ab Al-Hadi Ab Rahman
Faculty of Electrical Engineering, Universiti Teknologi Malaysia (UTM)
81300 Johor Bahru, Johor, Malaysia
Email: hadi@utm.my

1. INTRODUCTION

Integrated circuit (IC) design is the process of creating electronic circuits to be implemented on a chip. With the rapid evolution of IC designs, the complexity of modern circuits has increased dramatically, transitioning from small-scale integration (SSI) to very large-scale integration (VLSI) containing billions of transistors. As IC designs become more complex, the challenge of utilizing circuit components on a chip has become increasingly critical. In modern VLSI designs [1] billions of transistors [2], logic gates [3], and other components are integrated into a single chip [4]. The arrangement and design of these components not only affect the overall performance of the chip but also impact key design metrics such as wirelength, power consumption [5], and timing [6].

In the early stages of IC design, an accurate wirelength estimation is required to determine the physical connections between modules. From pre-estimated wirelength, designers assess the feasibility and performance of different design choices. It helps them quickly optimize delays along signal paths [7]. Since actual routing solutions are precise but computationally expensive and impractical for early-stage evaluations [8]. As a result, wirelength estimation methods are an efficient alternative for designers to evaluate placement quality without the need for complete routing execution [9].

Several established techniques, such as half-perimeter wirelength (HPWL) [10] rectilinear minimum severance tree (RMST) and rectilinear Steiner minimal tree (RSMT) [11] are widely used in wirelength estimation. However, these methods often involve trade-offs between speed and accuracy. For example, HPWL offers speed but at the expense of accuracy, while RSMT, though more accurate, suffers from increased computational complexity, particularly for high-degree nets [12]. As circuit designs grow in scale and complexity, there is a pressing need for wirelength estimation methods that strike a better balance between runtime efficiency and accuracy. Despite the widespread use of these methods, their applicability, and limitations in research-based cell placement with more standard benchmark circuits, the ISPD 2011 benchmark suite [13] are not fully understood. Previous studies relied primarily on older benchmarks, such as the IBM ISPD 2004 suite [14] leaving a gap in evaluating these estimation techniques on more modern circuit designs. Additionally, efforts to combine the strengths of existing methods for complex designs are lacking.

This study addresses this gap by introducing a novel hybrid estimation technique. The proposed technique combines the accuracy of RSMT for low-degree nets with a statistical learning-based approach for high-degree nets. By incorporating a hybrid method, this study aims to improve the accuracy and computational efficiency of wirelength estimation and offers a more practical solution for modern VLSI design. It effectively addresses the run-time challenges associated with RSMT in large-scale designs. Similarly, it implements, evaluates, and compares the performance of several existing wirelength estimation methods in the ISPD 2011 benchmark suite. The contributions of this research are twofold: first, the development of a hybrid technique that significantly enhances performance, and second, a comprehensive evaluation of existing wirelength estimation methods on newer benchmark ISPD 2011.

2. BACKGROUND

This section presents the existing wirelength estimation methods in VLSI placement, specifically the HPWL, RMST, and RSMT. In addition, the ISPD-2011 benchmark suite used in the present work is also described.

2.1. Wirelength estimation methods

The three classical wirelength estimation methods, HPWL, RMST, and RSMT are shown in Figure 1. HPWL estimates wirelength by calculating the half-perimeter of the bounding box that encloses all pins of a net. The bounding box is the smallest rectangle covering all the net pins. Each net is iterated to find the minimum and maximum pin coordinates, and the bounding box dimensions are computed. The wirelength for each net is then calculated as the sum of the bounding box's width and height [15]. The formula for HPWL is given by:

$$HPWL_{\{\varepsilon\}} = (\max\{x_i\} - min\{x_i\}) + (max\{y_i\} - min\{y_i\}) \quad (1)$$

where i and e represent all pins and nets, while (x_i, y_i) is the coordinate for a given block. The total HPWL in the netlist is thus:

$$HPWL = \sum_{e \epsilon E} HPWLe \quad (2)$$

Which is the sum of the HPWL of each net e in the design floorplan. The pins of a net in the given netlist are traversed in a loop to store the minimum x-coordinate of a pin, y-coordinate (w_i, y_i) and maximum x-coordinate of a pin, and y-coordinate (x_i , y_i). The length of the bounding box tot_x (H) is computed as max (x_i) -min (x_i) while the width of the bounding box toty (W) is computed as max (y_i) – min(y_i). The total wirelength, WL_{total} of the net, is calculated as (3).

$$WL_{total} = T_{totx} + T_{toty} \quad (3)$$

Where x_i and y_i are the coordinates of pins within the net e, the total HPWL is computed by summing the HPWL values of all nets [16].

The process for calculating HPWL involves iterating over the pins of each net, determining the minimum and maximum x and y coordinates, and computing the half-perimeter of the bounding box formed by these coordinates. An example of computing the HPWL is given in Figure 1(a). The HPWL technique is widely used for wirelength estimation due to its simplicity and efficiency. It approximates the wirelength as half the perimeter of the bounding box, which encloses all pin locations [16]. While HPWL accurately estimates wirelength for 2-terminal and 3-terminal nets, its scalability diminishes as the net degree exceeds 4, resulting in significant underestimation. For 4-terminal nets, HPWL predicts wirelength 33% less accurately than the rectilinear minimum spanning tree (RMST) [17]. Experimental results empirically demonstrated that the HPWL model fails to accurately approximate routing wirelength, leading to significant sub-optimality [18].

RSMT uses the sequential Steiner tree heuristic on the Hanan grid [11], including all vertical and horizontal intersections passing through terminal pins. The algorithm iterates through the pins to construct the Steiner tree by finding the closest pairs of points and connecting them, adding Steiner points when beneficial [9]. RSMT is a key technique used for wirelength estimation in VLSI design because it provides a precise measure compared to conventional methods. RSMT uses Steiner points to minimize the total rectilinear distance for connecting terminals. This approach significantly reduced the overall wirelength, as seen in the example of RSMT computation in Figure 1(b).

On the other hand, RMST provides a good approximation of wirelength with reasonable processing time [19]. RMST utilizes Manhattan geometry and achieves a runtime complexity of O(nlogn) [20]. However, it typically adopts a simple O(n2) implementation when the degree of nets is small. As discussed in [21], this approach can result in longer wirelength estimations than RSMT, as it does not allow for branching, potentially leading to RMST lengths up to 1.5 times that of RSMT. Meanwhile, RSMT is known for its high accuracy in wirelength estimation, but it comes at the cost of long runtime due to its complex algorithm. RSMT permits branching at any point [22], known as the Steiner point, along the path. Several works have aimed to improve the runtime of RSMT, such as the development of the FLUTE tool in [23], which optimizes RSMT computations and the extensions of RSMT to include obstacles through a multi-level approach in [20] and [24]. An example of computing the RMST algorithm for a three-pin net is given in Figure 1(c).

Each method presents trade-offs: HPWL is the fastest but least accurate, RMST offers a balance between speed and accuracy but often overestimates, while RSMT is the most precise but computationally expensive. To address these limitations, the proposed Hybrid-LRWL method strategically integrates classical approaches with statistical learning to achieve both efficiency and precision in wirelength estimation.

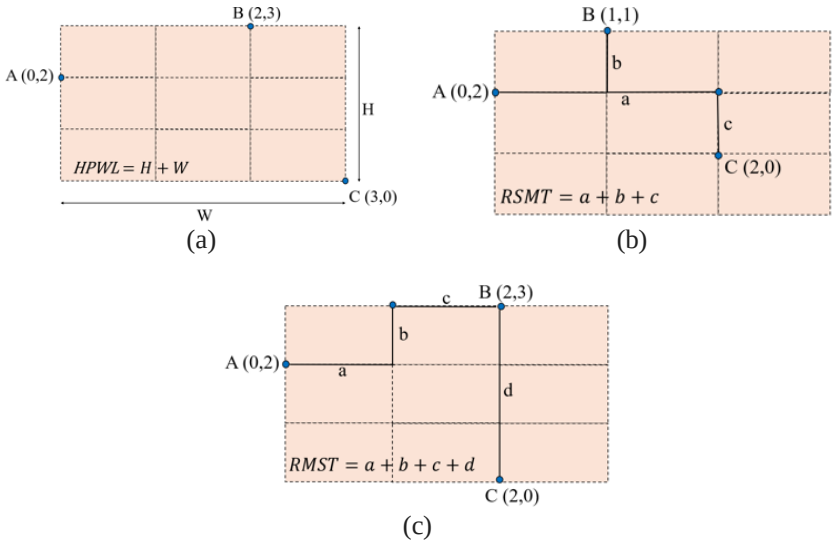

Figure 1. Example of (a) HPWL, (b) RSMT, and (c) RMST algorithms to estimate the wirelength between nodes A, B, and C

2.2. ISPD-2011 Benchmark Suite

The ISPD 2011 Benchmark Suite is designed to evaluate VLSI placement and routing algorithms focusing on routability. It includes 10 placement benchmarks based on real-world ASIC designs, featuring up

to 5.7 million instances and 210,000 nets. It also provides 5 routing benchmarks, each presenting challenges such as varying densities, wire lengths, and via counts. These benchmarks are standardized test cases to assess placement and routing tools under diverse and complex design conditions.

The experiment utilizes data from the ISPD 2011 Benchmark Suite, which includes multiple input files that provide essential circuit layout details. These files contain benchmark configurations, node information such as count, size, and type, non-rectangular node shapes, placement coordinates, placement row details, net connections, and final node placement solutions. The information from these files was stored in dictionaries to facilitate efficient access throughout the wirelength estimation and legalization processes. The experiments were performed using Python on a system equipped with a 12th Gen Intel® Core™ i5-12400F processor (2.50 GHz), 64 GB of RAM, and an NVIDIA GeForce RTX 3060 GPU (driver version 560.94), running a 64-bit operating system. The key characteristics of the selected designs from the ISPD 2011 Benchmark Suite are provided in Table 1.

Table 1. The key characteristics from the ISPD 2011 Benchmark Suite

Design	Total nodes	Movable nodes	Terminal nodes	Terminal NI nodes	Total nets	Total pins
Superblue1	847,441	765,102	52,627	29,712	822,744	2,861,188
Superblue2	1,014,029	921,273	59,312	33,444	990,899	3,228,345
Superblue4	600,220	521,466	40,550	38,204	567,607	1,884,008
Superblue5	772,457	677,416	74,365	20,676	786,999	2,500,306
Superblue10	1,129,144	914,921	153,595	60,628	1,085,737	3,665,711
Superblue12	1,293,433	1,278,084	8,953	6,396	1,293,436	4,774,069
Superblue15	1,123,963	829,614	252,053	42,296	1,080,409	3,816,680
Superblue18	483,452	442,405	25,063	15,984	468,918	1,864,306

3. METHOD

This section describes the key concepts and methodology in developing a wirelength estimation algorithm and performance evaluation to facilitate the VLSI chip development flow. The study proposes a hybrid approach for wirelength estimation. It also implements traditional wirelength estimation techniques for evaluation and comparison on ISPD 2011 Benchmark Suite. The proposed methodology follows a structured flow that integrates benchmark data preprocessing, implementation of wirelength estimation algorithms, and result computation. The process consists of several key steps: data parsing, algorithm execution, and result comparison. The general workflow aims to optimize wirelength estimation using hybrid HPWL and RSMT technique. The objective is to combine the strengths of various traditional methods to maximize speed and accuracy while optimizing computational complexity.

As discussed before, the limitation of existing methods is net degree. RSMT is suitable for low-degree nets but less efficient with high-degree nets. Therefore, this work introduces a hybrid wirelength estimation method that integrates RSMT and statistical learning-based methods (SLM). A net degree threshold was chosen based on runtime and data analysis. The hybrid method selectively applied algorithms based on net characteristics, such as net degree and pin distribution. For nets with lower degrees than the threshold, the model dynamically selected RSMT as it becomes computationally expensive for higher-degree nets. In contrast, HPWL based on statistical learning has been employed to reduce computational complexity for higher-degree nets above the threshold. The motivation behind this approach was to address the limitations of HPWL in handling high net degrees, where significant deviations from actual wirelength values can arise. A direct RSMT calculation was computationally intensive and less efficient for high-degree nets above the threshold. Instead, a line regression model estimated the wirelength by examining the deviation between HPWL and RSMT values. The regression model used an exponential fit derived from (4).

$$Y = -0.913 \ln(x) + 9.8787 \quad (4)$$

Where x represents the HPWL, a commonly used, more straightforward estimation metric that sums the horizontal and vertical extents of a bounding box enclosing the nodes of a net, and Y represents the rate of deviation, quantifying how much the HPWL underestimates or overestimates the wirelength compared to the RSMT for high-degree nets [25]. The model effectively adjusts the HPWL estimation for high-degree nets by applying the calculated deviation factor. This correction accounts for the observed deviations between HPWL and RSMT, particularly as net complexity increases.

From the net degree data of the ISPD-2011 benchmark circuits, those with a degree above D have been taken for analysis, and the HPWL and RSMT for each net have been calculated for the placed circuits. The threshold of net degree D=1,000 has been selected as a net degree less than this value, which can be

quickly and accurately calculated using RSMT. The HPWL deviations with respect to RSMT have been plotted for each of the nets, as shown in Figure 2.

The wirelength optimization process is detailed in Algorithm 1. It takes in all the nets and pins, threshold D, and line regression function LG and returns the total wirelength for the overall design. For each net, it first checks the degree. If it is less than the threshold, the RSMT method estimates wirelength. Otherwise, the wirelength is estimated using a correction based on the line regression function.

Algorithm 1. Proposed line regression algorithm

```
Procedure HYBRID-LRWL(nets N , set of all pins P , total T , threshold degree D, Line regression
        function LG)
Initialise wirelength function W .
for each N do
      if N 's degree < D then
      W←RSMT
      else if N 's degree > D then
      W ←HPWL × (1 + LG(HPWL))
      end if
         T ← T + W
end for
return T
End Procedure
```

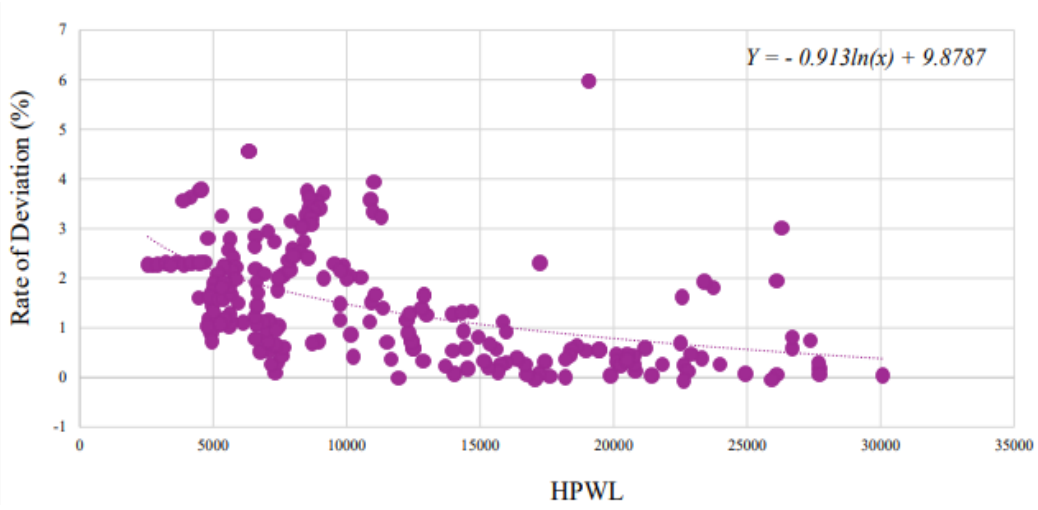

Figure 2. Line Regression is derived from HPWL, and its mean deviation from RSMT is for a net degree of more than 1,000

4. RESULTS AND DISCUSSION

The proposed hybrid algorithm is implemented in Python, and performance evaluation is performed using different benchmarks. The results are compared to traditional methods regarding wirelength accuracy and computational efficiency. The evaluation uses solution placements from the ISPD 2011 benchmark suite, focusing on average runtime and error rates. The comparison revolved around two aspects: speed and accuracy. The performance of the proposed methods was validated using the Superblue-4 design to ensure robustness, while statistical learning training utilizes the other Superblue Benchmark circuits. Detailed results demonstrating the superiority of the hybrid method over traditional techniques are provided in subsequent sections.

4.1. Runtime analysis and comparison

The efficiency of the proposed hybrid-LRWL method was evaluated by measuring the time required to estimate wirelengths for all 567,607 nets in the Superblue-4 benchmark circuit. The results, shown in Figure 3, indicate that Hybrid-LRWL takes 1,069.9 seconds, which is significantly faster than the RSMT method, which takes 3,829.3 seconds, approximately 3.6 times longer. The key reason for this speed improvement is the hybrid approach used in hybrid-LRWL. Instead of applying the complex and computationally expensive RSMT method to all nets, hybrid-LRWL selects the appropriate technique based

on net complexity. It applies RSMT only to low-degree nets (nets with fewer connections) to maintain accuracy. In contrast, high-degree nets (nets with many connections) are handled by a faster statistical learning model, which has been trained on previous placement data. This allows hybrid-LRWL to reduce computation time while maintaining accuracy significantly.

However, when comparing hybrid-LRWL to more straightforward wirelength estimation techniques, such as HPWL and RMST, we see that HPWL takes only 2.5 seconds, and RMST takes 599.7 seconds. HPWL is the fastest because it uses a simple bounding box method to estimate wirelength, but this comes at the cost of lower accuracy. RMST is more advanced and requires more computation, but it still does not reach the accuracy of RSMT. Although Hybrid-LRWL is not the fastest method, it optimizes computation time and accuracy. It is well suited for modern circuit design, where speed and precision optimization are both essential.

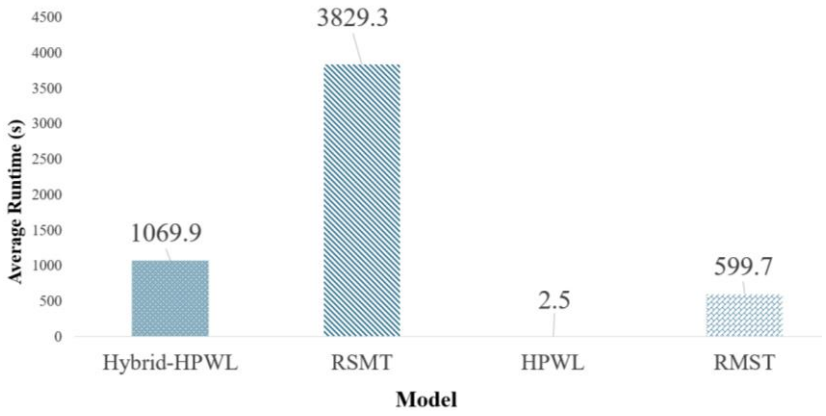

Figure 3. Runtime of the proposed method and traditional techniques

4.2. Accuracy analysis and comparison

The mean error-based performance characteristics of each method are highlighted in Figure 4 for the Superblue-4 benchmark circuit. The wirelength estimation error for each of the 567,607 nets for RSMT is calculated and averaged for wirelength techniques RMST, HPWL, and the proposed Hybrid-LRWL. In this case, RSMT is set to be ground truth with a zero percent error.

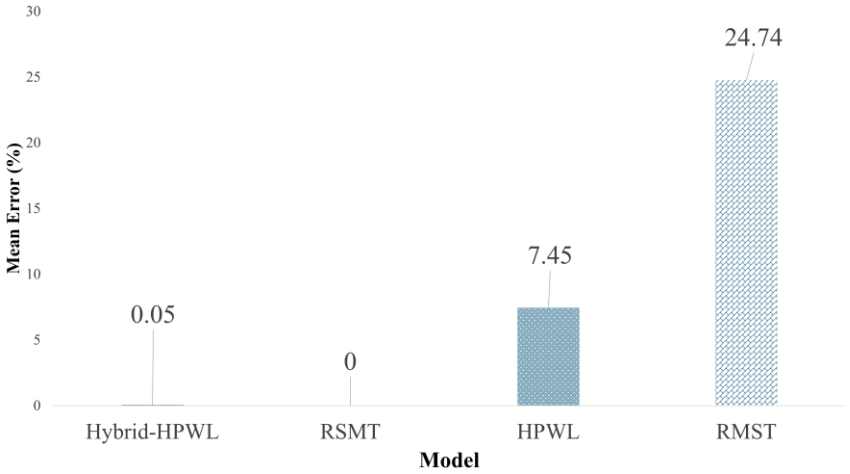

Figure 4. Comparison of mean errors of wirelength estimation methods

The hybrid-LRWL method achieves an exceptionally low error of just 0.05%, significantly outperforming HPWL (7.45%) and RMST (24.74%). The high error rate of RMST suggests that it tends to overestimate wirelengths, especially in circuits with dense layouts and many overlapping connections. This is

because RMST does not fully capture the optimized net structures used in actual circuit routing. HPWL, while much faster, also suffers from estimation inaccuracies due to its simple rectangular bounding box approach, which does not account for detailed routing paths. HPWL performs better than RMST but fails to accurately model wirelength in complex circuit designs, especially when many closely packed nets introduce congestion.

In contrast, hybrid-LRWL achieves near-perfect accuracy by strategically combining two techniques. A precise RSMT method is used for low-degree nets to ensure accuracy where it matters most. High-degree nets rely on a trained statistical learning model, which predicts wirelength based on previous circuit designs. This hybrid strategy effectively minimizes errors while keeping the computation time manageable.

To ensure the robustness of hybrid-LRWL, additional tests were conducted using different Superblue benchmark circuits, confirming that the method consistently maintains high accuracy across various designs. Combining machine learning and traditional estimation techniques makes hybrid-LRWL a strong candidate for future improvements, such as enhancing its statistical learning model with more training data, optimizing its runtime even further, and integrating it with congestion-aware routing algorithms. These findings demonstrate that Hybrid-LRWL is highly accurate and practical for real-world circuit design, where fast and precise wirelength estimation is crucial for optimizing performance, reducing delays, and improving overall chip efficiency.

5. CONCLUSION

This study introduced the hybrid-LRWL method, a novel wirelength estimation approach that combines traditional models with statistical learning to achieve accuracy and efficiency. Unlike fixed estimation techniques such as HPWL, RMST, and RSMT, the proposed method dynamically adapts its strategy based on net complexity, optimizing performance while reducing computational overhead. Experimental results demonstrate its effectiveness, achieving up to 3.6× faster computation than RSMT while maintaining a mean error below 0.1%, addressing the long-standing trade-off between speed and precision in wirelength estimation.

The significance of this work extends beyond wirelength estimation itself. By integrating statistical learning into classical VLSI design methodologies, hybrid-LRWL demonstrates how adaptive hybrid models can enhance EDA tool efficiency, improve scalability, and reduce design bottlenecks. The ability to selectively apply estimation strategies based on circuit complexity offers a more refined and intelligent approach to wirelength prediction, making it particularly relevant for modern large-scale chip designs.

Future research should explore extending this framework by incorporating nonlinear optimization techniques, refining statistical models to handle even more complex net structures, and integrating the approach into real-time placement and routing algorithms. Additionally, investigating its compatibility with AI-driven EDA workflows could lead to fully automated, high-precision design pipelines, ultimately pushing the boundaries of computational efficiency in semiconductor design. By building on this foundation, hybrid-LRWL has the potential to set a new standard for wirelength estimation in advanced VLSI systems.

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AUTHOR CONTRIBUTIONS STATEMENT

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Joyce Ng Ting Ming		✓	✓	✓		✓		✓	✓					
Ab Al-Hadi Ab Rahman	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓
Nuzhat Khan	✓	✓		✓	✓	✓	✓	✓	✓					
Muhammed Paend Bakht	✓		✓	✓			✓	✓		✓	✓		✓	
Shahidatul Sadiah	✓		✓	✓	✓		✓		✓			✓		
Mohd Shahrizal Rusli	✓		✓	✓	✓	✓		✓	✓	✓	✓	✓		✓
Muhammad Nadzir Marsono		✓	✓		✓	✓		✓		✓			✓	

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare no known conflict of interest.

DATA AVAILABILITY

The data that support the findings of this study are openly available in ISPD Contests at https://www.ispd.cc/contests/11/ispd2011_contest.html.

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BIOGRAPHIES OF AUTHORS

Joyce Ng Ting Ming received a first-class B.S. degree in electrical and electronic engineering from University Technology Malaysia (UTM). She was recognized for her exceptional presentation skills and received Best Presenter Award at ICECE Conference. Currently, she works at Intel microelectronics Malaysia as ASIC Front-End Validation Engineer, applying expertise in electrical engineering and validation processes to ensure the quality and performance of integrated circuits in cutting edge technologies. She can be contacted at email: n.ting@graduate.utm.my.

Ab Al-Hadi Ab Rahman obtained his Ph.D. degree from the École Polytechnique Fédérale de Lausanne, Switzerland, M.Eng. degree from the Universiti Teknologi Malaysia (UTM), and B.S. degree from the University of Wisconsin-Madison, USA. He has been actively involved in hardware and SoC design for ASIC and FPGA systems implementation for more than 18 years and has authored and co-authored more than 70 journal and conference papers, with contributions to developing new design methodologies, automated tools, and techniques for high-performance and low-power systems. From 2018 to 2020, he was a research engineer at Mediatek Singapore, working on machine learning methodologies in physical design. He is currently an associate professor at UTM. He can be contacted at email: hadi@utm.my.

Nuzhat Khan received her Ph.D. degree in environmental technology from the School of Industrial Technology, University of Science Malaysia (USM) and M.S. degree in information technology from the Balochistan University of Information Technology, Engineering and Management Science (BUITEMS), Quetta, Pakistan, in 2019. She received the Higher Education Commission (HEC) Scholarship for her master's study. Her research interests include image processing, natural language processing, statistical linguistics, optical character recognition, machine vision, artificial intelligence, precision agriculture, machine learning, and deep learning. Currently, she is working as a postdoctoral research fellow as part of the research group at VeCAD (VLSI and Embedded Computing Architecture Design) laboratory at the University of Technology Malaysia (UTM). She is a technical committee member for the ICEST 2025 conference. She serves as a reviewer for several reputed journals, including pattern recognition, genetic resources, and crop evolution, artificial intelligence review, scientific reports, theoretical and applied climatology, journal of oil palm research, discover applied sciences, cluster computing, and the journal of big data, among others. She can be contacted at email: khan.nuzhat@utm.my.

Muhammed Paend Bakht received his Ph.D. degree in electrical engineering from the University of Technology Malaysia (UTM). He worked as a postdoctoral researcher at Universiti Tun Hussein Onn Malaysia. Before his doctoral journey, he was an assistant professor at the Faculty of Information and Communication Technology, Balochistan University of Information Technology, Engineering and Management Sciences (BUITEMS), Quetta, Pakistan. His research interests include optimizing and managing renewable energy systems, smart grid technologies, and machine learning applications in energy and agriculture. Currently, he is working as a Postdoctoral Researcher at Teagasc, Ireland. His current research involves the adoption of renewable energy in the agriculture sector. He can be contacted at email: paend.bakht@graduate.utm.my.

Shahidatul Sadiah (Member, IEEE) received a B.Eng. degree in communication network engineering and an M.Eng. degree in electronic and information system engineering from Okayama University, Japan, in 2013 and 2015, respectively, and a Ph.D. degree in information engineering from Hiroshima University, Japan, in 2018. She has been a senior lecturer with the Department of Electronics and Computer Engineering, Universiti Teknologi Malaysia, since January 2019. Her research interests include cryptography, information security, digital system design, and computer architecture. She can be contacted at email: shahidatulsadiah@utm.my.

Mohd Shahrizal Rusli received his Ph.D., M.Eng., and B.Eng. in electrical engineering from Universiti Teknologi Malaysia (UTM), Malaysia. During his doctoral study, he attended the University of California Irvine, USA, and the University of Catania, Italy, as a research scholar. His research interests are in the field of network-on-chip, computer architecture, machine learning accelerators and power management. He has published in numerous journals, proceedings and book chapters. From 2021 to 2022, he was a SoC design engineer at Mediatek Singapore, working on interconnect design and timing closure. He currently serves as senior lecturer of electronic and computer engineering, UTM and also a researcher for VLSI and Embedded Computing Architecture Design (VeCAD) Research Group. He can be contacted at email: shahrizalr@utm.my.

Muhammad Nadzir Marsono is an electronics and computer engineering Professor at Universiti Teknologi Malaysia. He serves as Deputy Dean (Academic and Student Affairs) at the Faculty of Electrical Engineering. He is also a member of the VeCAD research group. His research focuses on domain-specific computing architecture, VLSI/SoC design, and embedded systems. His interests span digital system design, computer architecture, reconfigurable computing, multicore/manycore SoCs, NoCs, network algorithmics, network processing, and software-defined networks. He holds a Ph.D. from the University of Victoria, Canada, and an MEng degree from UTM. He can be contacted at email: mnadzir@utm.my.