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Three Phase Trinary Source MLI Using Multicarrier SPWM Strategies

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Abstract

This paper presents a comprehensive analysis of various bipolar Multicarrier Pulse Width Modulation (MCPWM) strategies with Sinusoidal reference for three phase Nine level Trinary Source cascaded inverter. A new approach of nine levels is for medium voltage applications. The proposed topology uses reduced number of switching devices and thus reducing losses and low THD in comparison with the conventional topology. The configuration of the circuit is simple and easy to control. Performance factors such as %THD, V_{RMS} where measured and Crest Factor (CF), Distortion Factor (DF), Form Factor (FF) of output voltage were calculated for different modulation indices and the results were compared. VFPWM strategies provides minimum THD and COPWM strategy provides higher fundamental V_{RMS} output voltage.

Keywords: *cascaded multilevel inverter (CMLI), total harmonic distortion (THD), multicarrier pulse width modulation (MCPWM),* b*ipolar, minimum switches*

1. Introduction

Multilevel inverter is used to synthesize a nearby sinusoidal voltage from various levels of DC voltages and the proposed cascaded H-bridge inverter is used to reduce the number of bridges and the switches.The proposed three phase nine level trinary source inverter require a less number of components to obtain same number of voltage levels when compared to diode clamped and flying capacitor type topologies.The structure requires lesser active switches as compared with conventional cascaded H-bridge topology with much reduced switching losses. Due to this, the switching loss gets reduced. Also, it generally regularises the stair-case voltage waveform from several DC sources which has reduced harmonic content. Arun et al [1] introduced unipolar PWM control technique having inverted sine carrier for Trinary DC source multilevel inverter. Performance evaluation of various unipolar SPWM strategies of Trinary DC Source multilevel inverter was discussed in [2]. Bharath et al [3] proposed a 9-Level Trinary DC source inverter using Embedded Controller. Chechnya et al [4] aims to extend the knowledge about the performance of different clamped multilevel inverter through harmonic analysis. Gnana Prakash et al [5] proposed a method which is well suited for a high power applications and it built with three DC sources and six Switches. Gupta et al [6] and [7] developed the topology for multilevel inverters to attain maximum number of levels from given DC sources and a comprehensive review of a recently proposed multilevel inverter. JansiRani et al [8] presented the implementation of 81 level inverter using Trinary logic. Mohammed Yaichi et al [9] implemented a mechanism of SVM control strategies applied to five level cascaded multi-level inverter.

Sudhakar et al [10] focussed on the design of nine level inverter topology for three phase induction motor drives. Yu Liu et al [11] and [18] suggested that trinary hybrid 81-level multilevel inverter for motor drive with zero common-mode voltage. Bahravar et al [12] designed a new cascaded multilevel inverter topology with reduced variety of magnitudes of DC voltage

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sources. Chattopadhyay et al [13] distinguished cascaded H-bridge and neutral point clamped hybrid asymmetric multilevel inverter topology for grid interactive transformerless photovoltaic power plant. Cheol-soon Kwon et al [14] presented cascaded H-bridge multilevel inverter using Trinary DC sources. Miranda et al [15] evaluated the modulation techniques to multilevel trinary inverter applied to current active filters. Rahila et al [16] developed a new 81 level inverter with reduced number of switches. Won-kyun Choi et al [17] analysed the performance of cascaded H-bridge multilevel inverter employing bidirectional switches.

This paper aims at comprehensively analysing the proposed three phase nine level Trinary source H-bridge cascaded inverter using various bipolar SPWM strategies. In this paper, the aforesaid topology was developed using MATLAB-SIMULINK.

2. Three Phase Nine Level Trinary Source Cascaded Multilevel Inverter

The fundamental H-Bridge cascaded topology increases the number of components required, which in turn makes the design complexity and increases the cost [1, 2]. It is also to be establishing that the maximum output voltage cannot go beyond the sum of voltage of individual sources which becomes the most important setback of this topology. Because of the foresaid reason in an application which requires high output voltage from low voltage level, it needs H-bridge module in addition or step-up transformers.To accomplish this problem a new topology proposed is shown in Figure 1 to reduce component count.

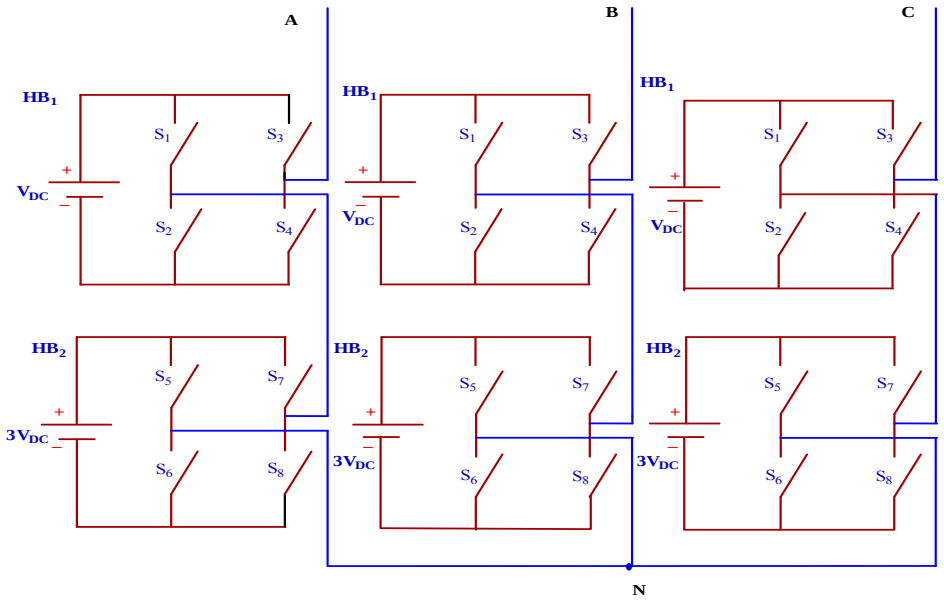

Figure 1. Three phase nine levels Trinary source Cascaded multilevel inverter

Figure 1 shows the topology of the proposed three phase nine level Trinary source cascaded multilevel inverter. It views like a conventional cascaded H-bridge multilevel inverter apart from input DC sources. The topology comprises of floating input DC sources connected through power switches. The structure requires lesser active switches as compared with conventional cascaded H-bridge topology with much reduced switching losses. By using V_{DC} and $3V_{DC}$, it can synthesize nine output levels; $-4V_{DC}$, $-3V_{DC}$, $-2V_{DC}$, $-V_{DC}$, 0, V_{DC}, $2V_{DC}$, $3V_{DC}$ and $4V_{DC}$. The lower inverter generates an elementary output voltage with three levels and then the upper inverter adds or subtracts one level from the fundamental wave to synthesize stepped waves. At this point, the final output voltage level becomes the sum of each terminal voltage of H-bridge [7] and it is given as:

$$V_{out} = V_{HB1} + V_{HB2} \quad (1)$$

In the proposed circuit design, suppose the *n* number of H-bridge component has self-governing DC sources in sequence of the power of 3, a predictable output voltage level is given as:

$$V_n = 3^n,\ n = 1,2,3,..... \quad (2)$$

Where; n is number of H bridges

Waveforms of output voltage are denoted as (V_{out}), upper terminal voltage is (V_{HB1}) and the lower voltage is (V_{HB2}) inverter in sequence. The output voltage has nine levels include zero level. Though it is close to a sinusoidal wave, it has lower order harmonics. So it needs more H-bridge modules or output filter to obtain high quality output voltages. Advantage of the proposed multilevel inverter scheme is the elimination of transformer in the main power stage. However, each cell of the proposed multilevel inverter requires its own isolated power supply. The provision of these isolated supplies is the main limitation in the power electronic circuit design. So the proposed multilevel inverter is suitable for photovoltaic power generating systems equipped with distributed power sources [7].

3. Multicarrier Sine Pulse Width Modulation Strategies

To synthesize multilevel output AC voltage using different levels of DC inputs, semiconductor devices must be switched ON and OFF in such a way that desired fundamental is obtained with minimum harmonic distortion. There are different types of approaches for the selection of switching strategies for the Trinary source inverters. Among all the PWM methods for Trinary source cascaded inverter, carrier based PWM methods and space vector methods are often used but when the number of output levels is more than five, the space vector method will be very complicated with the increase of switching states. So the carrier based PWM strategy is preferred under this condition in Trinary source inverters. This paper focuses on carrier based PWM strategies which have been extended for use in Trinary source inverter by using multiple carriers. Multicarrier based PWM strategies have more than one carrier that can be triangular waves or sawtooth waves and so on. The carrier waves can be either bipolar or unipolar. In this paper, a comprehensive analysis of the aforementioned topology is carried out using bipolar multi-carrier PWM strategies. In this paper, various multicarrier PWM strategies like Phase Disposition (PD), Phase Opposition Disposition (POD), Alternative Phase Opposition Disposition (APOD), Variable Frequency (VF) and Carrier Overlapping (COPWM) were proposed for three phase nine level Trinary source cascaded inverter.

For an m-level inverter using bipolar multicarrier strategy, $(m\text{-}1)$ carriers with same frequency f_c and same peak-to-peak amplitude A_C are used. The reference waveform has amplitude A_m and frequency f_m are placed at zero reference. The reference wave is continuously compared with each of the carrier signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched ON. Otherwise, the device switched OFF. In this paper, the frequency ratio $m_f = 40$ and modulation index m_a is varied from 0.8 to 1.

$$m_f = f_c / f_m \quad (3)$$

except for VFPWM

$$m_a = 2A_m / (m\text{-}1)A_C \quad (4)$$

except for COPWM

3.1. Phase Disposition (PD) PWM Strategy

The Principle of PDPWM strategy is to use the several carriers with single modulating waveform. In Phase Disposition all the carriers are in phase and the carriers are disposed so that the bands they occupy are contiguous. The modulation wave is centered in the middle of

the carrier set. Figure 2 shows the multicarrier arrangement for PDPWM strategy for $m_a = 0.9$ and $m_f = 21$.

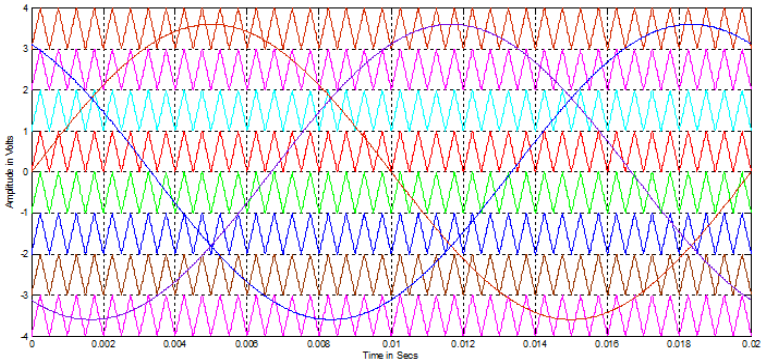

Figure 2. Carrier arrangement for PDPWM Strategy

3.2. Phase Opposition Disposition (POD) PWM Strategy

With the PODPWM method the carrier waveforms above the zero reference value are in phase. The carrier waveforms below zero are also in phase but are 180° phase shifted from those above zero. Figure 3 shows the multicarrier arrangement for PODPWM method for $m_a = 0.9$ and $m_f = 40$.

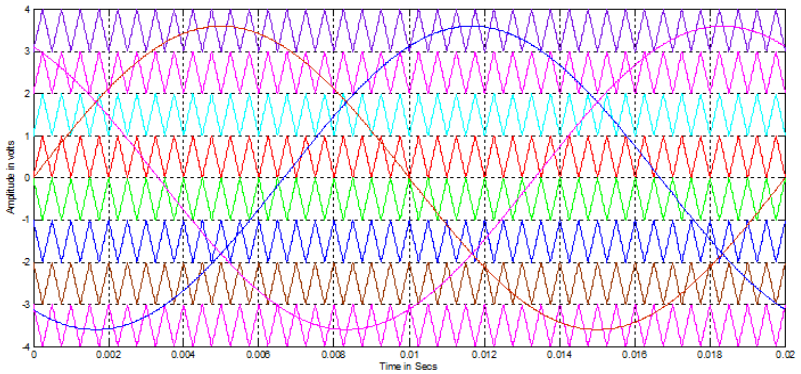

Figure 3. Carrier arrangement for PODPWM Strategy

3.3. Alternative Phase Opposition Disposition (APOD) PWM Strategy

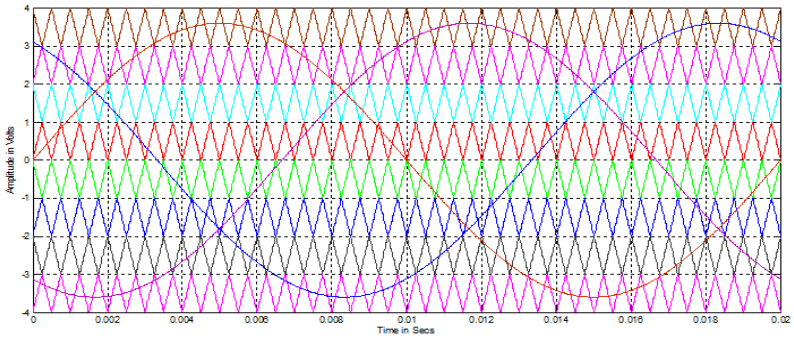

Figure 4. Carrier arrangement for APODPWM Strategy

This method requires each of the eight carrier waves for a nine level inverter to be phase displaced from each other by 180° alternately. Fig.4 shows the multicarrier arrangement for APODPWM method for $m_a=0.9$ and $m_f=40$.

3.4. Variable Frequency (VF) PWM Strategy

The number of switchings for upper and lower devices of chosen nine level three phaseTrinary cascaded DC source inverter is much more than that of intermediate switches in constant frequency carriers. In order to equalize the number of switchings for all the switches, variable frequency PWM strategy is used as illustrated in Figure 5, in which the carrier frequency of the intermediate switches is properly increased to balance the number of switchings for all the switches.

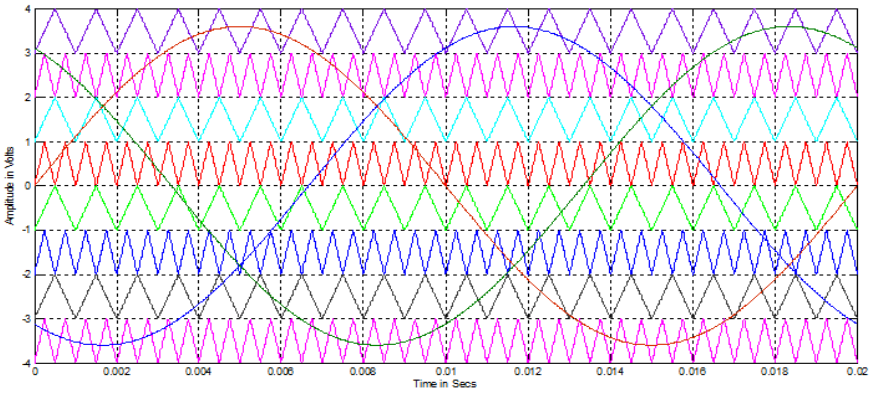

Figure 5. Carrier arrangement for VFPWM Strategy

3.5. Carrier Overlapping (CO) PWM Strategy

In the Carrier Overlapping strategy, m -1 carriers are disposed such that the bands they occupy overlap each other, the overlapping vertical distance between each carrier is $A_c/2$ $(A_c=1)$. The reference waveform is centred in the middle of the carrier signals. The amplitude modulation index m_a is defined as follows:

$$m_a=A_m/(2.5\times A_c) \quad (5)$$

The vertical offset of carriers for nine-level inverter with COPWM strategy is shown in Figure 6.

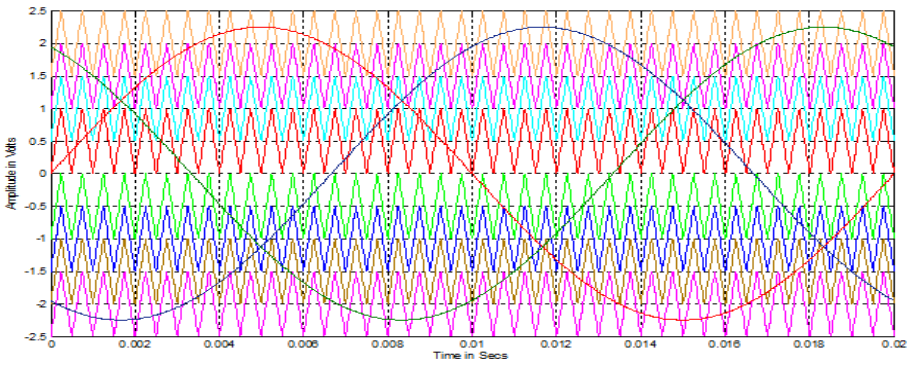

Figure 6. Carrier arrangement for COPWM Strategy

4. Simulation Results

The nine level three phase Trinary cascaded DC source multilevel inverter is modeled in SIMULINK using Power System block set. Switching signals for Trinary cascaded source multilevel inverter are developed using multicarrier sinusoidal PWM strategies. Simulations are performed for different values of m_a ranging from 0.8 –1.

Figure 7-17 show the simulated output voltage of three phase Trinary source cascaded inverter with their corresponding FFT plots shown for only one sample value of $m_a = 0.9$ for above said PWM strategies. Figure 17 shows a graphical comparison of %THD for various strategies for different modulation indices.

The corresponding %THD is measured using the FFT block and their values are listed in Table 1. Table 2 shows the Distortion Factor (a measure of closeness in shape between a waveform and its fundamental component) of the output voltage of chosen MLI. Table 3 displays the V_{RMS} of fundamental inverter output (a measure of DC bus utilization). Table 4 display the corresponding Crest Factor (used to specify peak current rating of the devices). Table 5 display the consequent Form Factor (FF).The following parameter values are used for simulation: V_{DC1}=100V , V_{DC2}= 300V , load (R=100Ω) , f_c = 2000Hz and f_m = 50Hz .

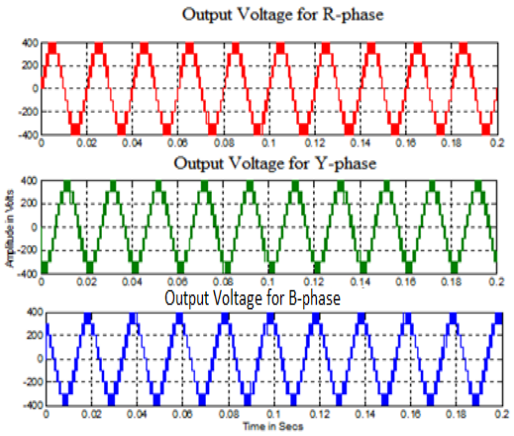

Figure 7. Output Voltage generated by PDPWM Strategy

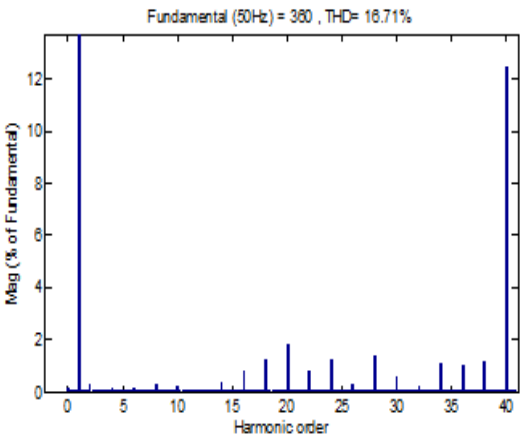

Figure 8. FFT Plot for Output Voltage of PDPWM Strategy

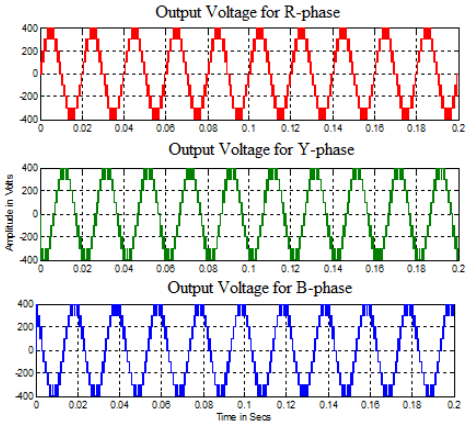

Figure 9. Output Voltage generated by PODPWM Strategy

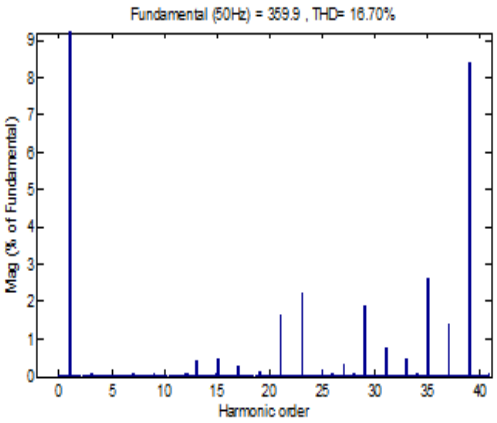

Figure 10. FFT Plot for Output Voltage of PODPWM Strategy

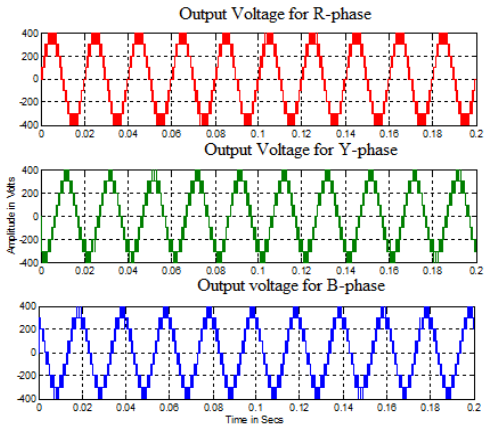

Figure 11. Output Voltage generated by APODPWM Strategy

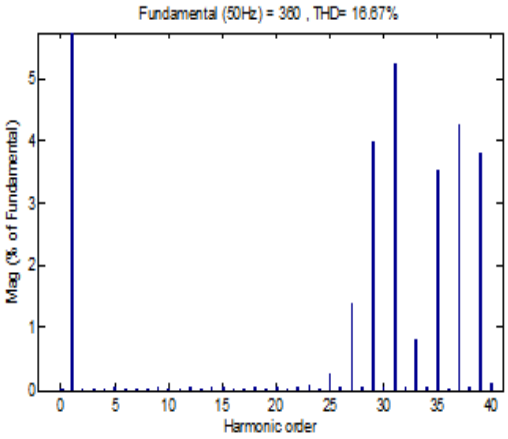

Figure 12. FFT Plot for Output Voltage of APODPWM Strategy

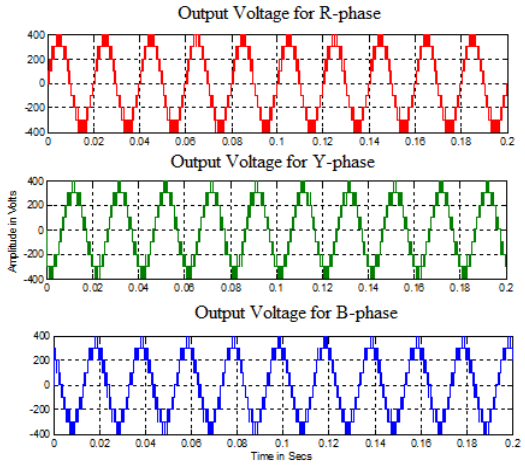

Figure 13. Output Voltage generated by VFPWM Strategy

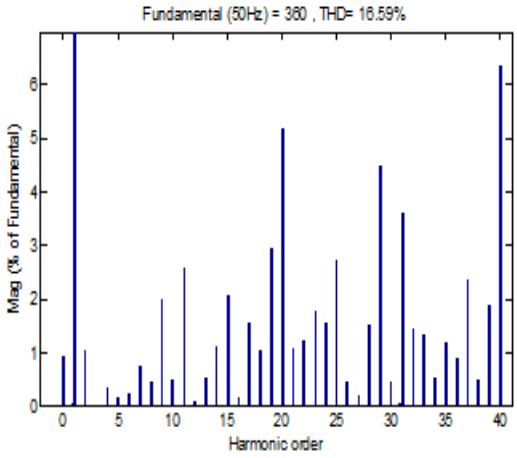

Figure 14. FFT Plot for Output Voltage of VFPWM Strategy

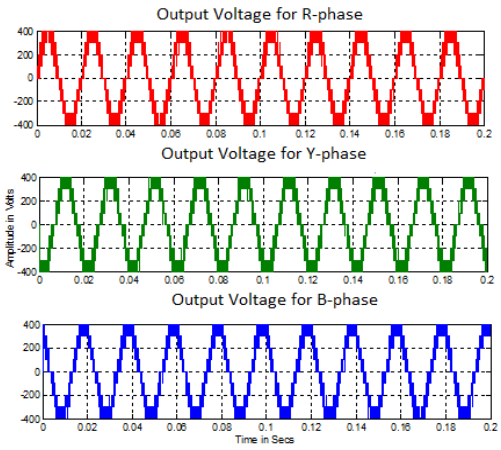

Figure 15. Output Voltage generated by COPWM Strategy

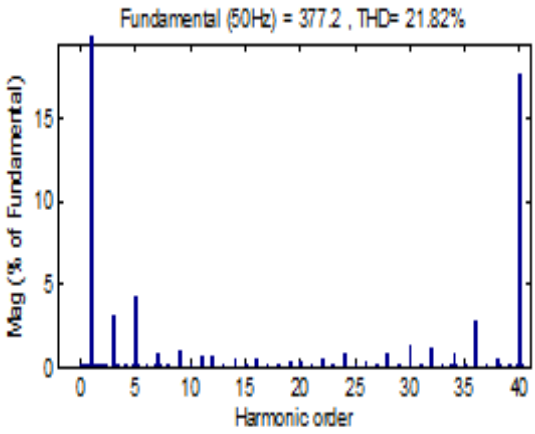

Figure 16. FFT Plot for Output Voltage of COPWM Strategy

Table 1. %THD for Different Modulation Indices

m_a	PDPWM	PODPWM	APODPWM	VFPWM	COPWM
1	13.65	13.47	13.20	13.76	18.27
0.95	15.53	15.56	15.56	15.52	20.08
0.9	16.71	16.70	16.67	16.59	21.82
0.85	17.00	16.94	16.82	17.00	23.56
0.8	17.13	16.80	17.25	16.62	25.97

Table 2. %Distortion Factor for Different Modulation Indices

m_a	PDPWM	PODPWM	APODPWM	VFPWM	COPWM
1	0.02250	0.0425	5.7459	0.0587	0.1871
0.95	0.0302	0.0437	5.7609	0.0987	0.2574
0.9	0.0643	0.014	6.4549	0.2572	0.3778
0.85	0.1133	0.0571	0.0162	0.4405	0.5265
0.8	0.1219	0.0359	6.4145	0.436	0.6437

Table 3. V_{RMS} (Fundamental) for Different Modulation Indices

m_a	PDPWM	PODPWM	APODPWM	VFPWM	COPWM
1	282.8	283.4	282.8	282.9	290.4
0.95	268.7	269.1	268.7	268.7	278.8
0.9	254.5	254.5	254.6	254.5	266.7
0.85	240.4	239.6	240.4	240.4	253.3
0.8	226.2	226.2	226.2	226.3	238.3

Table 4. Crest Factor for Different Modulation Indices

m_a	PDPWM	PODPWM	APODPWM	VFPWM	COPWM
1	1.414	1.414	1.414	1.413	1.414
0.95	1.414	1.413	1.414	1.414	1.414
0.9	1.414	1.414	1.413	1.414	1.414
0.85	1.414	1.414	1.413	1.414	1.414
0.8	1.414	1.413	1.414	1.414	1.414

Table 5. Form Factor for Different Modulation Indices

m_a	PDPWM	PODPWM	APODPWM	VFPWM	COPWM
1	2.02E+3	INF	INF	2.3575E+3	3.63E+3
0.95	3.3587E+3	0.0134E+ 6	INF	0.4554E+3	0.0278E+6
0.9	2.1208E+3	0.0127E+6	INF	0.2796E+3	3.3337E+3
0.85	0.5463E+3	0.0239E+ 6	INF	0.2246E+3	1.6886E+3
0.8	0.9425E+3	0.0226E+6	INF	0.1985E+3	5.9575E+3

It is observed from Table 1 that the harmonic content is found to be minimum in VFPWM strategy and maximum in COPWM strategy for chosen modulation indices. Table 2 shows that the variation in harmonic content of the output voltage after second order attenuation indicated by % DF is relatively less in PODPWM strategy. From Table 3, it is found that the COPWM strategy provide relatively higher DC bus utilization. It is inferred from Table 4 that CF is almost same for all the strategies of the simulated output voltage. Table 5 indicates that APODPWM has higher Form Factor.

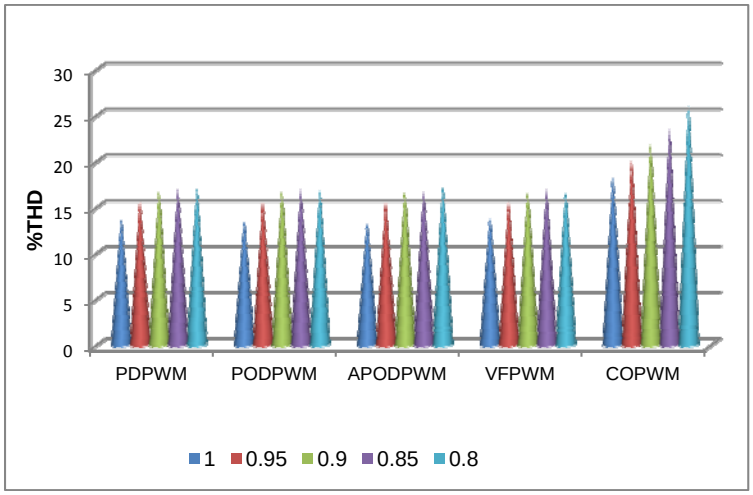

Figure 17. %THD V_S m_a

5. Conclusion

In this paper, various multicarrier PWM strategies for chosen nine level three phase Trinary source cascaded inverter have been developed and simulation results are presented for different modulation indices ranging from 0.8-1. Various performance factors like %THD, DF, V_{RMS} of fundamental, CF and FF have been evaluated, presented and analysed. It is observed that VFPWM strategy provides relatively minimum THD. PODPWM provides relatively lower DF. The maximum DC bus utilization is achieved in COPWM strategy (Table 3). CF is almost same for all the strategies (Table 4). Higher FF is obtained in APODPWM Strategy (Table 5). Appropriate PWM strategies may be employed depending on the performance measure required in a particular application.

References

[1] Arun V, Shanthi B, Natarajan SP. Unipolar PWM Control Technique having Inverted Sine Carrier for Trinary DC source Multilevel Inverter. *International Journal of Advanced Scientific and Technical Research.* 2013; 2(3): 448-460.
[2] Arun V, Shanthi B, Bharathi A. Performance Evaluation of Various Unipolar SPWM Strategies of Trinary DC Source Multilevel Inverter. *International Journal of Engineering and Innovative Technology (IJEIT).* 2012; 2(6): 458-462.
[3] Bharath R, Arun V. 9-Level Trinary DC Source Inverter Using Embedded Controller. *IOSR Journal Engineering.* 2012; 2(10): 90-95.
[4] Chechnya Gupta, Devbrat Kuanr, Abhishek Varshney, Tahir Khurshaid, Kapil Dev Singh. Harmonic Analysis of Seven and Nine Level Cascaded Multilevel Inverter using Multi-Carrier PWM Technique. *International Journal of Power Electronics and Drive System (IJPEDS).* 2014; 5(1): 76-82.
[5] Gnana Prakash M, Balamurugan M, Umashankar S. A New Multilevel Inverter with Reduced Number of Switches. *International Journal of Power Electronics and Drive System (IJPEDS)*. 2014; 5(1): 63-70.
[6] Gupta KK, Jain S. Topology for multilevel inverters to attain maximum number of levels from given DC sources. *IET Power Electron.* 2012; 5(4): 435–446.
[7] Gupta KK, Shailendra Jain. Comprehensive review of a recently proposed multilevel inverter. *IET Power Electronics*. 2014; 7(3): 467–479.
[8] JansiRani V, Rahila J, Santhi M. Implementation of 81 Level Inverter Using Trinary Logic. *International Journal of Innovative Research in Science, Engineering and Technology*. 2014; 3(3): 214-220.
[9] Mohammed Yaichi, Mohammed-Karim Fellah. Implementation Mechanisms of SVM Control Strategies Applied to Five Levels Cascaded Multi-Level Inverters. *International Journal of Power Electronics and Drive System (IJPEDS).* 2014; 4(2): 146-155.
[10] Sudhakar G, Prabhakaran S. Design of Nine Level Inverter Topology for Three Phase Induction Motor Drives. *Bonfring International Journal of Power Systems and Integrated Circuits.* 2014; 4(1): 14-17.
[11] Yu Liu, Fang Lin Luo. Trinary Hybrid 81-Level Multilevel Inverter for Motor Drive with Zero Common-Mode Voltage. *IEEE Transactions on Industrial Electronics*. 2008; 55(3): 1014-1021.

[12] Bahravar S, Babaei E, *New cascaded multilevel inverter topology with reduced variety of magnitudes of dc voltage sources* . 5th India IEEE International Conference on Power Electronics. 2012; 1-6.
[13] Chattopadhyay SK, Chakraborty C, Pal BC. *Cascaded H-Bridge & neutral point clamped hybrid asymmetric multilevel inverter topology for grid interactive transformerless photovoltaic power*. 38th Annual conference on IEEE Industrial Electronics Society. 2012: 5074-5079.
[14] Cheol-soon Kwon, Won-kyun Choi, Un-Taek Hong, Seok-Hwan Hyun, Feel-soon Kang.*Cascaded H-bridge multilevel inverter using trinary dc sources*. IEEE International Conference on Electrical Machines and Systems (ICEMS). 2010; 52-55.
[15] Miranda H, Cardenas V, Perez J. *A comparative development for the modulation techniques to multilevel trinary inverter applied to current active filter*s. 9th IEEE International Power Electronics Congress. 2004: 171 – 176.
[16] Rahila J, Santhi M, Kannabhiran A. *A new 81 level inverter with reduced number of switches*. IEEE International Conference on Advances in Engineering, Science and Management. 2012:485 – 489.
[17] Won-kyun Choi, Cheol-soon Kwon, Un-Taek Hong, Feel-soon Kang. *Cascaded H- bridge multilevel inverter employing bidirectional switches*. IEEE International Conference on Electrical Machines and Systems (ICEMS). 2010: 102 –106.
[18] Yu Lin, Fang Lin Luo .*Trinary hybrid 81 –level multilevel inverter for motor drive with zero common–mode voltage.* Proc IEEE Conference. 2007: 1-7.