

Development of an analysis capacity model for high electron mobility transistor AlGaN/GaN

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ABSTRACT

In this paper, we demonstrate the analytical model developed to characterize the gate-to-drain capacitance C_{gd} and the gate-to-source capacitance C_{gs} , and the impact of the gate length on those capacitances, for the high electronic mobility transistor based on GaN. This model is developed from our previous work on the current voltage characteristic (I , V), and small signal parameters for AlGaN/GaN HEMT. The research study examined the impact of parasitic resistances (drain, source), low field mobility, the aluminum amount in the AlGaN barrier, and high-speed saturation. The developed model has matched the experimental data well, confirming the validity, accuracy, and robustness of the model we have developed.

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1. INTRODUCTION

High electronic mobility transistors (HEMT) based on GaN have known a good interest for high-power, high-frequency, and high-temperature applications [1], [2], and pose specific challenges such as the management of non-linear capacitive effects, the control of trapped charges, and thermal dissipation, which are crucial to guaranteeing reliability and high-frequency performance [3].

They have gotten a lot of attention lately, for their high-performance power electronics take advantage of electron transfer properties and the high critical field of the wide band gap material [4], [5]. Also, the AlGaN/GaN transistors can maintain significantly higher current densities compared to other III-V HEMTs [6]. GaN has attractive electronic and thermal properties, such as high breakdown voltages, high carrier saturation, and good thermal conductivity [7]-[9].

To explain the frequency behavior of the AlGaN/GaN device, a precise analysis of the capacitances related to the device should be conducted. For that, we developed our previous model analysis of the small signal parameter and current voltage [10] to obtain the characteristics of the capacitances: gate to source capacitance and gate to drain capacitance.

The principal objective of this work is to have developed an analytical capacitance model for the AlGaN/GaN transistor, firstly we calculate the total charge Q , after we calculate the transconductance and the conductance, finally we deduce the evolution of the gate to source capacitance versus the gate voltage and the variation of the gate to drain capacitance as a function of the drain voltage for several different values of the

gate voltage and we compare them with the experimental results to validate the development proposed model, finally we study the impact of the gate length L on the capacitances analysis.

2. METHOD

2.1. Total channel charge

The channel charge Q is given by [11]:

$$Q = qn_s(T, m) \quad (1)$$

where, $n_s(T, m)$ is present the sheet carrier concentration of the two-dimensional electron gas (2-DEG) formed at the AlGaN/GaN heterojunction, it's can be written by [12]:

$$n_s(T, m) = \frac{\varepsilon(m)}{qd} (V_{gs} - V_{th}(T, m) - E_F(T, m)) \quad (2)$$

where m , q , T are the aluminum mole fraction in AlGaN/GaN, the electron charge and the temperature respectively. $\varepsilon(m)$ illustrates the dielectric constant of AlGaN, d is the addition of the undoped AlGaN spacer layer thickness d_i , and the doped AlGaN layer thickness d_d , as mentioned in Figure 1 that presents the fundamental structure of transistors HEMTs AlGaN-GaN, $E_F(T, m)$ is the position of the Fermi level which is denoted as a function of $n_s(T, m)$ and its expression given by [13].

$$E_F(T, m) = K_1(T) + K_2(T)\sqrt{n_s(T, m)} + K_3(T)n_s(T, m) \quad (3)$$

with K_1, K_2 and K_3 are three parameters which depend on the temperature.

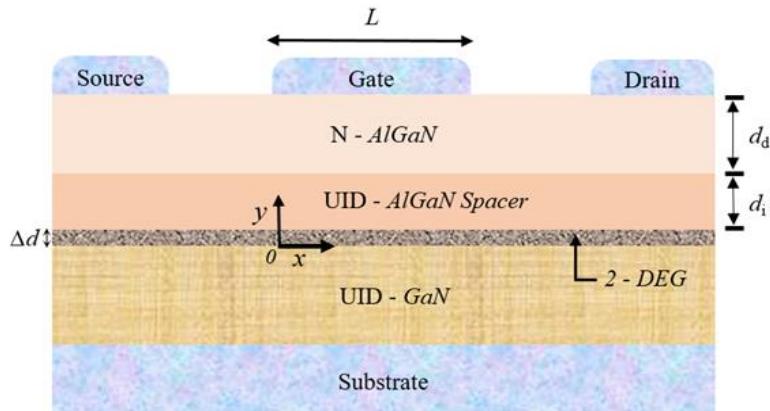


Figure 1. Diagram in cross-section of AlGaN/GaN HEMT transistor

The threshold voltage $V_{th}(T, m)$ can be expressed by [14]:

$$V_{th}(T, m) = \phi(m) - \Delta E_C(T, m) - \frac{qN_d d_d^2}{2\varepsilon(m)} - \frac{\sigma_{PZ}(m)}{\varepsilon(m)} d \quad (4)$$

where $N_d, \Delta E_C(m), \phi(m)$ are the doping density of the AlGaN layer conduction band discontinuity between GaN and AlGaN, and the Schottky barrier height, respectively, $\sigma_{PZ}(m)$ is the charge density induced by the total polarization, can be given by [15]:

$$\sigma_{PZ}(m) = |P_{PP}(m) + P_{Al_mGa_{1-m}N}^{sp}(m) - P_{Al_mGa_{1-m}N}^{sp}(0)| \quad (5)$$

where, $P_{PP}(m)$ is the piezo-electric polarization with its expression varies as a function of the value of m , and $P_{Al_mGa_{1-m}N}^{sp}(m)$ and $P_{Al_mGa_{1-m}N}^{sp}(0)$ are the spontaneous polarizations of Al_mGa_{1-m}N and GaN respectively [15].

$$P_{PP}(m) = \begin{cases} P_{AlmGa_{1-m}N}^{pz}(m) & \text{For } 0 \leq m < 0.38 \\ P_{AlmGa_{1-m}N}^{pz}(2.33 - 3.5m) & \text{For } 0.38 \leq m \leq 0.67 \\ 0 & \text{For } 0.67 < m \leq 1 \end{cases} \quad (6)$$

Total channel charge Q is also obtained by integrating the charge density along the channel [16]:

$$Q = \int_0^L \frac{I_{ds}}{v_d(x)} dx \quad (7)$$

where L , I_{ds} are present the gate length and the drain current, $v_d(x)$. The electron drift velocity, and is a function of the field $E(x)$ as follow [17],

$$v_d(x) = \frac{\mu_0 E(x)}{1 + \frac{E(x)}{E_C}} \quad (8)$$

with, E_C is the saturation electric field and the field $E(x)$ can be written as [18].

$$E(x) = \frac{dV_C(x)}{dx} \quad (9)$$

With $V_C(x)$ is the channel potential at position x , for obtaining the charge total Q as function of drain current, we substitute the (9) into (8), and by replacing the (8) in (7) we obtain.

$$Q = \int_0^L \frac{I_{ds}}{\mu_0} \left(\frac{dx}{dV_C(x)} \right) dx + \int_0^L \frac{I_{ds}}{\mu_0 E_C} dx \quad (10)$$

According to [19], we can substitute the inverse of the derivative of potential at position x by the follow expression.

$$\frac{dx}{dV_C(x)} = \frac{\mu_0 Z q n_s}{I_{ds}} \quad (11)$$

We replacing the (11) into (10) we get.

$$Q = \int_0^L Z \cdot q \cdot n_s \cdot dx + \int_0^L \frac{I_{ds}}{\mu_0 E_C} dx \quad (12)$$

$$Q = \int_0^L Z \cdot q \cdot \left(\frac{-K_2(T) + \sqrt{K_2^2(T) + 4K_4(T)(V_{gs} - V_{th}(m) - K_1(T))}}{2K_4(T)} \right)^2 \cdot dx + \int_0^L \frac{I_{ds}}{\mu_0 E_C} dx \quad (13)$$

By resolving the integral (13) along the channel L , we conclude the total charge Q channel as a function of the drain current can be expressed as follow:

$$Q = L \left(Z q \left(\frac{-K_2(T) + \sqrt{K_2^2(T) + 4K_4(T)(V_{gs} - V_{th}(m) - K_1(T))}}{2K_4(T)} \right)^2 + \frac{I_{ds}}{\mu_0 E_C} \right) \quad (14)$$

2.2. Current-Voltage characteristics (I_{ds} - V_{ds})

The model of the current voltage characteristic that we will develop in this work, in both linear and saturated regions, to get the capacitance analysis in the transistor HEMT, was proposed in our previous work [10].

2.2.1. The linear region ($V_{ds} < V_{dsat}$)

The (15) shows the expression of the drain current as a function of drain voltage in the linear region.

$$I_{ds} = \frac{-\alpha_2 + \sqrt{\alpha_2^2 - 4\alpha_1\alpha_3}}{2\alpha_1} \quad (15)$$

With,

$$\alpha_1 = -\left(\frac{(\mu_0 E_C - v_{sat})}{E_C v_{sat}} (R_s + R_d)\right) \quad (16)$$

$$\alpha_2 = L + Zq\mu_0(R_s + R_d) \left(\frac{-K_2(T) + \sqrt{K_2^2(T) + 4K_4(T)(V_{gs} - V_{th}(m) - K_1(T))}}{2K_4(T)} \right)^2 + \frac{(\mu_0 E_C - v_{sat})}{E_C v_{sat}} V_{ds} \quad (17)$$

$$\alpha_3 = -Zq\mu_0 \left(\frac{-K_2(T) + \sqrt{K_2^2(T) + 4K_4(T)(V_{gs} - V_{th}(m) - K_1(T))}}{2K_4(T)} \right)^2 V_{ds} \quad (18)$$

Where, v_{sat} is the saturation drift velocity, μ_0 is the low-field mobility, and R_s and R_d are the parasitic resistances of the source and drain, respectively.

2.2.2. The saturation region ($V_{ds} \geq V_{dsat}$)

The free charge carriers (electrons and holes) acquire a saturation velocity of displacement v in this region, that we can conclude the drain current become in its maximum value, the expression of the drain current as a function of drain voltage in the saturation regime can be written in the bellow form:

$$I_{dsat} = \frac{-\beta_2 + \sqrt{\beta_2^2 - 4\alpha_1\beta_3}}{2\alpha_1} \quad (19)$$

With:

$$\beta_2 = \delta_2 + \frac{(\mu_0 E_C - v_{sat})}{E_C v_{sat}} V_{dsat} \quad (20) \quad \text{and} \quad \beta_3 = \delta_3 V_{dsat} \quad (21)$$

Where,

$$\delta_2 = L + Zq\mu_0(R_s + R_d) \left(\frac{-K_2(T) + \sqrt{K_2^2(T) + 4K_4(T)(V_{gs} - V_{th}(m) - K_1(T))}}{2K_4(T)} \right)^2 \quad (22)$$

$$\delta_3 = -Zq\mu_0 \left(\frac{-K_2(T) + \sqrt{K_2^2(T) + 4K_4(T)(V_{gs} - V_{th}(m) - K_1(T))}}{2K_4(T)} \right)^2 \quad (23)$$

Where, V_{dsat} presents the saturation voltage.

$$V_{dsat} = \frac{-\delta_1(2\delta_2 + \delta_1)}{\left(2\delta_1 \frac{(\mu_0 E_C - v_{sat})}{E_C v_{sat}} + 4\alpha_1\delta_3\right)} \quad (24)$$

2.3. Small signal parameters

2.3.1. Transconductance g_m

The transconductance g_m is considered as a provider of the intrinsic gain mechanism of the HEMT, as well as is a measurement of the variation in output current I_{ds} for a given change in input voltage V_{gs} . It can be defined mathematically as [20].

$$g_m = \left. \frac{\partial I_{ds}}{\partial V_{gs}} \right|_{V_{ds}=\text{cte}} \quad (25)$$

$$g_m = \frac{1}{2\alpha_1} \left(-\frac{\partial \alpha_2}{\partial V_{gs}} + \frac{2\alpha_2 \frac{\partial \alpha_2}{\partial V_{gs}} - 4\alpha_1 \frac{\partial \alpha_3}{\partial V_{gs}}}{2\sqrt{\alpha_2^2 - 4\alpha_1\alpha_3}} \right) \quad (26)$$

2.3.2. Drain conductance g_d

The variation of the current I_{ds} with the missing of control of the gate on the electrons in the channel at the interface AlGaN/GaN (V_{gs} fixe) and the variation of the drain voltage V_{ds} , this defines the conductance g_d of the transistor HEMT. Mathematically, it is given by [21]:

$$g_d = \frac{\partial I_{ds}}{\partial V_{ds}} \Big|_{V_{gs}=cte} \quad (27)$$

$$g_d = \frac{1}{2\alpha_1} \left(-\frac{\partial \alpha_2}{\partial V_{ds}} + \frac{2\alpha_2 \frac{\partial \alpha_2}{\partial V_{ds}} - 4\alpha_1 \frac{\partial \alpha_3}{\partial V_{ds}}}{2\sqrt{\alpha_2^2 - 4\alpha_1 \alpha_3}} \right) \quad (28)$$

2.4. Capacitance analysis

To study the dynamic behavior of the HEMT transistor, it is necessary to examine the charge and discharge of the internal capacitors of the device.

2.4.1. Gate to source capacitance C_{gs}

The gate to source capacitance C_{gs} determines the commutation speed by controlling the gate charge, thus influencing the dynamic response of the transistor, and it represents the variation of the total charge Q as a function of the gate voltage V_{gs} . It's can obtained as follows [22].

$$C_{gs} = \frac{\partial Q}{\partial V_{gs}} \quad (29)$$

$$C_{gs} = L \left(Zq \left(\frac{-K_2(T) + \sqrt{K_2^2(T) + 4K_4(T)(V_{gs} - V_{th}(m) - K_1(T))}}{K_4(T) \sqrt{K_2^2(T) + 4K_4(T)(V_{gs} - V_{th}(m) - K_1(T))}} \right) + \frac{g_m}{\mu_0 E_C} \right) \quad (30)$$

2.4.2. Gate to drain capacitance C_{gd}

The gate to drain capacitance C_{gd} contributes to the Miller effect, which can slow down switching and impact high-frequency performance and represents too the variation of total charge Q as a function of the drain voltage V_{ds} and it given by [22].

$$C_{gd} = \frac{\partial Q}{\partial V_{ds}} \quad (31)$$

$$C_{gd} = \frac{L}{\mu_0 E_C} g_d \quad (32)$$

3. RESULTS AND DISCUSSION

To highlight the model of the capacitance analysis parameters (C_{gs} and C_{gd}) of the HEMT transistor, we followed a comparative study with experimental results [23]. In the current calculation, the different parameters used to simulate our developed proposed model are listed in Table 1, also the values of the parameters K_1, K_2, K_3 at different gate voltages V_{gs} which are calculated using the identical method [24], employing the effective mass $m^* = 0.22m_0$ [25], also used in the present calculation are presented in Table 2.

Table 1. Various parameters included in the suggested model.

Parameter	Description	Value
V_{th}, V	Threshold voltage	-2.98
d_d, nm	Thickness of the doped layer	25
d_i, nm	Thickness of the undoped layer	5
$Z, \mu\text{m}$	Gate width	250
$L, \mu\text{m}$	Gate length	0.35
$V_{sat}, \text{m/s}$	Saturation velocity	1.19×10^5
R_s, Ω	Parasitic source resistance	0.9
R_d, Ω	Parasitic drain resistance	2

Figure 2, presents the gate to source capacitance C_{gs} versus the gate voltage with a fixed value of drain voltage equals 7V. The capacitance is too small when the gate voltage V_{gs} is inferior of threshold voltage, this due to the small density of the channel 2-DEG, when the gate voltage is little superior of threshold voltage V_{th} , the gate to source capacitance rise very quickly, in the high values of gate voltage the gate to source capacitance become almost constant. The adequacy of the proposed developed model with the experimental data [23] demonstrates the validity of the proposed model.

Figure 3 shows a plot of the gate to drain capacitance C_{gd} against drain voltage V_{ds} for different value of the gate voltage, from this figure the gate to drain capacitance decreases when the drain voltage rises, this decreases of the gate to drain capacitance will degrade of the drain control over the channel charge. The gate voltage too have the influence on the gate to drain capacitance that's when the value of gate voltage decrease the gate to drain capacitance decreases too. In the other words, the experimental data [23] in concordance with the result of our proposed developed model.

Table 2. Values of the parameters K_1 , K_2 and K_3 .

Gate voltage V_{gs} , V	K_1 , V	$K_2 \times 10^{-8}$, V·m	$K_3 \times 10^{-18}$, V·m ²
-1	-0.57282	3.06693	-1.03474
-1,5	-0.57281	2.45502	-7.61086
-2	-0.57280	1.84921	-4.90162

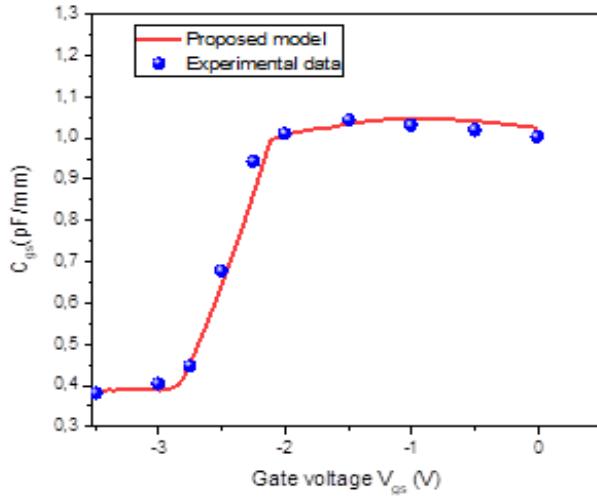


Figure 2. Gate to source capacitance C_{gs} versus the gate voltage V_{gs} by fixing the drain voltage V_{ds} at 5V

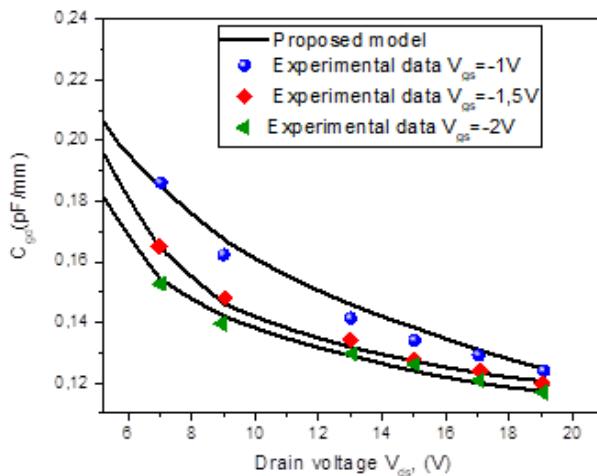


Figure 3. Gate to drain capacitance C_{gd} as function of the drain voltage V_{ds} for different values of the gate voltage V_{gs}

Figure 4 illustrates the variation of the gate to source capacitance versus gate voltage for different values of gate length L with a fixed value of drain voltage fixed at 5V, we notice that when the gate length L increases the gate to source capacitance elevates. Figure 5 displays the variation of the gate to drain capacitance as a function of drain voltage for different value of the gate length L with the gate voltage V_{gs} equals -1V, from this figure, we observe that when the gate length L rises the gate to drain capacitance increases.

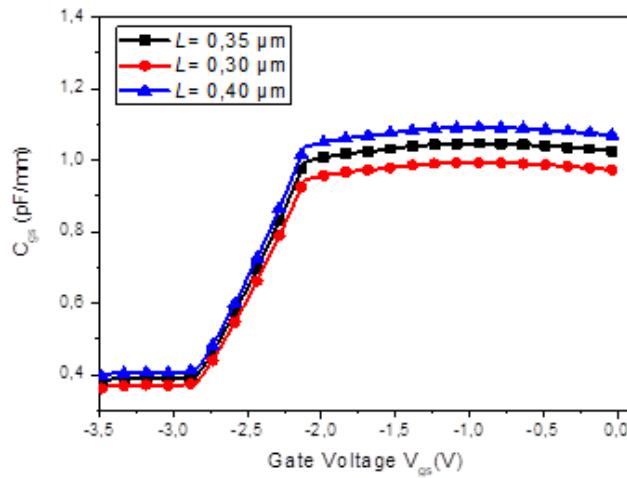


Figure 4. Variation the gate to source capacitance C_{gs} versus gate voltage V_{gs} for different gate length L

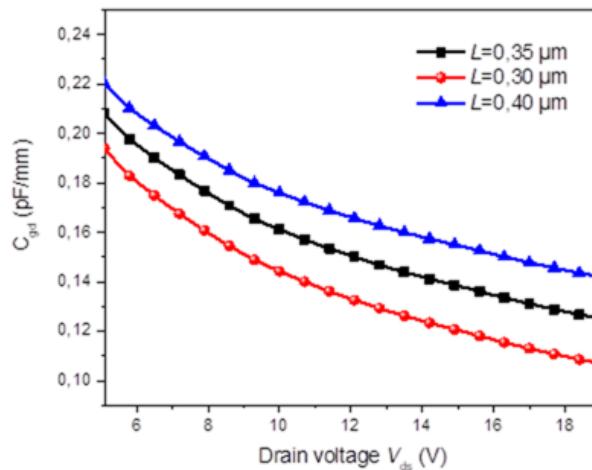


Figure 5. Variation the gate to drain capacitance C_{gd} as function of the drain voltage V_{ds} for different gate length L

4. CONCLUSION

In this work, we presented a newly developed of the capacitance analysis (gate to source capacitance and gate to drain capacitance) for AlGaN/GaN transistors. The approach begins by determining the total channel charge Q from the current-voltage characteristic, followed by deriving the relevant capacitances from this total charge. The model captures key physical effects such as low-field mobility, parasitic resistances, the aluminum composition of the AlGaN barrier, and high-speed saturation. Additionally, it highlights the influence of gate length on both capacitances. Our simulated results show strong agreement with experimental data, confirming the model's relevance for designing and optimizing high-frequency GaN-based devices. This model improves our understanding of dynamic capacitive behavior in HEMTs, which is essential for improving power applications and device performance in RF. Future research can focus on integrating these factors to refine and extend the scope of the suggestion model.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

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Azzeddine Farti	✓	✓	✓	✓	✓	✓		✓	✓	✓			✓	
Abdelkader Touhami		✓				✓		✓	✓	✓	✓	✓	✓	

C : Conceptualization

I : Investigation

Vi : Visualization

M : Methodology

R : Resources

Su : Supervision

So : Software

D : Data Curation

P : Project administration

Va : Validation

O : Writing - Original Draft

Fu : Funding acquisition

Fo : Formal analysis

E : Writing - Review & Editing

CONFLICT OF INTEREST STATEMENT

The authors state no conflict of interest.

DATA AVAILABILITY

Data availability is not applicable to this paper as no new data were created or analyzed in this study.

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