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Performance Evaluation of 3Φ Asymmetrical MLI with Reduced Switch Count

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Abstract

The multi level inverter system is habitually exploited in AC drives, when both reduced harmonic contents and high power are required. In this paper, a new topology for three phase asymmetrical multilevel inverter employing reduced number of switches is introduced. With less number of switches, the cost, space and weight of the circuit are automatically reduced. This paper discusses the new topology, the switching strategies and the operational principles of the chosen inverter. Simulation is carried out using MATLAB-SIMULINK. Various conventional PWM techniques that are appropriate to the chosen circuit such as PDPWM, PODPWM, APODPWM, VFPWM and COPWM are employed in this work. COPWM technique affords the less THD value and also affords a higher fundamental RMS output voltage.

Keywords: *THD, asymmetrical, MLI, CF, Vrms, DF*

1. Introduction

The multilevel inverter [MLI] is used for high voltage and high power applications. This inverter produce staircase (stepped) waveform from several different levels of DC voltage. It have lower voltage rating of devices, low harmonics distortion, high power quality waveforms, lower switching frequency and losses, higher efficiency, reduction of dv/dt stresses. Because of the above characteristics, it have a possibility of working with low speed semiconductors if its comparison with the two-level inverters. Many number of MLI topology are available but most popular MLI topology is Diode Clamped, Flying Capacitor and Cascaded Multilevel Inverter. Radan [1] et al introduced an evaluation of carrier based PWM methods for multi level inverters. Rodriguez [2] proposed multilevel voltage source converter topologies for industrial medium voltage drives. McGrath and Holmes [3] introduced a general analytical method for calculating

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inverter dc link current harmonics. Palanivel and Dash [4] proposed multicarrier pulse width modulation methods based three phase cascaded multilevel inverter including over modulation and low modulation indices. Pan and Peng [5] introduced a sinusoidal PWM method with voltage balancing capability for diode clamped five level converters. Konstantinou and Agelidis [6] deal with a performance evaluation of half bridge cascaded multilevel converters operated with multicarrier sinusoidal PWM techniques. Judi [7] deal with a modified cascaded multilevel inverter with reduced switch count employing bypass diodes. Ahmed [8] made a new multilevel inverter topology with reduced number of switches. Suroso and Noguchi [9] discussed a multilevel voltage-source inverter using h-bridge and two level power modules with a single power source. Bayat and Babaei [10] a new cascaded multilevel inverter with reduced number of switches. Sun [11] multi-level inverter capable of power factor control with dc link switches. Kureve [12] proposes a switching control for a cascaded H-bridge inverter structure with reduced switches which is used to improve the THD performance of a single phase five level CHB MLI. Imran Azim and Mohiuddin [13] portray an approach of an analysis that provides information regarding the presence of harmonics at the inverter output terminal.

2. Multilevel Inverter

The operation of a multilevel inverter is concerned with comparison of carrier and reference wave. The basic operation can be explain as an optional stacking of a number of DC voltage source stages which depends on certain time of operation that one stage is stacked (forward or reverse) or bypassed. MLIs also have some issues such as necessitate a big number of semiconductor switches which increases as the number of steps/levels increases. If the levels of the steps increase the design will be multifarious for synchronous gate drivers for different levels. The order of numbering of the switches is S_1, S_2, S_3, S_4 and S_5. This circuit does not have a capacitor and diode. So price tag of the circuit is low compared to the conventional circuit.

The voltage level of the outputs are $3V_{dc}$, $2V_{dc}$, V_{dc}, $0_{,}$ - $V_{dc,}$ $-2V_{dc,}$ $-3V_{dc.}$ In proposed circuit semiconductor switches are less when compared to the conventional circuit. So the advantages of the proposed circuit are fewer cost and minimum switching losses. Figure 1 shows a Three Phase Seven level Inverter.

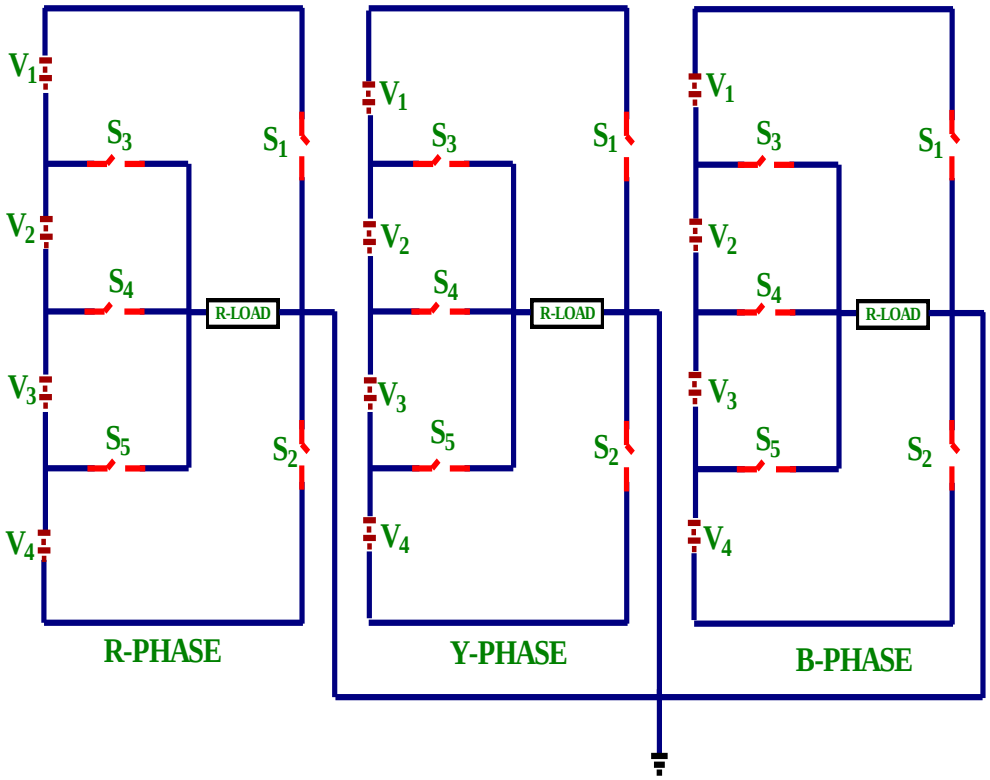

Figure 1. Three Phase Seven Level Inverter

Table 1. Comparison Table Between Conventional and Proposed Circuit

S.NO	Conventional circuit DCMLI (7-level)	Conventional circuit FCMLI (7-level)	Conventional circuit CMLI (7-level)	Proposed circuit(7-level)
Switches	36	36	36	15
Main Diode	36	36	36	0
Clamping Diode	36	0	0	0
DC Bus capacitor	18	18	18	0
Balancing Capacitor	0	45	0	0

3. Modulation Strategies

The most standard PWM methods are available to the inverter. For controlling the output voltage, one of the methods is SPWM method. In this method, a fixed DC input voltage is applied to the inverter and get a controlled AC output voltage by adjusting the ON and OFF

periods of the inverter power semiconductor devices. By this technique increasing the switching frequency of the PWM pattern reduces the lower frequency harmonics by moving the switching frequency carrier harmonics and associated sideband harmonics further away from the fundamental frequency component. The modulating/reference wave of multilevel carrier based PWM strategies is sinusoidal. The sinusoidal reference wave is concerned to multiple Control Freedom Degree including frequency, amplitude, and phase angle of the reference wave. The principle of SPWM strategy is to employ the several carriers with three phase sinusoidal modulating signal. For an m level inverter, m-1 carriers are used. All carriers having same frequency f_c and same peak-to-peak amplitude A_c which are disposed such that the bands they occupy overlap each other. The amplitude of the reference wave is A_m and frequency is $f_{m,}$ which are centered in the middle of the carrier signals. The frequency ratio m_f is defined in the carrier overlapping method as follows:

$$m_f = \frac{f_c}{f_m} \quad (1)$$

This paper focuses on five SPWM strategies. They are: PDPWM, PODPWM, APODPWM, VFPWM and COPWM.

Table 2. Switching Table for Asymmetrical Multi Level Inverter

Switching Level	S_1	S_2	S_3	S_4	S_5
3 V_{dc}	0	1	0	0	1
2 V_{dc}	0	1	0	1	0
V_{dc}	0	1	1	0	0
0	0	0	0	0	0
-V_{dc}	1	0	0	0	1
-2 V_{dc}	1	0	0	1	0
-3 V_{dc}	1	0	1	0	0

3.1 PDPWM Strategy

This method is one of the PWM techniques. In this work, six carriers are applying for chosen MLI. All carriers are having amplitude as 1V. The sinusoidal reference wave is placed at the middle of the six carriers. In PDPWM technique all carriers are established in a same manner.

3.2 PODPWM Strategy

This method is same as PDPWM but carrier establishment is some what different. The carriers are uniformly divided into two groups based on positive/negative average levels. In this type the two groups are opposite in phase with each other while remaining in phase surrounded by the group.

3.3 APODPWM Strategy

This method is also same as PDPWM technique but one of the main different in APODPWM by evaluate to the PDPWM is that the alternate carriers are phase altered by 180 degree with each other.

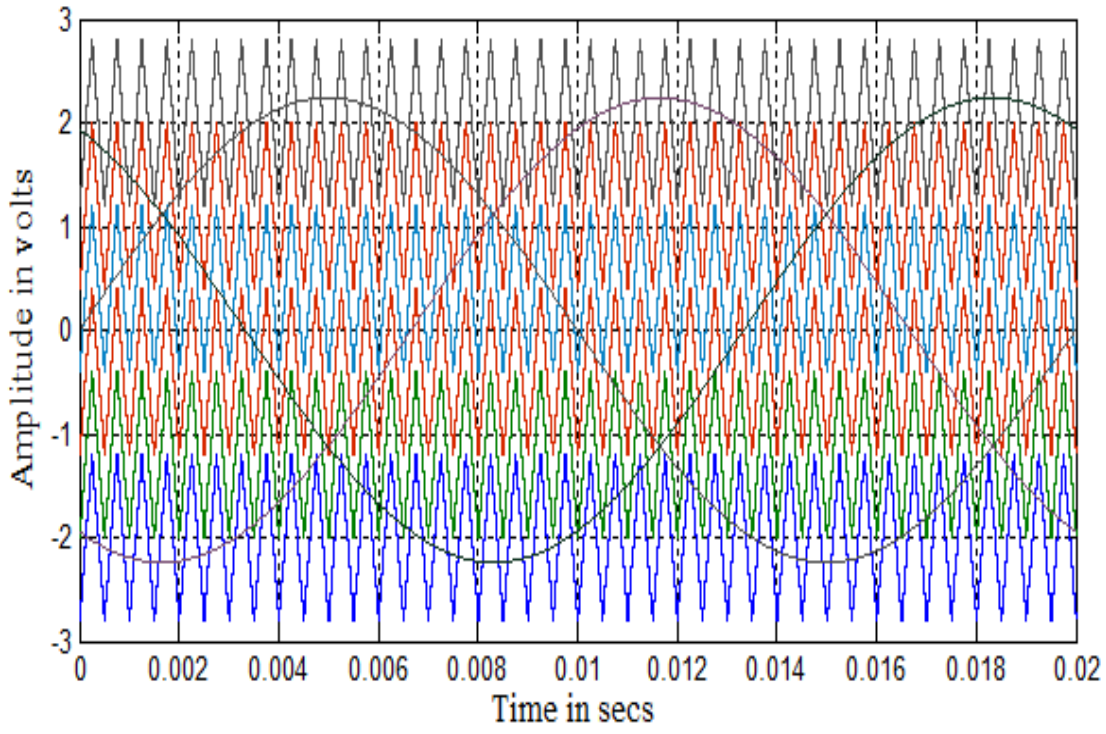

Figure 2. Modulating and Carrier Waveforms for COPWM Strategy (m_a=0.8 and m_f=40)

3.4 VFPWM Strategy

This method is one of the PWM techniques and it is same as PDPWM but intermittent carrier having different frequency compare to upper and lower carrier. The carrier arrangement for this strategy is shown in Figure 3.

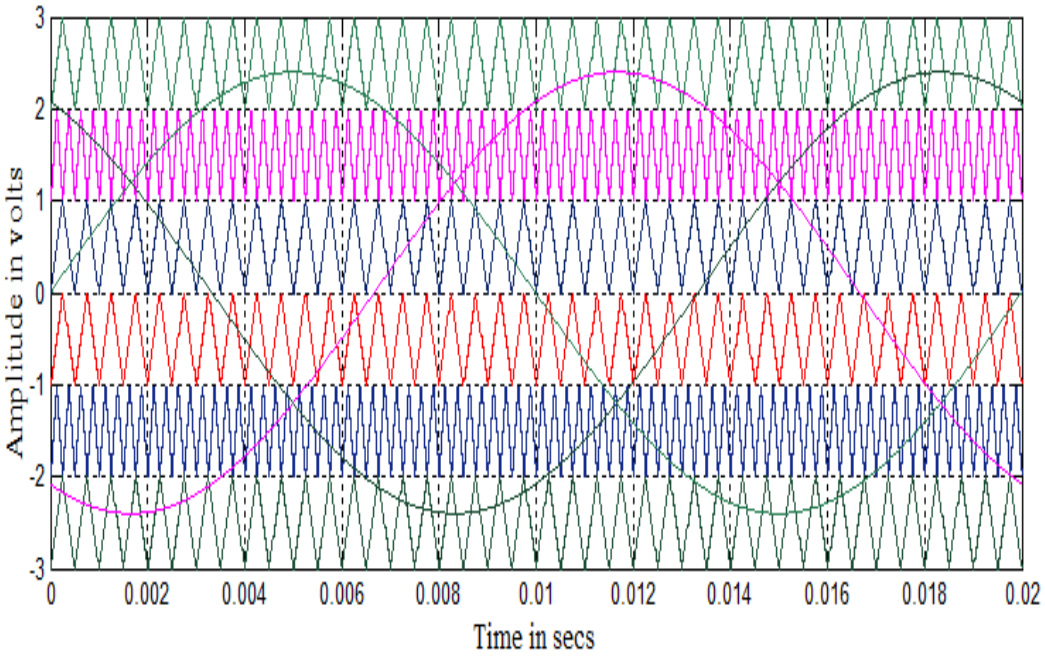

Figure 3. Modulating and Carrier Waveforms for VFPWM Strategy (m_a=0.8 and m_f=40)

3.5 COPWM Strategy

This method is same as PDPWM method but all carriers are overlapped each other and overlapping amplitude is 0.8V but each carrier having amplitude 1.6V and the total amplitude of this technique is 2.8. The carrier arrangement for this strategy is shown in Figure 2.

4. Simulation Results and Analysis

The three phases chosen seven level inverter is modeled in SIMULINK using power system block set. Switching signals for MLI are developed using sinusoidal PWM techniques discussed previously. Simulation is performed for different values of m_a ranging from 0.6–1. The corresponding %THD values are measured using FFT block and they are shown in Tables III. Next table displays the V_{RMS} of fundamental of inverter output for same modulation indices.

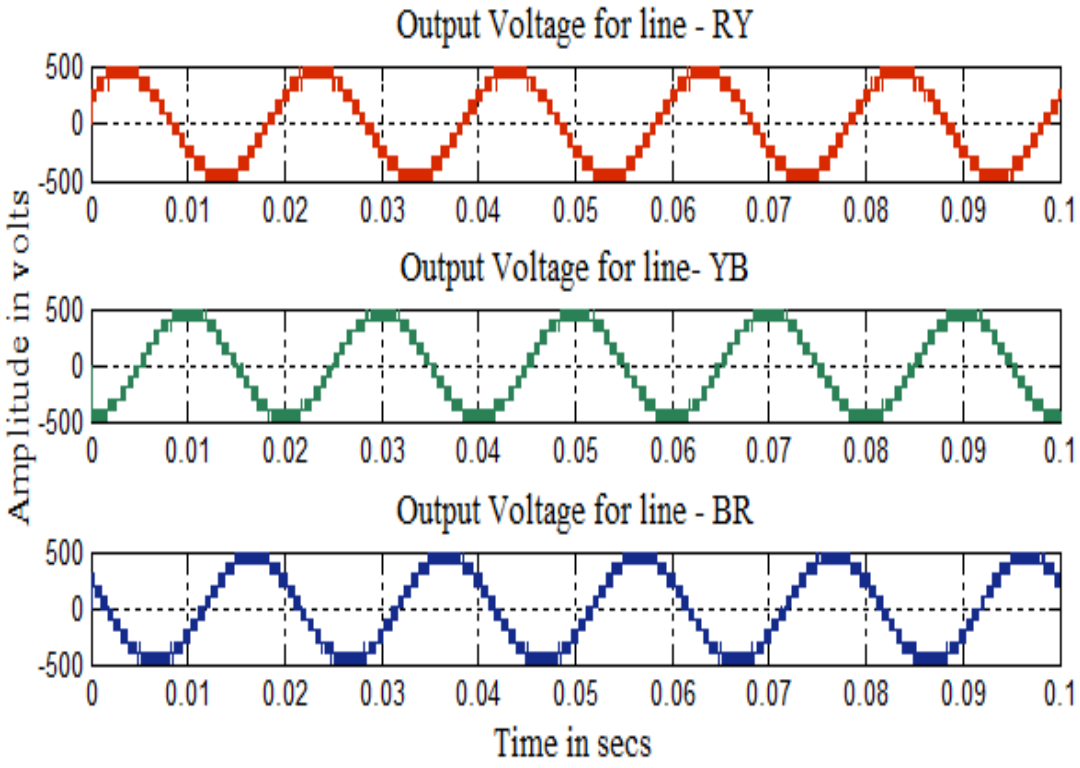

Figure 4. Simulated Output Voltage Generated by COPWM Technique for R Load

Table 3. % THD of Output Voltage of Chosen MLI for Various Modulating Indices

m_a	PD	POD	APOD	VF	CO
1	10.9	15.3	14.99	13.36	13.68
0.9	12.8	20.7	18.13	15.13	12.55
0.8	13.31	22.06	19.73	18.06	12.97
0.7	16.66	20.14	23.81	20.13	13.38
0.6	17.61	29.98	28.72	23.85	16.77

Table 4. $\%V_{RMS}$ (Fundamental) of Output Voltage of Chosen MLI for Various Modulating Indices

m_a	PD	POD	APOD	VF	CO
1	367.3	366.8	367.1	367.3	388.9
0.9	330.8	330.8	331.5	331	361.8
0.8	293.7	293.8	293.7	293.5	333
0.7	257.4	363.5	257.3	257.3	298.3
0.6	220.2	220.3	220.4	220.2	255.6

Table 5. Form Factor of Output Voltage of Chosen MLI for Various Modulating Indices

m_a	PD	POD	APOD	VF	CO
1	2295.6	12226.6	12236.6	6121.6	3889
0.9	3675.5	11026.6	11050	5516.6	3015
0.8	2670	7345	7342.5	2935	6660
0.7	990	8566	25730	2573	14915
0.6	3670	7343.33	11020	7340	4260

The followings are observed from the FFT spectra:

1. Harmonic energy above 3 % is present in (i) 4^{th}, 5^{th}, 6^{th}, 8^{th}, 12^{th}, 14^{th}, 18^{th}, 20^{th}, 24^{th}, 26^{th}, 30^{th}, 32^{nd}, 36^{th} and 38^{th} orders in PDPWM strategy. (ii) 27^{th}, 29^{th}, 35^{th} and 39^{th} orders in PODPWM strategy. (iii) 33^{rd}, 35^{th} and 39^{th} orders in APODPWM strategy. (iv) 20^{th}, 24^{th}, 26^{th}, 30^{th}, 32^{nd}, 36^{th} and 38^{th} orders in VFPWM strategy. (v) 2^{nd}, 4^{th}, 5^{th}, 6^{th}, 7^{th}, 13^{th}, 14^{th}, 20^{th}, 24^{th}, 26^{th}, 28^{th}, 30^{th}, 32^{nd}, 36^{th}, 38^{th} and 39^{th} orders in COPWM strategy.
2. 2^{nd} harmonic are dominant in COPWM strategy.
3. Dominant lower side band harmonic (40th order) is not present in all PWM strategies.
4. PDPWM and COPWM contain more number of dominant harmonics.
5. Among the five strategies APODPWM and PODPWM contain minimum harmonic energy whereas least number of harmonics exists in APODPWM strategy.
6. Among the non-overlapping PWM strategies, APODPWM contain relatively minimum harmonic energy with the least number of dominant harmonics.

The following parameter values are used for simulation: V_{dc}=100V, f_c=2000Hz, f_m=50Hz and R (load) = 100 ohms.

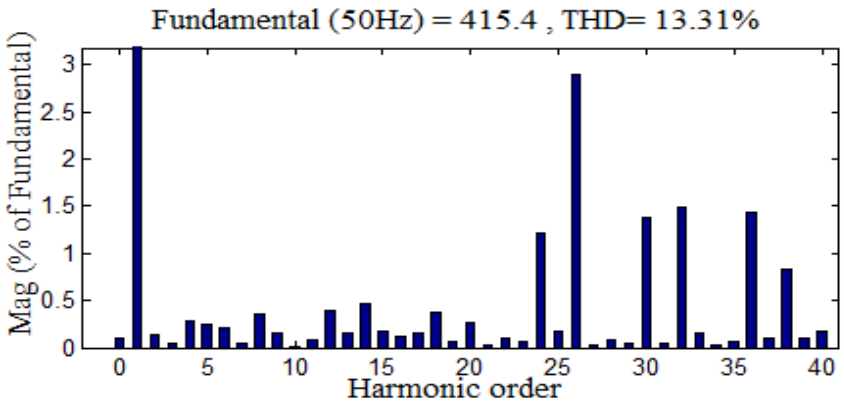

Figure 5. FFT Spectrum for PDPWM Technique (m_a=0.8 and m_f=40)

Table 6. Crest Factor of Output Voltage of Chosen MLI for Various Modulating Indices

m_a	PD	POD	APOD	VF	CO
1	1.4144	1.4141	1.4141	1.4144	1.4139
0.9	1.4144	1.4144	1.4142	1.4142	1.4140
0.8	1.4143	1.4146	1.4144	1.4143	1.4144
0.7	1.4141	1.4144	1.4139	1.4143	1.4140
0.6	1.4141	1.4144	1.4138	1.4141	1.4143

Table 7. Distortion Factor of Output Voltage of Chosen MLI for Various Modulating Indices

m_a	PD	POD	APOD	VF	CO
1	0.0575	0.0249	0.0183	0.0178	0.0463
0.9	0.1109	0.0249	0.0187	0.0938	0.0102
0.8	0.0424	0.0242	0.0258	0.0421	0.1557
0.7	0.0415	0.0269	0.0273	0.0331	0.0867
0.6	0.0447	0.0466	0.019	0.0503	0.0812

4. Conclusion

In this paper various new proposal adopting the constant switching frequency multicarrier CFD concepts are developed and simulated for chosen seven level inverter. Performance indices like %THD, V_{RMS} (indicating the amount of DC bus utilization), CF, FF and DF related to power quality issues have been evaluated, presented and analyzed. By comparing among the conventional PWM techniques, COPWM technique offers the less THD value (Table 3) and also offer a higher fundamental RMS output voltage (table 4).Table 5 shows FF for all modulating indices. Table 6 displays CF for all chosen modulating indices. Table 7 displays DF for all chosen modulating indices. The result indicate that appropriate COPWM and VACOPWM strategies have to be employed depending on the performance measure required in a particular application of MLI based on the criteria of output voltage quality (Peak value of the fundamental, THD and dominant harmonic components).

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