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Low-power high-speed FinFET DRAM array using sleep transistors

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ABSTRACT

Dynamic random-access memory (DRAM) is a fundamental memory technology widely employed in modern digital systems because of its high storage density and simple cell structure. However, conventional DRAM cells suffer from considerable power dissipation and propagation delay, which limit their suitability for high-speed and low-power applications. This paper presents three novel FinFET-based DRAM architectures incorporating sleep transistor techniques to reduce power consumption while improving operating speed. The proposed designs include a 2T-DRAM with sleep transistors and two configurations of 3T-DRAM with sleep transistors. The FinFET technology enhances switching performance and reduces propagation delay, whereas the sleep transistor technique effectively suppresses leakage, dynamic, and short-circuit power during memory operations. The proposed DRAM cells are designed and evaluated using the cadence virtuoso analog design environment. Simulation results demonstrate significant improvements over conventional DRAM architectures. The proposed 2T-DRAM achieves a 66% reduction in write delay, while the proposed 3T-DRAM achieves up to a 98% reduction in read delay. Furthermore, write power consumption is reduced by 56.8%, 63.02%, and 99.6% for the 2T, 3T-B, and 3T-C configurations, respectively. During read operations, power consumption is reduced by 99.8%, 99.5%, and 99.8%, respectively. These results demonstrate that the proposed FinFET DRAM architectures provide an effective solution for high-speed, low-power embedded memory applications.

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1. INTRODUCTION

Memory is one of the fundamental components of modern digital systems, enabling data storage and processing in applications ranging from portable consumer electronics to high-performance computing, cloud servers, artificial intelligence, and defense systems [1]–[3]. The rapid advancement of these technologies has substantially increased the demand for memory architectures that simultaneously provide high speed, low power consumption, and compact silicon area. Consequently, optimizing the power-performance-area (PPA) characteristics of memory circuits has become one of the major challenges in contemporary very large-scale integration (VLSI) design [4]. Among semiconductor memories, dynamic random-access memory (DRAM) is widely employed because of its simple cell structure, high storage density, and low fabrication cost [5], [6]. Unlike static random-access memory (SRAM), DRAM requires fewer transistors per memory cell, allowing

significantly higher memory capacity within the same chip area [7]. However, DRAM stores binary information as electrical charge in a storage capacitor, making it a volatile memory that requires periodic refresh operations to compensate for charge leakage [8].

As CMOS technology continues to scale into deep nanometer technologies, leakage current, propagation delay, and power dissipation have become critical challenges that limit the performance and energy efficiency of conventional DRAM architectures [9], [10]. Several approaches have been proposed to reduce DRAM power consumption while maintaining high operating speed. Low-power design techniques, including sleep transistors and power-gating methods, have proven effective in suppressing standby leakage current by disconnecting inactive memory cells from the power supply [11]–[13]. These approaches significantly reduce static power consumption without requiring major modifications to the memory architecture. Nevertheless, leakage reduction techniques alone are insufficient to overcome the performance degradation associated with aggressive complementary metal-oxide-semiconductor (CMOS) technology scaling. To address these limitations, fin field-effect transistor (FinFET) technology has emerged as an attractive alternative to conventional planar MOSFETs for advanced technology nodes below 22 nm [14]–[17]. Owing to its three-dimensional gate structure, FinFET provides superior electrostatic control over the channel, effectively suppressing short-channel effects, reducing leakage current, and improving process variation tolerance [18]. In addition, FinFET devices exhibit higher drive current, lower propagation delay, improved write/read stability, and reduced power-delay product compared with conventional CMOS technology [19]–[21]. These characteristics make FinFET technology particularly suitable for implementing next-generation low-power and high-speed memory circuits [22]. Recent studies have investigated various DRAM architectures based on FinFET devices, low-transistor-count memory cells, and leakage reduction techniques [23]–[27]. Although these approaches have demonstrated improvements in either power efficiency or operating speed, most studies focus on a single optimization strategy. The combined advantages of FinFET technology and sleep transistor-based power gating have not been fully explored for low-transistor-count DRAM cells [28]. Furthermore, comprehensive evaluations of multiple FinFET DRAM configurations under identical design conditions remain limited [29], [30].

To address these research gaps, this paper proposes three novel FinFET-based DRAM architectures incorporating sleep transistor techniques, namely a 2T-DRAM with sleep transistors and two different configurations of 3T-DRAM with sleep transistors. The proposed designs combine the superior switching characteristics of FinFET devices with power-gating mechanisms to reduce leakage, dynamic, and short-circuit power while improving read and write performance. The proposed memory cells are designed and analyzed using the cadence virtuoso analog design environment. Simulation results demonstrate substantial reductions in propagation delay and power consumption, indicating that the proposed architectures provide an effective solution for future high-speed, low-power embedded memory and VLSI applications.

2. OPERATING PRINCIPLE OF FINFET DRAM CELLS

2.1. Operating principle of conventional 2T FinFET DRAM cell

The conventional 2T FinFET DRAM cell is illustrated in Figure 1. It consists of two FinFET transistors and one storage capacitor for storing a single bit of information. The cell operates in two modes: write and read. During the write operation, the write word line (WWL) is activated, allowing the data on the write bit line (WBL) to charge or discharge the storage capacitor according to the input logic level. A charged capacitor represents logic '1', whereas a discharged capacitor represents logic '0'. During the read operation, the write path is disabled and the read word line (RWL) is enabled. The stored charge controls the conduction state of the read transistor, thereby producing the corresponding logic level at the read bit line (RBL). Since the stored charge gradually leaks through parasitic leakage currents, periodic refresh operations are required to preserve the stored data.

2.2. Operating principle of conventional 3T FinFET DRAM cell

The conventional 3T FinFET DRAM cell is shown in Figure 2. The circuit consists of three FinFET transistors and one storage capacitor. Compared with the 2T structure, the additional transistor provides an independent read path, thereby improving read stability and minimizing disturbance to the stored data. During the write operation, the WWL is asserted while the RWL remains inactive. The input data applied to the WBL charges or discharges the storage capacitor, representing logic '1' or logic '0', respectively. During the read operation, WWL is deactivated and RWL is enabled. The voltage stored in the capacitor controls the read transistor, allowing the stored data to be sensed at the RBL. The separated read and write paths reduce read disturbance and improve access reliability compared with the conventional 2T DRAM cell. Nevertheless, as a dynamic memory structure, the stored charge gradually decays over time due to leakage currents, making periodic refresh operations necessary to maintain data integrity.

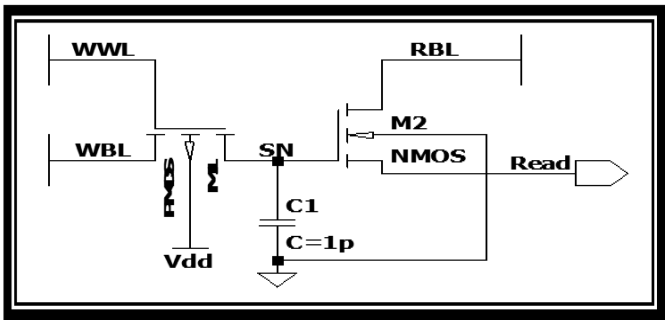

Figure 1. Conventional 2T-DRAM

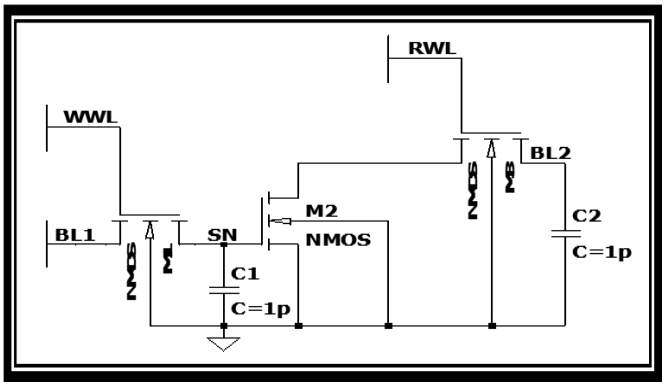

Figure 2. Conventional 3T-DRAM

3. METHOD

3.1. Proposed design and implementation

The overall design methodology adopted in this study is illustrated in Figure 3. The proposed workflow begins with the selection of conventional 2T and 3T DRAM cells implemented using FinFET technology as the baseline architectures. Subsequently, the sleep transistor technique is incorporated into the conventional cells to reduce leakage power while preserving their operating characteristics. The modified memory cells are then designed and simulated using cadence virtuoso [31]. Finally, the proposed architectures are evaluated in terms of write delay, read delay, and power consumption, and their performance is compared with the conventional designs to determine the effectiveness of the proposed approach.

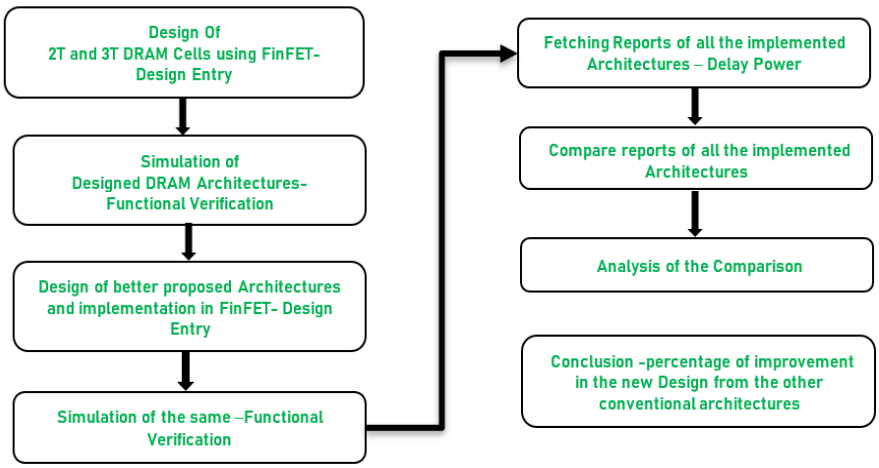

Figure 3. Flowchart of the methodology

Figure 3 presents the complete methodology adopted in this work. The primary objective is to optimize the PPA characteristics of DRAM cells. Since DRAM inherently occupies a smaller silicon area than SRAM, and technology scaling has already minimized the cell area, this work primarily focuses on reducing power consumption and improving operating speed. The proposed methodology combines FinFET technology with the sleep transistor technique. FinFET devices provide superior electrostatic control and lower propagation delay than conventional CMOS transistors, while sleep transistors significantly reduce leakage current during standby operation. The effectiveness of the proposed designs is evaluated by measuring the read delay, write delay, and average power consumption, followed by a comparative analysis with the conventional DRAM architectures.

The sleep transistor technique employed in this work is illustrated in Figure 4. A sleep transistor is a high-threshold-voltage (high-(V_T)) MOSFET that disconnects the logic circuit from the power supply during standby mode, thereby minimizing leakage current. Depending on its location, the sleep transistor can be implemented either as a header switch, using a p-type MOSFET connected between the circuit and the (V_{DD}) supply, or as a footer switch, using an n-type MOSFET connected between the circuit and ground. As shown in Figure 4, the footer-switch configuration is adopted because of its lower area overhead and effective leakage reduction. During active operation, the sleep transistor remains ON, allowing the circuit to function normally. During standby mode, it is turned OFF, effectively isolating the circuit from the power supply and significantly reducing static power dissipation without affecting normal read and write operations.

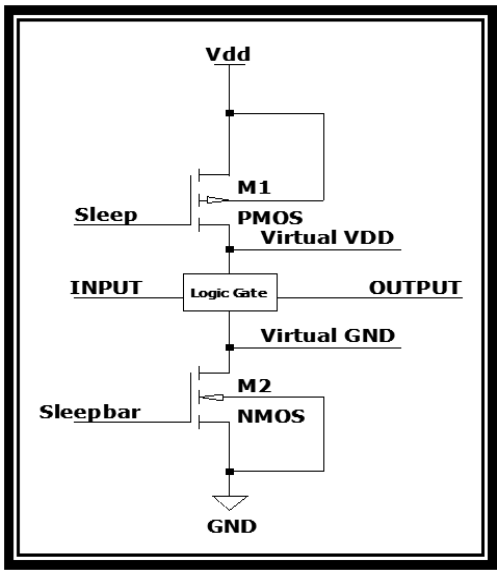

Figure 4. Block diagram depicting sleep transistor technique

As illustrated in Figure 4, the sleep approach decreases sub threshold leakage by separating the gates from the power source and ground. The sleep transistor is used between VDD and the pull-up network, as well as between GND and the pull-down network, in this approach. In idle mode, the sleep transistor switches off the circuit by shutting off the power rails, thus reducing leakage power. The sleep transistor for the pull up network is M1, whereas the sleep transistor for the pull-down network is M2. These two transistors safeguard the logic gate.

3.1.1. 2T-DRAM with sleep transistor

The novel FinFET 2T-DRAM is designed using two sleep transistors as shown in the Figure 5. The two sleep transistors – one PMOS and another NMOS receive inverted inputs so that it helps to enable the entire circuitry for the operations to be conducted. The write transistor and the capacitor which is grounded is placed between the sleep transistors. The read transistor is incorporated towards the read output. The write and read inputs are given to the write and read transistors respectively. The circuit diagram of the proposed 2T-DRAM with sleep transistors is as shown in the circuit diagram Figure 5. The inverted input for the sleep transistors is given via a NOT gate as shown. The write and read operations waveform of the proposed 2T-DRAM is shown in Figure 6 .and Figure 7 respectively.

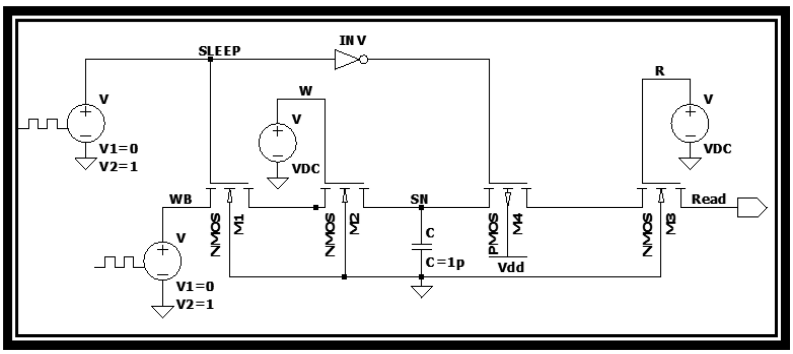

Figure 5. Proposed 2T-DRAM with sleep transistors

The waveforms show that the write and read operations occur during the read and write enabled periods. In Figure 6 it can be seen that write operation happens only when sleep is logic high. When W is high WB is stored to the capacitor. In Figure 7 shows read operation of proposed 2T-DRAM with sleep transistors. When sleep and R is high and W is low the charge stored in capacitor is read.

Figure 8 show schematics of the proposed 2T-DRAM array. The schematic was built in cadence and the read, write and power plots were obtained for the same. This 2T-DRAM is designed with sleep transistor in a simple manner where there is the actual circuitry of the access transistor alternative to the two sleep transistors.

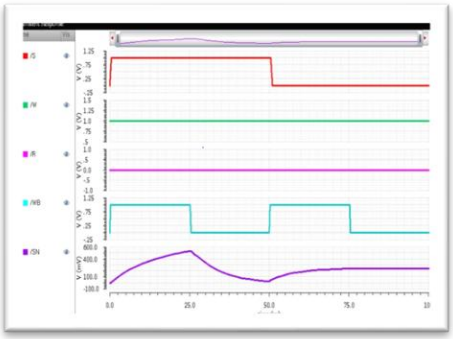

Figure 6. Write and read operation of proposed 2T-DRAM with sleep transistors

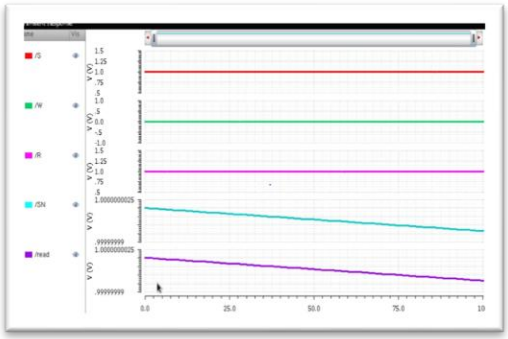

Figure 7. Read operation of proposed 2T-DRAM with sleep transistors

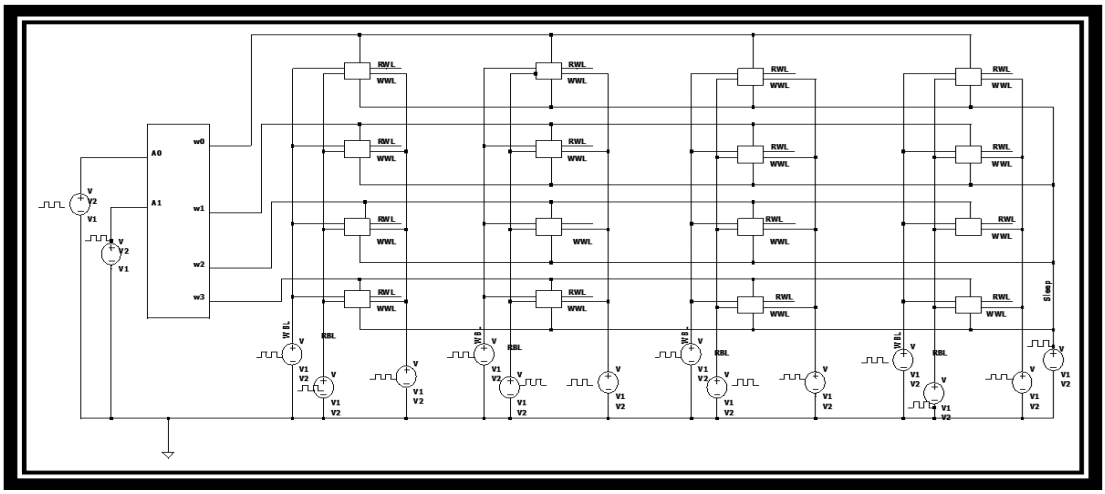

Figure 8. Schematic of proposed 2T-DRAM array with sleep transistors

The first step as discussed earlier is to enable the sleep transistors. Once the sleep transistors are enabled, the main circuitry is now enabled for the read and write operations. Now, the access transistor has to be enabled for operations. When the circuit is not in use the sleep transistors are off which prevents the leakage power. To write logic '1', or '0', W has to be driven high and R must be driven to low while the WB value is '1' or '0' respectively and the same value will be written in the storage capacitor. For read operation, the R is driven to high while W is driven to low, the value stored in capacitor is read from the output read.

3.1.2. 3T-DRAM (B) with sleep transistor

The novel FinFET 3T-DRAM design is implemented with two sleep transistors. All the transistors used are nMOS transistors. Two capacitors are used to store the write value making the current steady and the output reading more accurate. A transistor is placed between the capacitors that are grounded. The centre-most transistor is driven high during both the write and read operation. While it is turned OFF when the circuitry is not under operation. The write transistor is between the sleep transistors and the read transistor is connected to the read line. The circuit diagram of the proposed 3T-DRAM(B) with sleep transistors is as shown in the circuit diagram Figure 9.

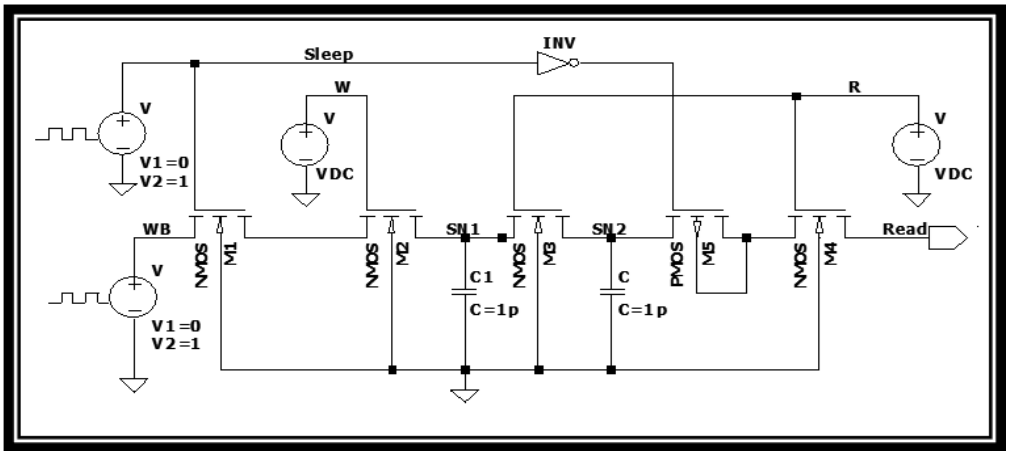

Figure 9. Proposed 3T-DRAM (B) with sleep transistors

Figure 10 shows both read and write operation of proposed 3T-DRAM(B) with sleep transistors. For write operation the sleep and the W must be logic high. For the read operation the sleep and R must be logic high and the stored value in capacitor is read.

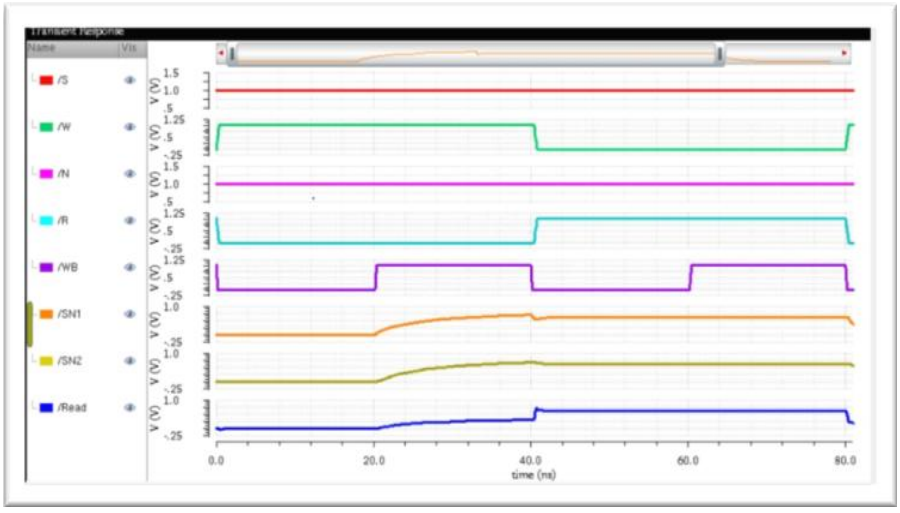

Figure 10. Write and read operation of proposed 3T-DRAM (B) with sleep transistors

The Figure 11 show the schematic of the proposed 3T-DRAM(B) array. This 3T-DRAM with sleep transistor is designed with two sleep transistors having the same input. The sleep transistors are enabled for the main circuitry to be enabled for the read and write operations. Now, the access transistor has to be enabled for operations. When the circuit is not in use the sleep transistors are off which prevents the leakage power. The centre-most transistor is also enabled by enabling N throughout the operations. To write logic '1', or '0', W has to be driven high and R must be driven to low while the WB value is '1' or '0' respectively and the same value will be written in the storage capacitors. For read operation, the R is driven to high while W is driven to low, the value stored in the capacitors discharge through the read capacitor and is read at the output terminal.

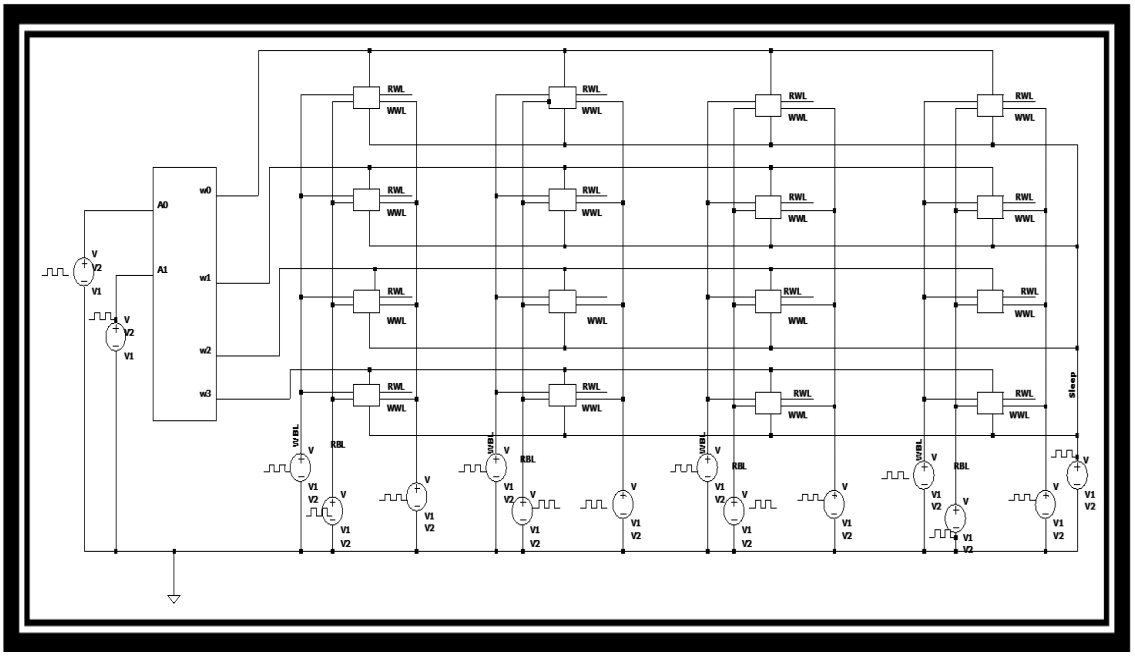

Figure 11. Schematic of proposed 3T-DRAM(B) array with sleep transistors

3.1.3. 3T-DRAM (C) with sleep transistors

This novel 3T-DRAM is implemented with three sleep transistors. With one pMOS transistor at the write line and five nMOS transistors. One capacitor is used to store the write value and is connected at the centre of the circuit. The ground of the capacitor is through the nMOS transistors. Unlike the previous circuits the sleep transistor is given'0' for write operation and is given '1' for read operation. The circuit diagram of the proposed 3T-DRAM(C) with sleep transistors is as shown in the circuit diagram Figure 12. The Figure.13 shows Write Operation of Proposed 3T-DRAM(C) with sleep transistors. For write operation the sleep and W is logic high and the value on WB is stored into the capacitor. The Figure14 shows read operation of proposed 3T-DRAM(C) with sleep transistors.

For read operation the sleep and R must be logic high and W must be logic low and then the value stored in the capacitor is read through the output pin. The Figures 15 show the schematic of the Proposed 3T-DRAM(C) array. The design of this 3T-DRAM with sleep transistor is done using three sleep transistors having the same input.

For write operation, the pMOS sleep transistor is enabled and the nMOS sleep transistors are disabled when the sleep transistors' gate is driven to '0'. W is made high and R is made low. The value of the WB is stored in the storage capacitor. For read operation, the pMOS sleep transistor is disabled and the nMOS sleep transistors are enabled when the sleep transistors' gate is driven to '1'. W is made low and R is made high. The value of the WB which is stored in the storage capacitor, discharges through the read transistor and read at the output terminal.

DRAMs of 4T and above were not given much attention during the selection of DRAM cells to be designed as SRAMs of 4T and above are available and preferred. 3T DRAMs have been concentrated on as we can have a single circuit for both write and read without interruption. Certain circuits of 4T-DRAM and above already exist [11], [15].

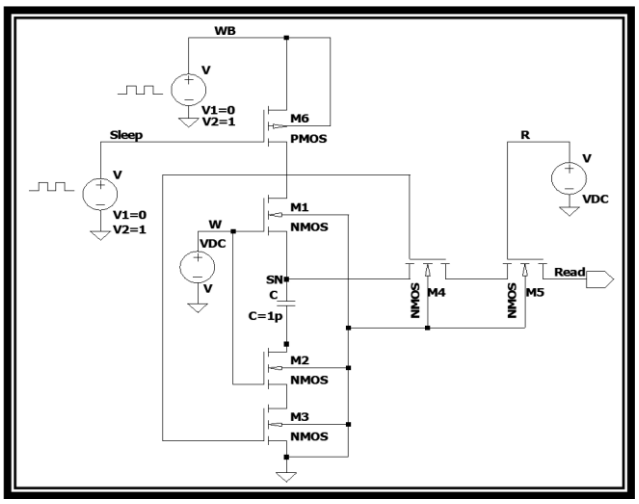

Figure 12. Proposed 3T-DRAM(C) with sleep transistors

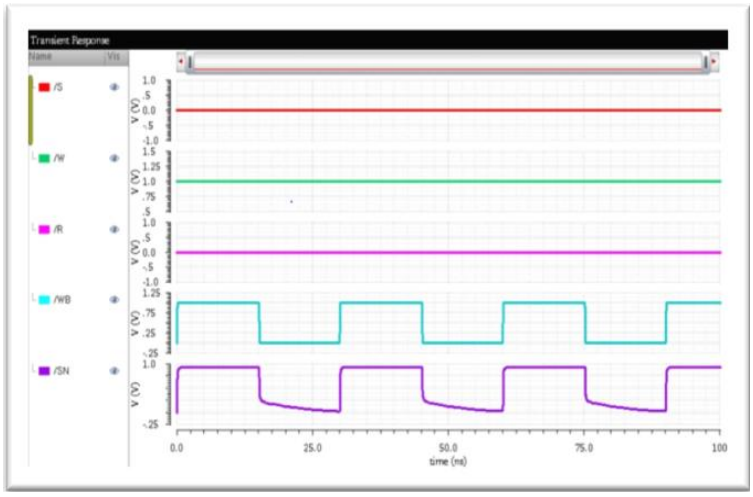

Figure 13. Write and read operation of proposed 3T-DRAM(C) with sleep transistors

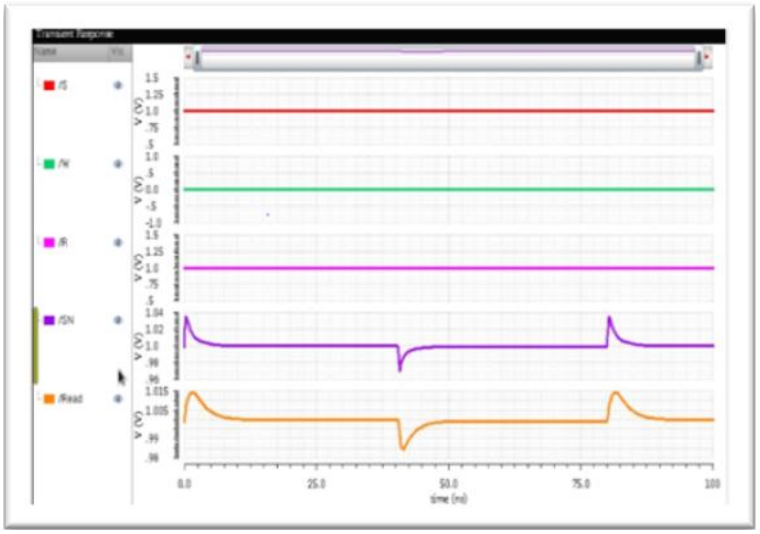

Figure 14. Read operation of proposed 3T-DRAM(C) with sleep transistors

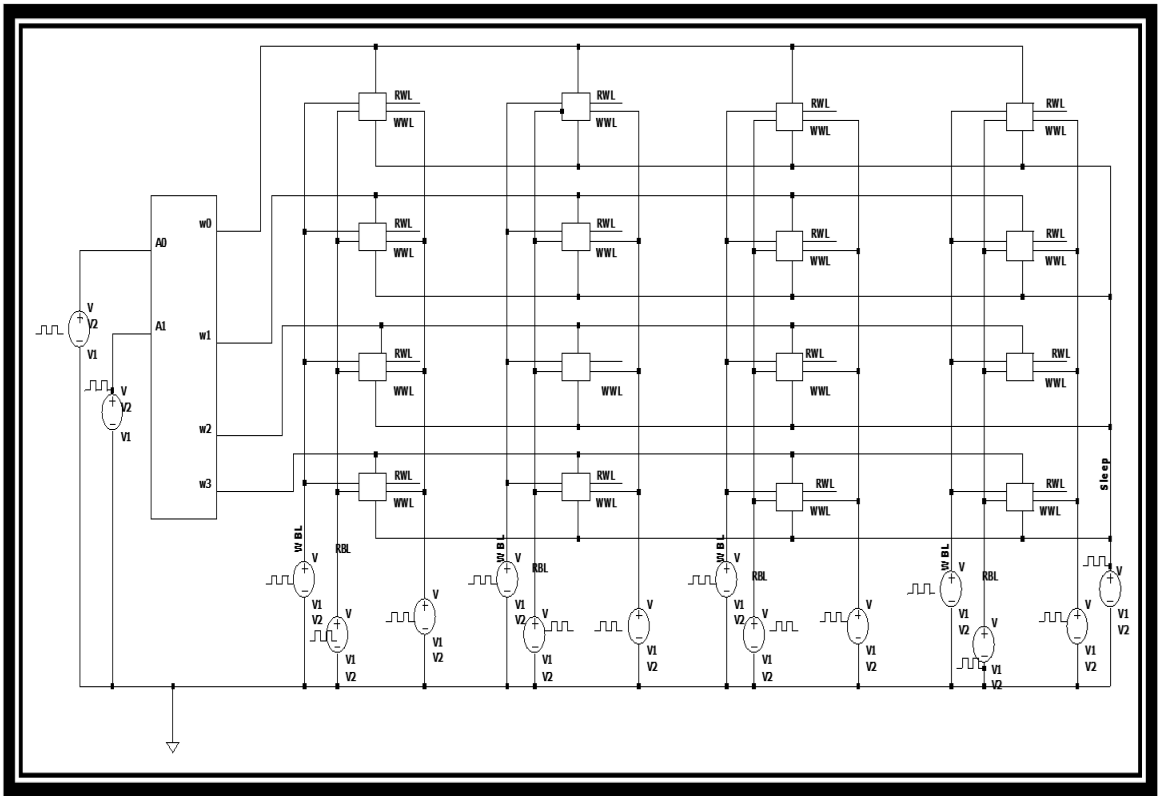

Figure 15. Schematic of proposed 3T-DRAM(C) array with sleep transistors

4. RESULTS AND DISCUSSION

Different DRAM designs–conventional and Proposed architectures with sleep transistors configuration are all implemented. These structures were implemented in cadence virtuoso using the FinFET technology library for 18nm. Also, the simulation and verification of the DRAM designs were done in the ADE environment offered by the cadence virtuoso tool from cadence.

The Table 1 contains delay and the percentages of improvement from the existing conventional architectures to the new proposed architectures of the cells and arrays. The Table 2 gives away the power details with respect to single Cell DRAMs – existing and proposed architectures. Whereas the Table 3 gives the power results obtained for the arrays. The tables give the data regarding which different architectures have optimised delay and consumed how much of power in both read and write operations of the circuit. In almost all the power reports that are concerned with the sleep transistor configuration, the sleep signals are such that they let the circuits to be active only for the half of the entire time period for which the circuits are simulated. The tables also have the percentage decrease of power consumption while using the novel proposed architectures compared to that of the conventional circuits. The delay and power reports of the existing DRAM circuits and the proposed novel circuits have been simulated and the values noted. As verified, The Delay is improved by 66% for write operation in 2T-DRAM and 98% for read operation in 3T-DRAM(C).

The novel proposed designs compared to its conventional counterpart. The novel proposed 2T-DRAM with sleep transistors circuit offers power reduction of 56.8% during the write and up-to 99.8% during the read operation compared to its conventional counterpart. Similarly, the 3T-DRAM(B) with sleep transistors that is proposed, offers a power reduction of 63.02% during the write operation, and up-to 99.5% during the read operation, compared to its conventional counterpart. The 3T- DRAM(C) with sleep transistors, also a proposed novel 3T-DRAM(C) cell, offers up- to 99.6% of power reduction during the write operation, and up-to 99.8% of power reduction during the read operation, compared to its conventional counterpart. Thus, the novel proposed 3T-DRAM(C) is proven to be providing the improved delay for read operation and the maximum power saving compared to others. Next are 2T-DRAM and 3T-DRAM(B) which are better than the conventional 3T-DRAM

Table 1. Comparison of delay in cells and array

DRAM designs			Delay (in nsec)		Percentage of improvement (%) (w.r.t. conventional)	
			Write	Read	Write	Read
Cell	2T	Conventional	38.09	0.012796	-66	59.58
		Proposed with sleep transistors	12.95	0.02042		
	3T	Conventional	6.432	0.09242	1.66	0.34
		Proposed(B) with sleep transistors	6.539	0.09273		
		Proposed(C) with sleep transistors	19.97	0.001838	210.5	-0.98
Array	2T	Conventional	51.02	24.73	-79	319
		proposed with sleep transistors	10.66	103.6		
	3T	Conventional	11.41	18.66	0.54	8.04
		Proposed(B) with sleep transistors	11.472	20.16		
		Proposed(C) with sleep transistors	33.21	12.79	191.06	-31.46

Table 2. Comparison of power consumption in cells

DRAM cells		Power consumption (in nW)		Percentage of improvement (%) (w.r.t. conventional)	
		Write	Read	Write	Read
2T	Conventional	14920	16860	-56.8%	-99.8%
	Proposed with sleep transistors	6432	31.48		
3T	Conventional	17410	6310	-63.02%	-99.5%
	Proposed(B) with sleep transistors	6437	31.48		
	Proposed(C) with sleep transistors	68.74	11.11	-99.6%	-99.8%

Table 3. Comparison of power consumption in arrays

DRAM arrays		Power consumption (in W)		Percentage of improvement (%) (w.r.t. conventional)	
		Write	Read	Write	Read
2T	Conventional	5.591m	752.6m	-99.99	-15.57
	Proposed with sleep transistors	10.66n	635.4m		
3T	Conventional	672m	21.164m	-54.2%	-98.6%
	Proposed(B) with sleep transistors	307.9m	296.3m		
	Proposed(C) with sleep transistors	216.4m	95.36m	-67.78	-99.55%

5. CONCLUSION

This paper presented low-power, high-speed FinFET-based 2T and 3T DRAM cells employing the sleep transistor technique to improve memory performance while reducing power consumption. Conventional and proposed DRAM architectures were designed and simulated using the Cadence Virtuoso analog design environment, and their performance was evaluated in terms of write delay, read delay, and power consumption. The simulation results demonstrate that integrating sleep transistors with FinFET technology significantly improves the power-performance characteristics of DRAM cells. The proposed 2T DRAM achieved approximately 66% reduction in write delay, while the proposed 3T DRAM (configuration C) achieved an approximately 98% reduction in read delay compared with their conventional counterparts. In terms of power consumption, the proposed architectures exhibited substantial improvements, with the proposed 3T DRAM (configuration C) providing the highest power savings, followed by the proposed 3T DRAM (configuration B) and the proposed 2T DRAM. Although several proposed configurations exhibit slightly higher delay during specific operations, this trade-off may be acceptable depending on the performance and energy requirements of the target application. Overall, the results confirm that the combination of FinFET technology and the sleep transistor technique provides an effective solution for designing energy-efficient DRAM cells without compromising operational functionality. The proposed architectures are therefore suitable for low-power, high-density memory applications where leakage reduction is a critical design objective.

Future work will investigate the scalability of the proposed DRAM cells by implementing larger memory arrays (e.g., 8×8, 16×16, and larger configurations) and evaluating their performance under process, voltage, and temperature (PVT) variations. Further studies may also explore adaptive sleep transistor control techniques, advanced FinFET technology nodes, and comparisons with emerging memory technologies to further enhance memory reliability, speed, and energy efficiency.

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