

Hardware Implementation of Cascaded Hybrid MLI with Reduced Switch Count

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Abstract

This paper presents the comparison of various multicarrier Pulse Width Modulation (PWM) techniques for the Cascaded Hybrid Multi Level Inverter (CHBMLI). Due to switch combination redundancies, there are certain degrees of freedom to generate the five level AC output voltage. This paper presents the use of Control Freedom Degree (CFD) combination. The effectiveness of the PWM strategies developed using CFD are demonstrated by simulation and experimentation. The simulation results indicate that the chosen five level inverter triggered by the developed Phase Disposition(PD), Phase Opposition and Disposition(POD), Alternate Phase Opposition and Disposition (APOD), Carrier Overlapping (CO), Phase Shift (PS) and Variable Frequency (VF) PWM strategies developed are implemented in real time using FPGA. The simulation and experimental outputs closely match with each other validating the strategies presented.

Keywords: CFD, FPGA, CHBMLI, PWM, bipolar

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1. Introduction

The term “multilevel converter” refers to the converter itself. Furthermore, the connotation of the term is that power can flow in one of two directions. Power can flow from the AC side to the DC side of the multilevel converter. This method of operation is called the rectification mode of operation. Power can also flow from the DC side to the AC side of the multilevel converter. This method of operation is called the inverting mode of operation. The term “multilevel inverter” refers to using a multilevel converter in the inverting mode of operation. Peny in [1] proposed a generalized multilevel inverter topology with self voltage balancing. Rodriguez, et al., [2] made a survey on topologies, control and applications of multilevel inverter. Corzine, et al., [3] analysed control of cascaded multilevel inverter. Jeevananthan et al proposed inverted sine carrier for fundamental fortification in PWM inverters and FPGA based implementation [4]. Rajesh gupta, et al., [5] developed switching characteristics of cascaded multilevel inverter controlled systems. Malinowski, et al., [6] also made a detailed survey on cascaded multilevel inverter. Abhisek maiti in [7] developed a microcontroller based inverted sine PWM switching technique for single phase inverter. Seyezhai and Mathur [8] suggested inverted sine pulse width modulated three phase cascaded multilevel inverter. Wu, et al., [9] proposed a two modulated digital control for three phase bi-directional inverter with wide inductance variation. Zabalza, et al., [10] developed a voltage balance control in three level neutral point clamped inverter using triangular carrier PWM modulation. Zadehbagheri and Payedar [11] discussed about the feasibility study of using space vector modulation inverters in two-level of integrated photovoltaic system. Ranjitha and Ravivarman [12] made a review on voltage balancing solutions in multilevel inverters. This paper discusses a comparative study carried out on various bipolar PWM strategies for chosen five level CHBMLI both by simulation and real time implementation.

2. Cascaded Hybrid Multilevel Inverter

The five-level hybrid cascaded inverter configuration is shown in Figure 1. By closing the appropriate switches, each H-bridge inverter can produce five different voltages $2V_{dc}$, V_{dc} , 0 , $-V_{dc}$, $-2V_{dc}$, depending on which switches that are switched ON. The DC source is connected to

all phase legs of the conventional three-phase, two-level inverter and the H bridge cell utilizes a capacitor as a voltage source. Assuming that the DC voltage is equal to $2V_{dc}$, then the voltage of the capacitor of the H-bridge cell has to be maintained to V_{dc} so that a five-level waveform is synthesized in the output. Considering a split DC source, the output of the two-level leg can be equal to either $+V_{dc}$ or $-V_{dc}$.

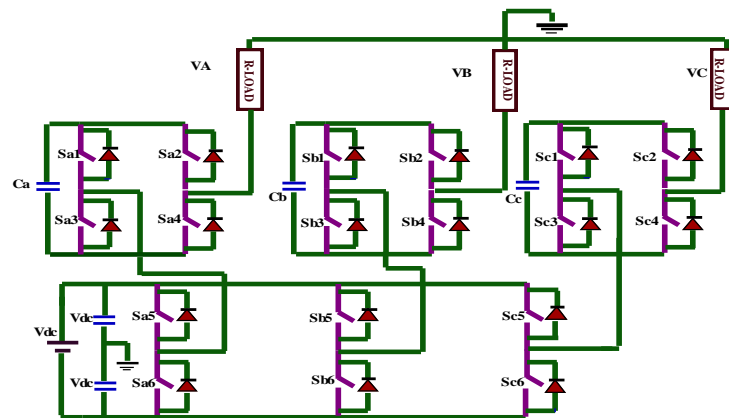


Figure 1. A Five Level Cascaded Hybrid Inverter

The voltage of the capacitor is affected during the converter states that the capacitor is connected to the load. These converter states occur during when the output voltage levels are $+2V_{dc}$ and $-2V_{dc}$ and during the zero voltage level. The capacitor is connected in such a way so that its voltage is opposite to the voltage of the lower phase-leg. Selection of the switching state is performed so that, together with the direction of the load current, the voltage of the floating capacitor is regulated within the predetermined limits.

The simulated and actual gate signals for the chosen five level CHBMLI are developed using MATLAB-SIMULINK and FPGA respectively. The gate signal generator model developed is tested for various values of modulation index. The results of the study are presented in this work in the form of the PWM outputs of the chosen multilevel inverter. The simulation and experimental results are compared and evaluated.

3. Modulation Strategies Based on CFD

We have used the intersection of a sine wave with a triangular wave to generate firing pulses. There are several modulation strategies possible for multilevel inverters. Here multicarrier modulation techniques with sine reference are presented. Number of triangular wave is compared with a controlled sinusoidal modulating signal. The number of carriers required to produce the m level output is $m-1$. Multiple degrees of freedom are available in carrier based multilevel PWM. Degrees of freedom exist in frequency, amplitude, phase, DC offset and multiple third harmonic content of carrier and reference signal.

MLIs have several CFDs. Multilevel carrier based PWM methods have more than one carrier option that can be triangular waves, saw tooth wave, a new function etc. As far as the particular carrier signals are concerned, there are multiple CFD including function, frequency, amplitude, phase of each carrier and offset between carriers. As far as the particular reference wave is concerned, there are also multiple CFDs including function, frequency, amplitude, phase angle of the reference wave. Therefore multilevel carrier based PWM method can have multiple CFD. These CFD combinations added with the basic topologies of MLI will produce many multilevel carrier based PWM strategies. The carrier waves can be either bipolar or unipolar. In this work, the bipolar multicarrier PWM based on CFD is considered. The modulating/ reference wave of multilevel carrier based PWM strategy is sinusoidal in this work. The frequency ratio m_f is defined in the bipolar PWM strategy as follows: $m_f = f_c / f_m$. In this paper, $m_f = 40$.

3.1. Phase Disposition PWM (PDPWM) Strategy

In this strategy uses four carriers, all these carriers have the same amplitude, frequency, and phase. Since all carriers are selected with the same phase. The PD PWM signal generation for modulation index $m_a = 0.8$ is shown in Figure 2.

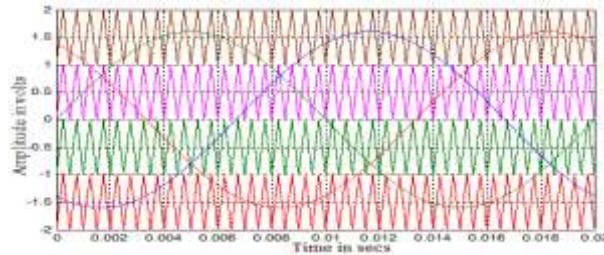


Figure 2. Carrier Arrangement for PDPWM Strategy with Sine Reference ($m_a=0.8$, $m_f=40$)

3.2. Phase Opposition and Disposition (PODPWM) Strategy

In this method uses two groups of carriers that is positive group and negative group carriers. The positive group carriers are phase shifted by 180 degrees with the negative group carriers. Since all carriers have the same frequency, phase and amplitude and but they are just different in DC offset to occupy contiguous bands. The PODPWM signal generation for $m_a = 0.8$ is shown in Figure 3.

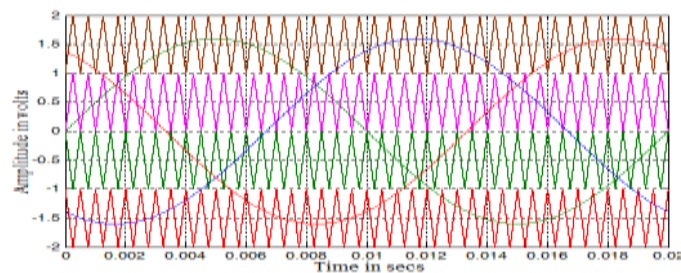


Figure 3. Modulating and Carrier Waveforms For PODPWM Strategy ($M_a = 0.8$ And $M_f = 40$)

3.3. Alternative Phase Opposition and Disposition (APODPWM) Strategy

The APODPWM signal generation for $m_a = 0.8$ is shown in Figure 4. In this method all carriers phase shifted 180 degree from its adjacent one. All these carriers have the same amplitude, frequency, and phase.

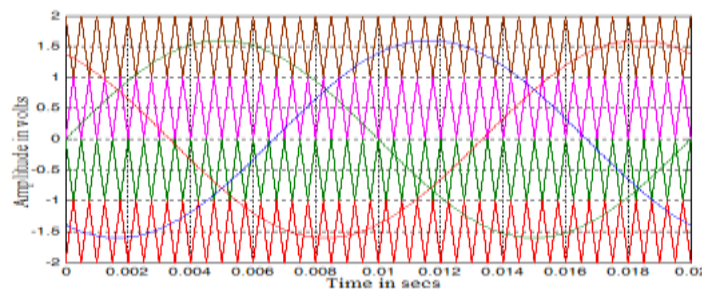


Figure 4. Modulating and Carrier Waveforms For APODPWM Strategy ($M_a = 0.8$ And $M_f = 40$)

3.4. Carrier Overlapping (COPWM) Strategy

In this method all carriers have the same frequency, and amplitude of carriers overlap with each other. Since all carriers are selected with the same phase, the method is known as CO strategy. The COPWM signal generation for $m_a = 0.8$ is shown in Figure 5.

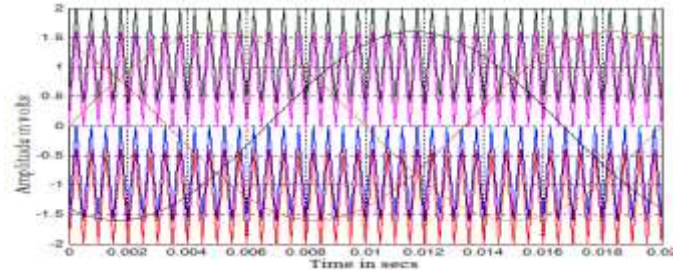


Figure 5. Modulating and Carrier Waveforms for COPWM Strategy ($m_a = 0.8$ and $m_f = 40$)

3.5. Variable Frequency (VFPWM) Strategy

The number of switchings for upper and lower devices of chosen MLI is much more than that of intermediate switches. This method having constant amplitude constant frequency. In order to equalize the number of switching for all the switches, variable frequency PWM strategy is used. The VFPWM signal generation for $m_a = 0.8$ is shown in Figure 6.

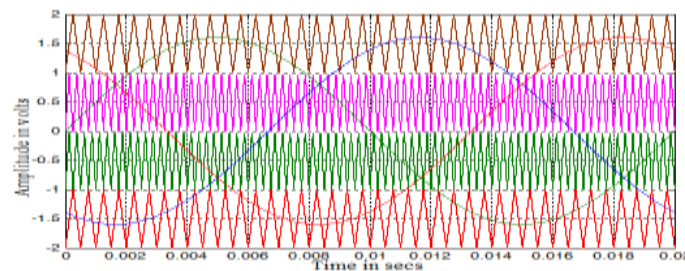


Figure 6. Modulating and Carrier Waveforms for VFPWM Strategy ($M_a = 0.8$ and $M_f = 40$ For Lower and Upper Switches and $M_a = 0.8$ And $M_f = 80$ for Intermediate Switches)

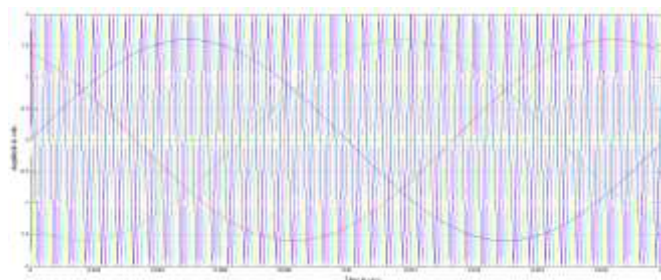


Figure 7. Modulating and Carrier Waveforms for PSPWM Strategy ($m_a = 0.8$ and $m_f = 40$)

3.6. Phase Shift (PSPWM) Strategy

The phase shift multi-carrier PWM technique uses in this work four carrier signals of the same amplitude and frequency which are shifted by 90 degrees to one another to generate the five level inverter output voltage.

4. Simulation Results and Analysis

4.1. Simulation Result

The chosen six topologies of five level inverter are simulated using SIMULINK - power system block set. Simulations are performed with different values of m_a ranging from 0.6 to 1 and resistive load of 100Ω . Simulated output voltages of chosen MLIs with various strategies are displayed only for a sample value of $m_a=0.8$. The following parameter values are used for simulation: $V_{dc1} = V_{dc2} = 220V$ and R (load) = 100Ω , $f_c = 2050$ Hz, $f_m = 50$ Hz, and $m_f = 40$.

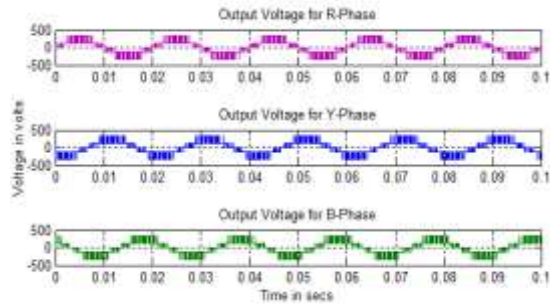


Figure 7. Output Voltage Generated by PDPWM Strategy with Sine Reference



Figure 8. Entire Hardware Setup



Figure 9. Experimental Output Voltage with PDPWM Strategy for R-Load



Figure 10. FFT Plot for PDPWM Strategy with R-Load

4.2. Hardware Results

This section presents the results of experimental work carried out on chosen CMLI using a FPGA-3E board which is based on the VPTB-05. Real time implementation of these strategies using VHDL coding requires less time for development as it can be expanded from the simulation blocks developed using MATLAB/SIMULINK. Spartan-3E Low Cost board which includes the following components and features 100,000-gate Xilinx Spartan-3E, XC3S100 E FPGA in a 144-Thin Quad Flat Pack package (XC3S100E- Q144), 2160 logic cell equivalents, Four 18K-bit block RAMs (72K bits), Four 18x18 pipelined hardware multipliers, Two Digital

Clock Managers (DCMs), 32 Mbit Intel Strata Flash, 3 numbers of 20 pin header to interface VLSI based experiment modules, 8 input Dip Switches, 8 output Light Emitting Diodes(LEDs), On Board programmable oscillator (3 to 200 MHz), 16x2 Alphanumeric LCD, RS232 UART, 4 Channel 8 Bit I2C based ADC & single Channel DAC, PS/2 Keyboard/Mouse, Prototyping area for user applications and on Board configuration Flash PROM XCF01S. The gate signal generation blocks using different PWM strategies listed above are designed and developed using VHDL coding and downloaded to FPGA. The results of the experimental study are shown in the form of the PWM outputs of chosen CHBMLI.



Figure 11. Experimental Output Voltage with PODPWM Strategy for Sine Reference



Figure 12. FFT Plot with PODPWM Strategy for R-Load



Figure 13. Experimental Output Voltage with APODPWM Strategy for R-Load



Figure 14. FFT Plot for APODPWM Strategy for R-Load



Figure 15. Experimental Output Voltage with COPWM Strategy for R-Load

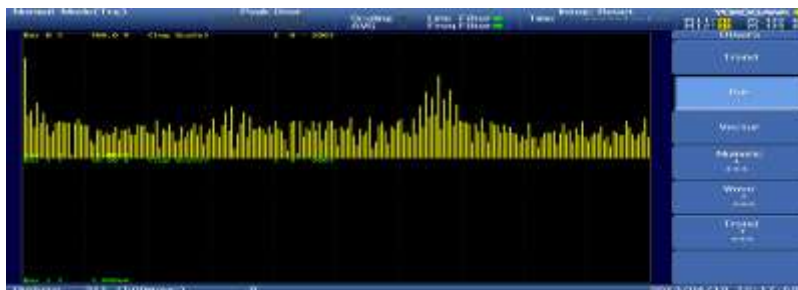


Figure 16. FFT Plot with COPWM Strategy for R-Load



Figure 17. Experimental Output Voltage with PSPWM Strategy for R-Load



Figure 18. FFT Plot with PSPWM Strategy for R-Load

Optocoupler circuit provides isolation between the control circuit and the power converter circuit. The optocoupler used is 6N137, which is an optically coupled gate that combines a GaAsP light emitting diode and an integrated high gain photo detector. An enable input allows the detector to be strobed. The output of the detector IC is in version of the applied input. The PWM signals from the FPGA are not capable of driving the MOSFETs. In order to strengthen the pulses a driver circuit is provided.



Figure 19. Experimental Output Voltage with VFPWM Strategy for R-Load



Figure 20. FFT Plot with VFPWM Strategy for R-Load

Table 1. % THD of Output Voltage of Chosen MLI for Various Modulating Indices (Hardware)

m_a	PD	POD	APOD	CO	VF	PS
1	28.9	23.2	22.79	31.0	26.4	27.6
0.9	35.8	29.1	30.84	37.1	33.7	36.0
0.8	42.6	34.3	34.03	31.0	38.9	42.3
0.7	44.0	35.2	37.49	50.6	37.8	44.0
0.6	38.7	34.7	33.36	58.6	31.1	39.6

Table 2. % V_{RMS} (Fundamental) of Output Voltage of Chosen MLI for Various Modulating Indices (Hardware)

m_a	PD	POD	APOD	CO	VF	PS
1	14.7	14.4	14.8	16.4	15.01	15.02
0.9	13.6	13.6	13.6	15.4	13.62	13.64
0.8	11.7	11.7	11.7	14.5	11.75	11.78
0.7	9.70	9.70	9.93	13.1	9.70	9.74
0.6	7.50	7.50	7.52	11.4	7.50	7.57

Table 3. Crest Factor of Output Voltage of Chosen MLI for Various Modulating Indices (Hardware)

m_a	PD	POD	APOD	CO	VF	PS
1	1.41	1.44	1.42	1.40	1.50	1.47
0.9	1.56	1.51	1.56	1.55	1.57	1.56
0.8	1.75	1.56	1.75	1.67	1.78	1.77
0.7	1.75	1.76	1.99	1.75	1.96	1.95
0.6	2	1.98	2.02	2.05	2.01	2.01

PWM outputs shown for only one sample value of $m_a=0.8$. After suitably scaling down the simulation values, in view of laboratory constraints, the peak-to-peak output voltage obtained experimentally is 40 V. The following parameter values are used for experimentation: $V_{dc1}=V_{dc2}=15$ V, $R(\text{load})=100$ Ω , $f_c=10$ KHz, $f_m=50$ Hz and $m_f=200$. Figure 8 shows the Entire Hardware setup for CHBMLI.

Table 4. Form Factor of Output Voltage of Chosen MLI for Various Modulating Indices (Hardware)

m_a	PD	POD	APOD	CO	VF	PS
1	190	144	150.4	82	150.1	150.2
0.9	147	136	136.3	77	136.2	136.4
0.8	136	117	117.7	72.5	58.75	58.9
0.7	48.5	97	33.11	65.5	32.33	32.46
0.6	25.0	37.5	37.62	57.4	25	25.23

5. Conclusion

Various bipolar PWM strategies have been developed for different modulation indices ranging from 0.6-1 for the chosen three phase CHBMLI. Various performance factors like (i) THD and harmonic spectra indicating purity of the output voltage (ii) V_{RMS} indicating the amount of DC bus utilization, (iii) CF shows the amount of stress applied to the devices and (iv) FF displays the DC content available at the output voltage have been evaluated, presented and analysed. The PWM outputs by simulation and experimentation closely match with each other validating the strategies presented.

References

- [1] Fang Zhang Peny. A generalized multilevel inverter topology with self voltage balancing. *IEEE Transactions on Industry Applications*. 2001; 37(2): 611- 618.
- [2] Jose Rodriguez, Jih-Sheng Lai, Fang Zheng. Multilevel Inverters: A Survey of topologies, controls and applications. *IEEE Transactions on Power Electronics*. 2002; 49(4): 724-738.
- [3] Corzine Keith, Wielebski Mike A, Peng Fang Z, Jin Wang. Control of cascaded multilevel inverter. *IEEE Transaction on Power Electronics*. 2004; 19(3): 732-738.
- [4] Jeevananthan S, Nandhakumar R, Dananjayan P. Inverted sine carrier for fundamental fortification in pwm inverters and FPGA based implementations. *Serbian Journal of Electrical Engineering*. 2007; 4(2): 171-187.
- [5] Rajesh Gupta, Arindam Ghosh, Avinash Joshi. Switching characterization of cascaded multilevel inverter-controlled systems. *IEEE Transactions on Industrial Electronics*. 2008; 55(3): 1047-1057.
- [6] Mariusz Malinowski, Gopakumar K, Jose Rodriguez, Marcelo A Perez. A Survey on cascaded multilevel inverters. *IEEE Transactions on Industrial Electronics*. 2010; 57(7): 2197-2206.
- [7] Abhisek Maiti. Development of microcontroller based ispmw switching technique for single phase inverter. *International Journal of Engineering Science and Technology*. 2011; 3(6): 5298-5305.
- [8] Seyezhai R, Mathur BL. Inverted sine pulse width modulated three phase cascaded multilevel inverter. *International Journal of Advances in Engineering and Technology*. 2012; 2: 602-610.
- [9] Wu TF Chang, CH Lin, LC Chang YC, Chang YR. Two modulated digital control for three phase bidirectional inverter with wide inductance variation. *IEEE Transactions on Power Electronics*. 2013; 28(4): 1598-1607.
- [10] Javier Chivite-Zabalza, Pedro Izurza-Moreno, Danel Madariaga, Gorka Calvo, Miguel Angel Rodriguez. Voltage Balancing control in 3-Level Neutral-Point Clamped Inverters Using Triangular Carrier PWM Modulation for FACTS Applications. *IEEE Transactions on Industrial Electronics*. 2013; 28(10): 4473-4484.
- [11] Mahmoud Zadehbagheri, Amin Payedar. The Feasibility Study of Using Space Vector Modulation Inverters in Two-Level of Integrated Photovoltaic System. *Indonesian Journal of Electrical and Computer Engineering*. 2015; 14(2): 205-214.
- [12] Ranjitha M, Ravivarman S. A Review on Voltage Balancing Solutions in Multilevel Inverters. *Indonesian Journal of Electrical and Computer Engineering*. 2016; 1(1): 53-59.