

Failure Analysis and Reliability Study of NAND Flash-Based Solid State Drives

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Abstract

This research focuses on conducting failure analysis and reliability study to understand and analyze the root cause of Quality, Endurance component Reliability Demonstration Test (RDT) failures and determine SSD performance capability. It addresses essential challenges in developing techniques that utilize solid-state memory technologies (with emphasis on NAND flash memory) from device, circuit, architecture, and system perspectives. These challenges include not only the performance degradation arising from the physical nature of NAND flash memory, e.g., the inability to modify data in-place read/write performance asymmetry, and slow and constrained erase functionality, but also the reliability drawbacks that limits Solid State Drives (SSDs) performance. In order to understand the nature of failures, a Fault Tree Analysis (FTA) was performed that identified the potential causes of component failures. In the course of this research, significant data gathering and analysis effort was carried out that led to a systematic evaluation of the components under consideration. The approach used here to estimate reliability utilized a sample of drives to reflect the reliability parameters (RBER, AFR, and MRR) over 1 year. It is anticipated that this study can provide a methodology for future reliability studies leading to systematic testing and evaluation procedure for SSD RDT's and critical components.

Keywords: Performance Analysis, Reliability, Solid State Devices

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1. Introduction

Many situations encountered in the engineering world, have a chance element associated with them such as variation in material properties, physical environments, loads, power and signal inputs. Some of the basic physical laws can be treated as deterministic – water seeks the lowest accessible level, objects float when they displace their own weight in liquid, etc. But many physical laws are probabilistic in nature. Since the beginning of history, humanity has attempted to predict the future by watching the flight of birds and the movement of leaves on the trees, to mention a few. Fortunately, today's engineers do not have to depend on a 'crystal ball' in order to predict the future of their products. Through the use of statistical tools for product life data analysis, reliability engineers can determine the probability and durability of components, and systems to perform their required functions for desired life span without failure. The product life data can be measured in hours, miles, cycles-to-failure, stress cycles or any other metric with which the life or exposure of a product can be measured.

A solid-state drive (SSD) is a data storage device using integrated circuit assemblies as memory to store data persistently. SSD technology uses electronic interfaces compatible with traditional block input/output (I/O) hard disk drives, thus permitting simple replacement in common applications.

The purpose of this research is to determine the performance capability of SSD NAND Flash by conducting Regression, Quality and Endurance Reliability Demonstration Test from reliability standpoint to assure the early identification of potential problems related to validation, firmware and NAND. The objectives are as follows:

1. Conduct a literature review on the methods used to perform a reliability study.
2. Gather failure data from the database for tests conducted.
3. Apply statistical tools and reliability methodologies to the failure data.
4. Analyze the results and determine the major causes of failure and predict the reliability of the component.

Quality and Reliability of a SSD includes initial product risk assessment, quality and reliability testing design, planning and scheduling, testing execution, testing result rollup and result interpretation There are three types of failures observed in a solid state drives:

- 1) **Bricked Drive:** Drive is undetectable by the system.
- 2) **Detected data error:** These errors are detected using CRC algorithm.
- 3) **Undetected data error:** These errors are undetected rendering corrupt Data.

The SSD drive reliability is characterized in terms of following parameters.

Annualized failure rate (AFR): It is the fraction of drives that fail in the field, per year. Manufacturers report 0.6-2.5% [1], but field data can be higher at 1.7-8.6% [2].

Mean time between failures (MTBF): This is the time elapsed between 2 consecutive field failures and is Equivalent to $1/AFR$.

Uncorrectable bit error rate (UBER): Number of data errors per bit read from the drive. Typically 1 in 10^{13} to 10^{16} for HDDs.

Undetected bit error rate: Number of undetected errors per bit read from the drive. Requirement can be same as uncorrectable for consumer drives, but enterprise requirements can be more stringent.

2. NAND/SSD Reliability

It can take a long time in development to get an SSD to the point where it is highly reliable and there is a strong need to balance reliability, cost, and complexity.

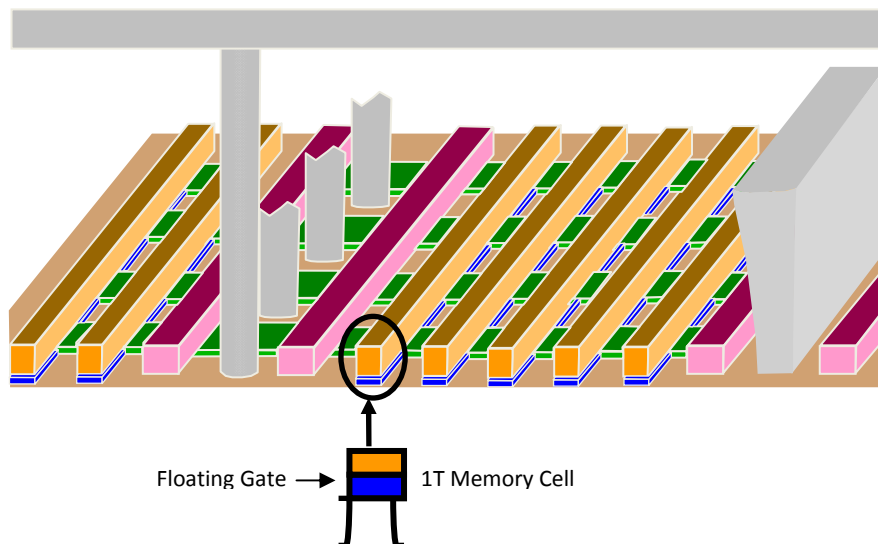


Figure 1. 3-D Structure of the transistor

The main reasons for NAND/SSD failures are

2.1. Charge Storage: Program and Erase

Approximately 90% of an SSD core is a memory array. Memory cell is a single transistor with gate (shown in Figure 1), source, drain, and channel. The NAND organization is shown in Figure 2.

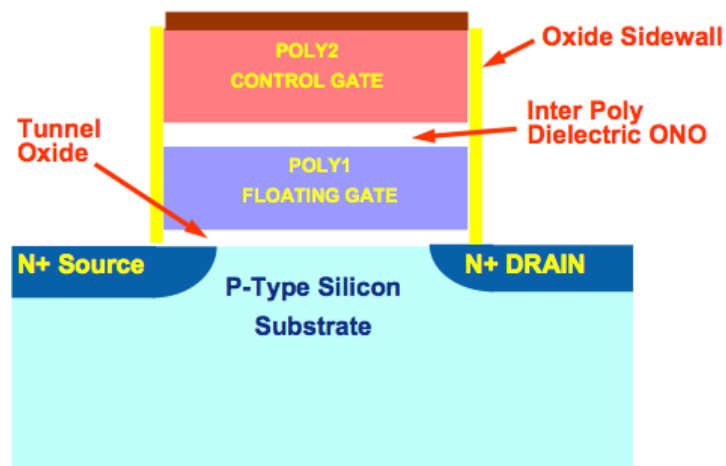


Figure 2. Structure of NAND Flash

In the memory cell, a “floating gate” (FG) is put below the control gate (CG). Negative charge on FG opposes the CG voltage, pushing the V_T higher. Positive charge on FG aids the CG voltage, pushing the V_T lower. NAND stores data by placing different cells at different V_T 's (as shown in Figure 3). Sensing circuitry detects the cell current and returns a 0 or a 1. Programming means injecting electrons to the FG and high CG voltage pulls electrons up. This is governed by quantum-mechanical tunneling through the “tunnel oxide” as shown in Figure 4 A. Erase means removing electrons from the FG-Tunneling in reverse direction.

2.2. Array Distributions and Multi-Level Flash

Single-level-cell (SLC) NAND has cells divided into two V_T levels (erased and programmed c.f. Figure 3). The FG charge varies from cell to cell, so that there are distributions of V_T 's for the programmed and erased states. Multi-level-cell (MLC) Flash has four levels. Sensing circuitry can distinguish 1's from 0's as long as the distributions *don't cross the read points*. Width of any level is called the state width. Space in between is the remaining read window budget.

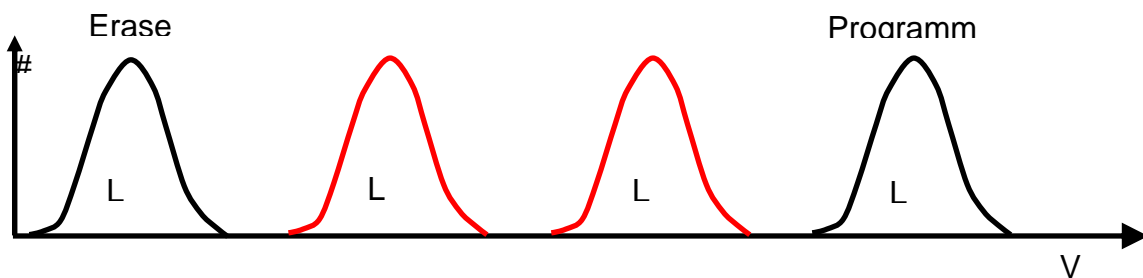


Figure 3. Array Distribution and Multi-Level Flash

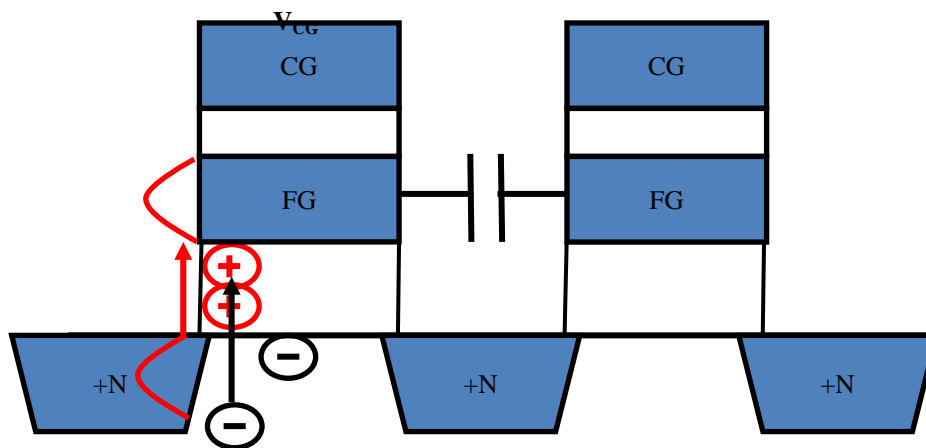


Figure 4. A. Quantum Tunneling in NAND Flash

2.3. Degradation of Tunnel Oxide

In a typical memory cell, one program operation is followed by an erase and this is called a program/erase cycle. As NAND is used, it can undergo many cycles. Cycling is a harsh stress inducing factor on the tunnel oxide. The magnitude of high electric field in the tunnel oxide is very large (> 10 million volts per cm). Owing to these factors (inclusive of thin oxide layer), lot of electrons pass through the oxide (tunneling). As a result, the oxide degrades and results into broken Atomic bonds, both in the bulk and at the interface, broken-bond sites can trap electrons that pass through, becoming electrically negative and tunnel oxide degradation (as shown in Figure 4 B)

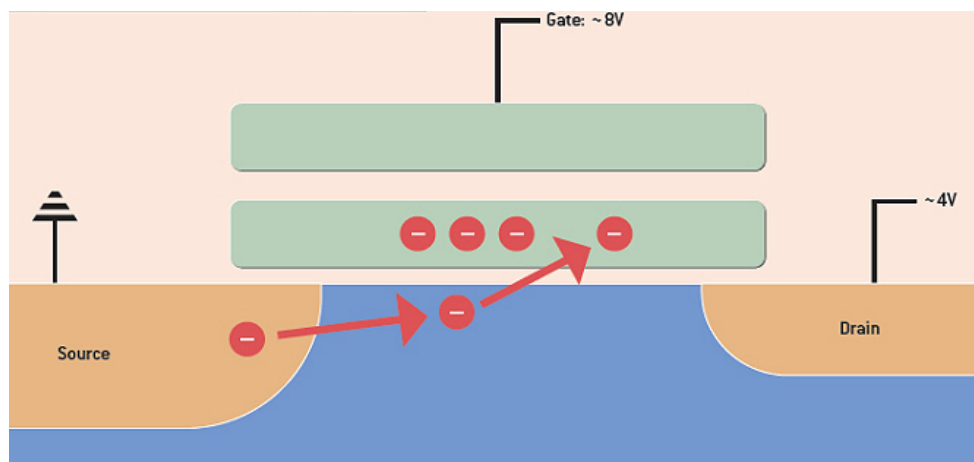


Figure 4. B. Degradation of Tunnel Oxide

Negative charge in tunnel oxide makes erase slower, program faster due to this is attributed to two effects that take place at the Gate-Substrate interfaces:

- Electrons in tunnel oxide repel channel electrons and raises the V_T which helps programming and hurts erase
- Electrons in tunnel oxide repel tunneling electrons and hurt both program and erase

As a result, erase slows down. Program has competing effects, net being slight speedup. When a block erases slower than datasheet, it **fails** and is retired. NAND datasheets allow 2% to 4% of blocks to fail in this way.

2.4. Write Errors

Bit errors occur during write because of following reasons. Some cells that are supposed to stay erased, end up programmed by mistake ("program disturb", PD), Some cells that are supposed to program to (say) L1, instead program to L2 ("overprogramming", OP), Some cells that are supposed to program never make it to their intended V_T level ("underprogramming") as shown in Figure 5. All these things get worse with cycling, because the trapped-up tunnel oxide gets worst with number of cycles.

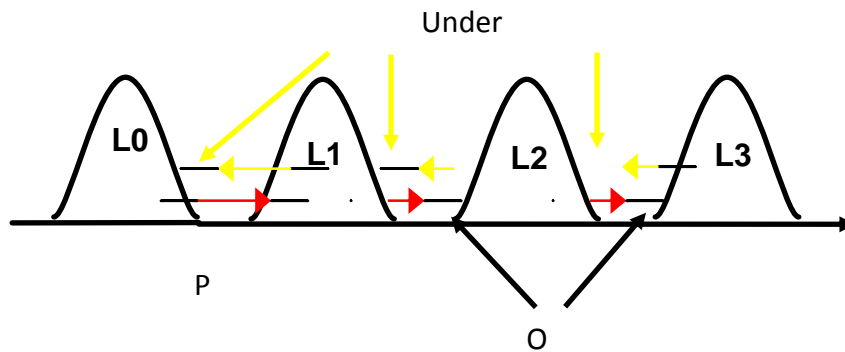


Figure 5. Underprogramming Write Error

2.5. Data Retention Errors

NAND is expected to retain data with the power off. There are two intrinsic mechanisms that cause programmed cells to lose V_T , primarily post-cycling

- **De-trapping:** The negative charge trapped in the tunnel oxide detraps from the oxide. Also called intrinsic charge loss (ICL)
- **SILC:** Electrons tunnel off the FG through broken bonds in the oxide. This is called stress-induced leakage current (SILC), also single bit charge loss (SBCL)

These mechanisms have different characteristics:

- De-trapping is a thermal effect with very little dependence on electric field
 1. Affects all three programmed levels, but mostly L1 & L2 because L3 usually has more margin
 2. Accelerated by high temperature bake (standard qualification test is 10 hours at 125°C)
- SILC, like all tunneling, is driven by electric field, not temperature
 1. Affects mostly L3, because L3 cells have the highest built-in electric field (programmed the highest)
 2. High-temperature bakes, the standard way of accelerating data loss, has no effect
- Both depend on traps in the tunnel oxide, so the retention time gets worse with cycling.
- Erasing/writing a block resets the retention clock to zero. You need to retain data only for the time between writes, not the entire product lifetime.

2.6. Read Disturb Errors

High V_{pass} on deselected WLs causes reverse SILC -- electrons tunneling from channel to FG. This phenomenon is Electric-field driven, so mostly causes $L0 \Rightarrow L1$. As with retention SILC, it worsens post-cycling because of the more defects are present in the tunnel oxide. As with retention, erasing and rewriting a block re-starts the clock.

The failure mechanisms discussed so far are 'analog' failures i.e. cell V_T shifts at a wrong level. Less common but more severe are defects, particularly shorts but sometimes opens. Shorts happen because insulators (dielectrics) break down. These shorts are due to

- Gate-oxide breakdown
- Interconnect-to-Interconnect shorting (as shown in Figure 6)

Interconnect shorts due to particles are the main source of failure for CPUs, so studied extensively. Same particles as the ones that cause yield fallout, only smaller or positioned so as not to cause immediate failure. Reliability failure rate is proportional to yield loss.

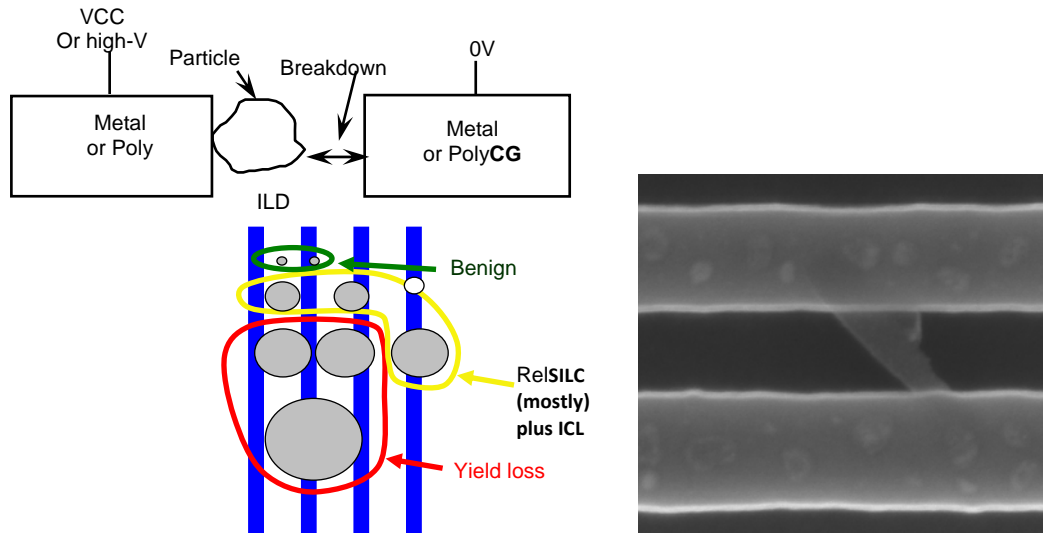


Figure 6. Oxide Breakdown and Interconnect to Interconnect Shorting

Shorts and opens can also be caused by corrosion of copper metallization. Topside silicon nitride passivation is supposed to keep the moisture out, but it fails when it is scratched or where the passivation is opened at bond pads. Large % of Ephraim field returns were traced to scratches. A number of PV OEM returns appear due to the bond pad issue. As with all defects, severity can range from single WL to total die fail. Amount of scratching can be improved but not eliminated totally.

3. Failure Analysis (FA)

Failure analysis [3-5] has eight basic steps. These steps are shown in Figure 7.

Step 1: Request Evaluation and Acceptance – Initial Investigation of Failure

A Failure analyst needs to know what the goal is for analyzing this failure. What is the background for the failure, meaning, where, when, and how it failed; why it failed based on the known information? What is the failure rate for this particular failure mode? Is it the first time to see such kind of failure? What are the hypotheses for root cause(s) and driving factors? Are the samples capable of answering the questions or are critical samples missing? Until the analyst has a clear picture on what needs to be done to accomplish the goal, and has enough background information prior to commencing the analysis.

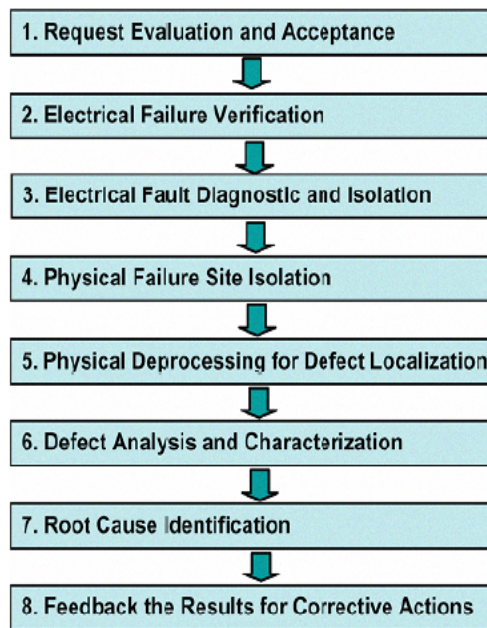


Figure 7. Failure Analysis Flow

Step 2: Electrical Failure Verification

During this step, electrical testing is performed to confirm if the failure can be detected under the outgoing production test program, internal quality assurance test program, or engineering evaluation test program. Each test program has a different guard-band for various test parameters, and can provide useful information on if the device failed marginally, or failed across all conditions, or even a test escape.

Step 3: Electrical Fault Diagnostic and Isolation

This is most difficult and time consuming step for FA work, and requires a lot of expertise from the analyst to understand the electrical phenomena, and in turn, to translate it into the physical phenomena. Some of these failures are shown in Figs. 8-11. To have more comprehensive understanding on electrical failures, some basic failure types, and typical causes for these failure types are listed in Table 1:

Table 1. Cause and Effect of Electrical Failures

<u>Typical Failure Types:</u>	<u>Typical causes for such failures include:</u>
<ul style="list-style-type: none"> o Parametric Hard Failures o Parametric Soft Failures o Functional Hard Failures o Functional Soft Failures o Recoverable Failures <p>Typical failure modes for the first four failure types include:</p> <ul style="list-style-type: none"> -Pin opens, shorts and leakage -High I_{CC1}, I_{CCSB} under different test modes -Pin to pin short -Incorrect logic input/output -Stuck-at fault -Speed and timing issues -Analog parameter drift -Memory array <ul style="list-style-type: none"> • Whole array or partial array • Particular sector or a group of sectors • Particular column(s) or row(s) 	<p>-Package related:</p> <ul style="list-style-type: none"> • Poor wire bonds, wire loops • Package cracking, die cracking • Package defects in molding compound • Damaged or corroded bond pads • Moisture trapping due to reliability stress tests • Improper laser marking damage • Package or die surface contamination • Damaged circuit due to sharp-edged fillers • Hairline die cracks or die surface scratches • Damaged or partially damaged package connections <p>-Device related:</p> <ul style="list-style-type: none"> • Electrical Static Discharge (ESD) • Electrical Over Stress (EOS) • Charge trapping due to minor EOS/ESD or hot carrier injection • Fabrication process error or random defect.

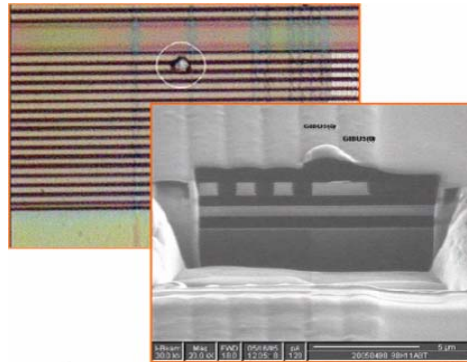


Figure 8. A random fab defect caused two adjacent metal lines

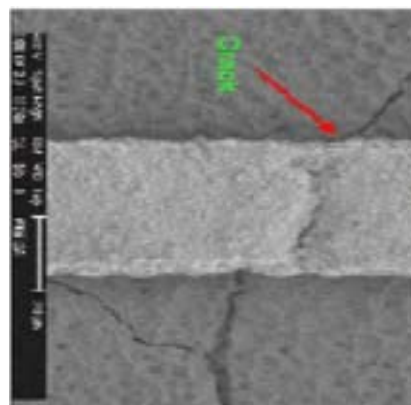


Figure 9. Optical and SEM photos showed some Cu trace

Step 4: Physical Failure Site Isolation

For physical failure site isolation, a two-step approach is recommended.

Non-destructive analysis step: In this step, following analysis are typically performed:

- Package level visual inspection
- Package wire-bond conditions analysis
- Package interface delamination analysis

Destructive analysis step: In this step, following analysis are typically performed:

- Package decapsulation for physical fault isolation
- Laser and FIB cuts for failure site isolation
- Delayering (deprocessing) for defect searching
- Mechanical cross-section through failure site

Physical fault isolation is carried out based on the electrical failure modes. If the failure mode indicates a possible package related failure, following tools and techniques can be used for fault isolation as presented in Table 2.

Table 2. Methods for Physical Failure Site Isolation

- Optical inspection
- Scanning Acoustic Microscopy (SAM)
- Real time, 3D X-ray inspection
- Time Domain Reflection (TDR) analysis
- Physical/mechanical probing
- Dye penetration analysis
- Decapsulation and visual inspection
- Mechanical cross-section



Figure 10. Real time X-ray showed a sagging

Step 5: Physical Deprocessing (or Defect Localization)

After electrical and physical fault isolation, a decision needs to be made on if the physical deprocessing is required. For failures that have similar failure modes and failure site as previous known failures, a signature analysis should always be considered to conclude the analysis results without going through the full physical deprocessing. Signature Analysis means that a new sample has the same set of failure modes, same environmental conditions as other devices that received a comprehensive failure analysis. By using signature analysis, it will help shorten the turn-around-time for analysis as well as avoid wasting FA resources on repeated failures. Suggested physical deprocessing methods (in chronological order) are presented in Table 3.

Table 3. Physical Deprocessing

- Chemical/Mechanical parallel lapping down to the level right above the failing layer
- Optical and SEM inspection at the suspected area
- Using binary search or passive voltage contrast (PVC)
- Perform FIB or TEM cross-section through the identified defective site for more details about the defects

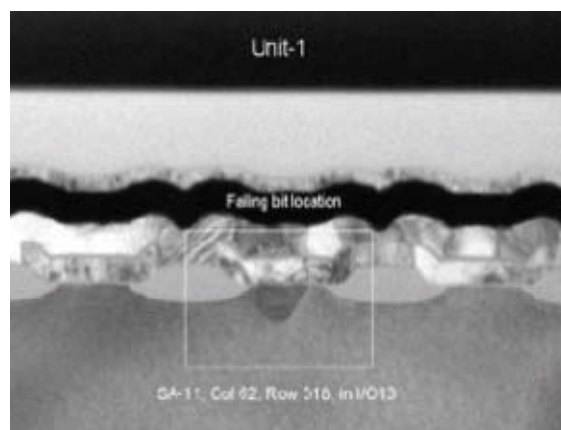


Figure 11. A Si defect was found under the failing cell with TEM cross-section analysis

Step 6: Defect Analysis and Characterization

Knowing the defect is just as important as finding the defect. Advanced technology has hundreds of process steps, and knowing which step that the defect was introduced will lead the

process team right to the core of the problem for correction actions. **TEM** is a daily failure analysis tool for defect examination and characterization.

Step 7: Root Cause Identification

Finding a physical defect provides a critical piece to the puzzle of what the true root cause is for the problem. Along with failure background evaluation, fabrication process history check and other critical information related to the failure, a root cause could be identified, then the corrective actions will be taken, and preventive actions shall be implemented.

Step 8: Feedback the Results for Corrective Actions

The FA process is a closed loop, providing information feedback for corrective actions is to stop the same kind of failures being submitted to the FA lab for analysis again.

4. Reliability Demonstration Testing (RDT) and Results

Reliability Testing was conducted on Enterprise drives. Enterprise drives have consistent performance and greater endurance with additional raw capacity. Enterprise drives require custom applications for specific needs and can be comprised of several SSDs. Joint Electron Device Engineering Council (JEDEC) Solid State Technology Association, a semiconductor trade and engineering standardization organization defines the JEDEC 218 and 219 standards for the SSD reliability tests. Table 4 shows the test conditions for the client and enterprise drives.

Table 4. Classification of Client and Enterprise Drives

Application Class	Workload	Active Use (power on)	Retention Use (power off)	Functional Failure Rqmt (FFR)	UBER
Client	Client	40°C 8 hrs/day	30°C 1 year	≤3%	≤10 ⁻¹⁵
Enterprise	Enterprise	55°C 24hrs/day	40°C 3 months	≤3%	≤10 ⁻¹⁶

Endurance RDT is used to check on the NAND capability of the drive. The test was carried out for High Endurance NAND. The drives were short stroke and only 49% of the actual drive area is used to analyze the complete NAND. This results are further used to extrapolate the full capacity of NAND. The well defined standards along with the SSDs of mixed density was used as sample size for the Endurance RDT. The tests started by first defining the flow, workload i.e amount of Terabytes that needs to be written on the SSD, followed by preping of the SSDs and final stage of debugging the failures if any and taking corrective actions.

The reliability parameters [7-9] under study for checking on the failures were:

Moving Read Reference (MRR): an error-avoidance or error-recovery scheme that moves the read trip points in response to shifts in distributions.

Raw Bit Error Rate (RBER): Probability of a bit being erroneous without use of any error correction techniques.

Defects per million (DPM): Attributed to a single failure mechanism (for a give component) without a corrective action plan in place to resolve defects.

The Endurance RDT was divided into 3 legs Read disturb at High and Room Temperature and No read disturb at High Temperature. The flow started by defining the density

and sample size and the block placement. The range for the blocks was provided by the NAND Component Team. The blocks were selected such that all the bad as well as good blocks were taken under consideration. The drives were low level formatted to delete the previously stored data and initialized using RDT.INT script. The drives were short stroke such that only 47% of the physical area was under test. A pre performance check was carried out on the drives and then the actual RDT workload was designed to write the Terabytes on the SSDs.

After the run of 1000hrs post performance was carried out and data matching was done. This formed the Power-on state for SSDs. The retention or Power-off check was done by placing the drives in oven at 40C for 3 months and bake readouts are collected. In the flow the same scripts were used except there was a change in the cycling on the drives.

A commercial tool was used to plot reliability parameters [12-13] as shown in Figures 12 and 13. As an example, Defects per million three different chip architectures are shown in Figure 12. at room temprature. Figure 13 shows MRR for same chip families at elevated temprature. It is noted that DPM for all architectures increase significantly at elevated (66 Deg. Celcius) temprature. Similar plots were generated and studied for MRR and RBER. These methods can be used for possibly extending the lifetime of SSD as discussed in reference [14] or can be used in conjunction with a multiparameter measurement system as discussed in reference [15].

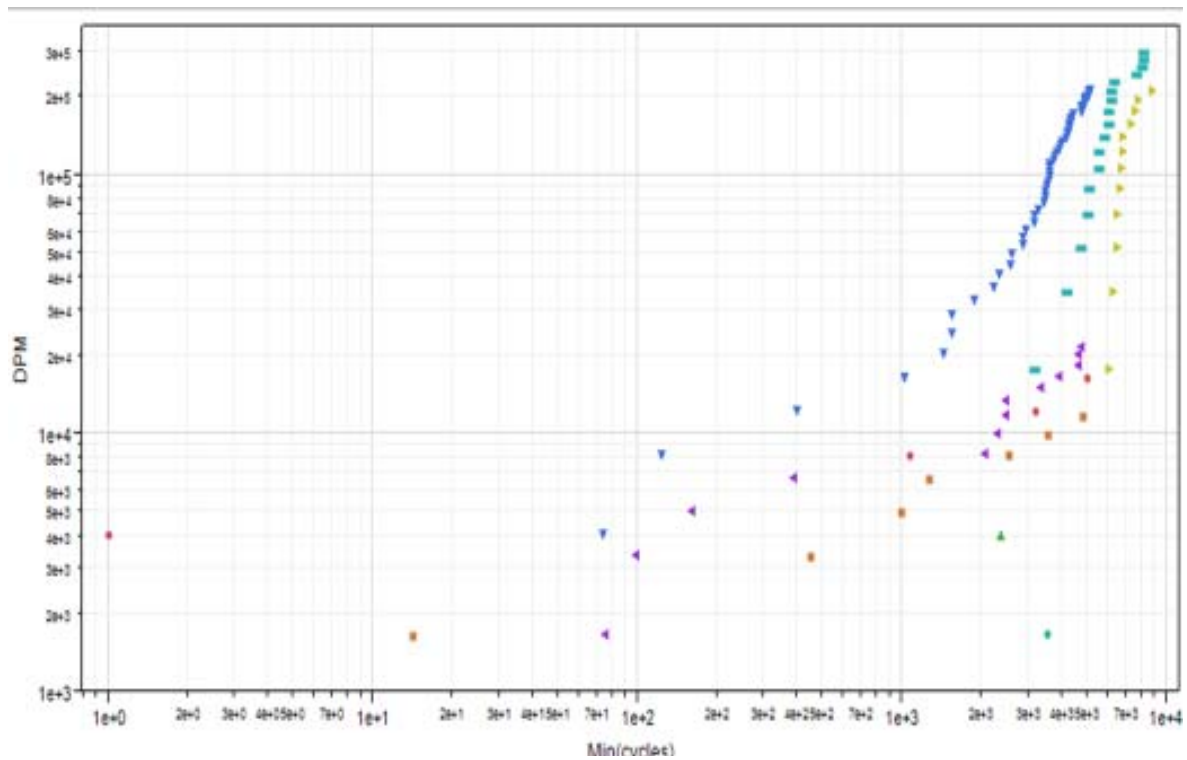


Figure 12. Defects per Million for 8 NAND architectures at room temperature

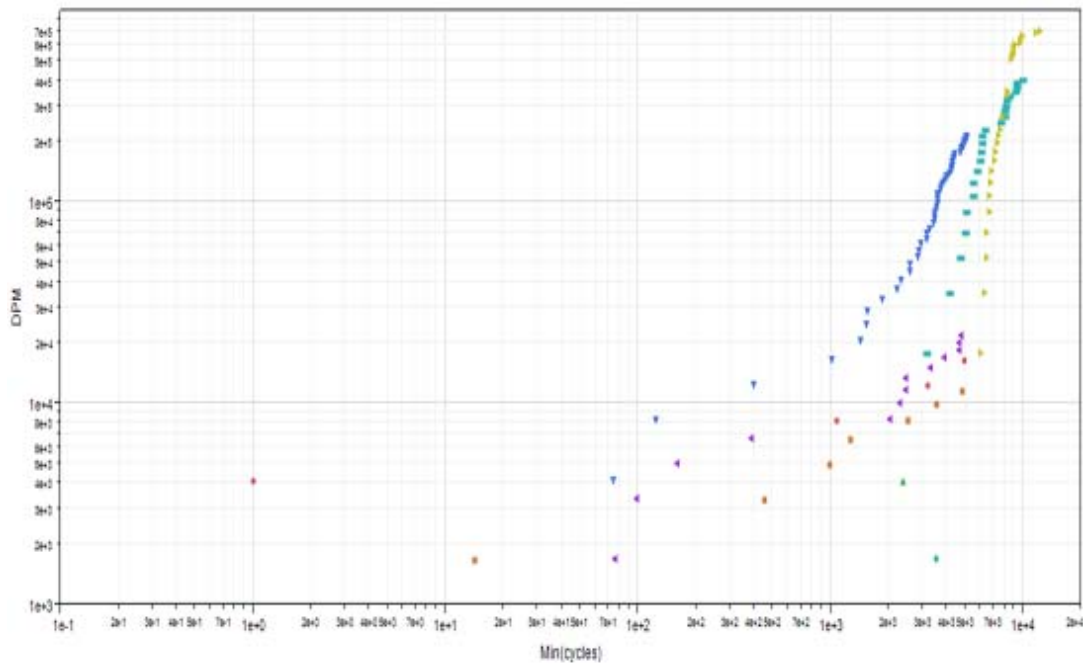


Figure 13. Defects per Million for 8 NAND architectures at elevated temperature

5. Conclusion

This study was focused on utilizing failure analysis and determination of reliability parameters for NAND by performing Endurance Reliability Demonstration Test. The failure mode reflected the program and erase failures affecting the reliability of NAND. Failure report files, the statistical analysis using commercial tools helped to get an insight on failures. Failure Analysis helped root cause the problem and provide corrective actions. The Failure Flow Analysis was used to determine the major cause of component failure. Statistical analysis was applied to the failure data to estimate the failure rate and the reliability of NAND flash drive cycled to 20K and 5K. Literature review provided insight into the use of the Scatter plot for Moving Read Reference (MRR), Raw Bit Error Rate (RBER) and Defects per Million (DPM) distribution as a commonly used methodology to calculate the reliability of a system. Reliability analysis showed increased DPM, MRR and RBER at elevated temperatures. The further analysis revealed that there were design issues due to which the circuitry was getting heated up. The reliability information can be used to establish preventive failure procedures in a cost effective way and continue to make improvements on the Endurance testing by using page wise short stroke so that with every block even the pages in failure can be easily determined.

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