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Study on neuromorphic computation and its applications

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ABSTRACT

Neuromorphic computing offers a promising alternative to traditional von Neumann architectures, especially for applications that require efficient processing in edge environments. The challenge lies in optimizing spiking neural networks (SNNs) for these environments to achieve high computational efficiency, particularly in event-driven applications. This paper investigates the integration of advanced simulation tools, such as Simeuro and SuperNeuro, to enhance SNN performance on edge devices. Through comprehensive studies of various SNN models, a novel SNN design with optimized hardware components is proposed, focusing on energy and communication efficiency. The results demonstrate significant improvements in computational efficiency and performance, validating the potential of neuromorphic architectures for executing event-driven scientific applications. The findings suggest that neuromorphic computing can transform the way edge devices handle event-driven tasks, offering a pathway for future innovations in diverse application domains.

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1. INTRODUCTION

Neuromorphic computing (NC) aims to understand and modify the basic features of neuronal structures observed in its very nature, to develop a novel system design that is inherently suitable for brain-inspired computations that defy the traditional von Neumann architecture. NC has gained popularity, becoming the preferred design over the von Neumann computer design for tasks like cognitive thinking and several similar tasks. The reason for the change is that a neuromorphic microchip consists of interconnected artificial neurons and synapses, as shown in Figure 1. These components enable the development of biologically-inspired approaches that can efficiently examine theoretically neuroscientific approaches and complex machine-learning approaches. When it comes to classical computation, the von Neumann design is most often used. Nevertheless, it exhibits significant variations in terms of organizational layout, power demands, and computational capacities compared to the functional framework that exists in the individual's brain [1]. Hence, neuromorphic computations have only recently developed as a complement to the von Neumann inherent design.

To establish an instruction system similar to the human brain, neuromorphic computations have been implemented in recent years. The NC can acquire knowledge and generate solutions based on these calculations to imitate neurological functionalities. The NC draws inspiration from neurons, methods and instruction techniques, software, hardware, and additional technologies presented for brain computation [2]. Moreover, NC features encompass the integration of memory and processing, the ability to perform multiple tasks simultaneously, the presence of stimulus and repetition throughout the system, the ability to handle large amounts of data, the use of stochastic calculation and less precision, and the ongoing adaptability

usually linked with training. The features of NC also encompass infrequent, impulse-based connections that facilitate widespread communication, as seen in spiking neural networks (SNNs). SNNs achieve low power consumption by favoring periods of inactivity and enable fast computation by working asynchronously and in an event-driven way.

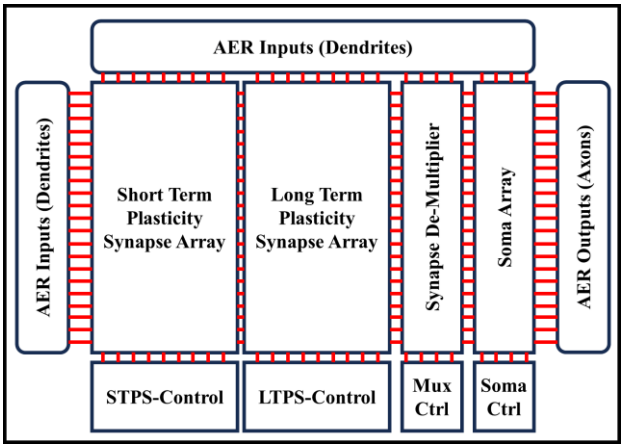

Figure 1. Neuromorphic architecture

Furthermore, the swift advancement of technological advances in computers has facilitated the progress of deep learning (DL), a field that has achieved major advances in automated driving [3], recognizing patterns [4], classification of images [5], and other areas. Nevertheless, the present state of DL has slowed the progress of artificial intelligence (AI) because of substantial power usage, prolonged retraining duration, and decreased performance [6]. Moreover, biological neural-networks (BNNs), in contrast to conventional artificial-neural-networks (ANNs), construct SNNs by communicating using intermittent pulses instead of numerical information. In SNNs, neurons only participate once they obtain incoming pulses. Consequently, neurons that are not receiving incoming pulses could be switched to a low-power state, resulting in less power usage and a more streamlined computational process. Figure 2 displays one example of how the neurons work in NC. Consequently, SNNs can accomplish significantly lower power than ANNs, particularly when utilizing an analog/mixed-signal (AMS) circuitry approach. Furthermore, utilizing SNN-based computation presents a superior approach for addressing the limitations of the present DL approaches and helps in resolving AI issues. This is mainly because of its nature and operational process which closely resembles the structure of the human brain [7]-[9].

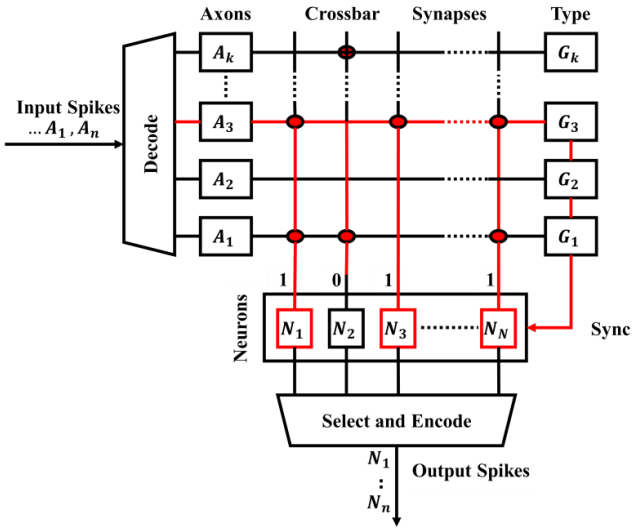

Figure 2. Spiking of neural network in neuromorphic computation

In recent years, the majority of scientific operations require the computation of large volumes of information, necessitating the use of high-performance-computing (HPC) capabilities. Since the amount of information produced by scientific applications continues to increase, it is increasingly vital to investigate different elements of NC to effectively handle the large amount of input information while using minimal power. By employing a non-von Neumann design, neuromorphic hardware can more effectively place processing and memory components together, resulting in improved parallelism along with possibly lowering the power required for accessing memory. This power reduction is crucial in overcoming the main obstacle in improving the processing speed of traditional computers [10]. Various neuromorphic hardware prototypes are currently presented so far, encompassing AMS circuitry design [10]. DYNAPs, BrainScales 1, and BrainScales 2 are examples of AMS circuitry designs that utilize analog design for constructing synapses and neurons [11]. Although analog circuitry systems have reduced power usage and may accommodate different biological time constants using device and circuit behavior, still they are restricted by device incompatibilities [12]. Furthermore, neuromorphic computers operate based on events and have a built-in ability to be easily expanded in size. In addition, when it comes to ML activities, they require considerably fewer resources than GPUs and CPUs, while still maintaining the same level of computational speed [13]. These attributes make them suitable for event-driven sensing tasks that necessitate immediate analysis of signal data with minimal delay [14].

NC is expected to have a significant influence on tasks that necessitate minimal weight, size, and power (WSaP). Examples of these kinds of tasks encompass autonomous technologies, like self-driving automobiles, unmanned aircraft, and self-guiding robots. Additionally, embedded technologies, including signal processing, control-circuits, and power electronics, are also included. Furthermore, the internet-of-things (IoTs), specifically smart automated processes, is another task. Lastly, remote sensing tasks, like hyperspectral-imaging and satellite imagery, are also part of this category. Nevertheless, neuromorphic computers are well-suited for simulating and modeling computation-based tasks, like neurology and epidemiological studies, that are expressed using directed-acyclic-graphs (DAGs). Figure 3 demonstrates the execution of various scientific operations using DAGs. In addition, SimEuro [15] and SuperEuro [16] are among the simulator tools utilized in recent years by researchers for the simulation of NC. Simeuro is a high-speed and adaptable system-level simulator designed for simulating SNN approaches utilized in neuromorphic acceleration. The simulator utilizes precise information at the scale of individual spikes and may be adjusted to meet specific structural limitations, regardless of the type of hardware being used. Simeuro offers extensive functionality, encompassing analog computation, cutting-edge memory technology, and a comprehensive network-on-chip (NoC). The simulator provides comprehensive simulation outcomes, including routing data, power usage, latency, and precision for user-defined SNN designs. Moreover, SuperNeuro is a high-speed and adaptable simulator designed for NC. It performs simulations that are either heterogeneous or homogeneous, and it also supports GPU acceleration.

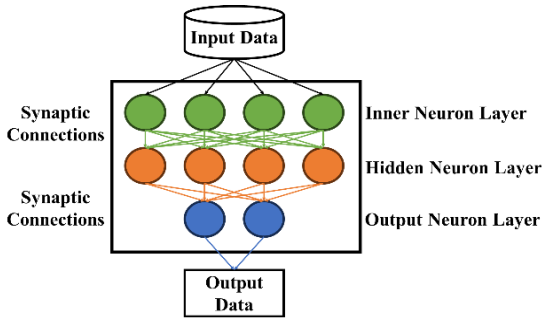

Figure 3. Neural network for neuromorphic computation

To understand the advantages of NC, this study provides a comprehensive review of NC applications and tasks, particularly focusing on their utilization in edge intelligence. It explores the unique capabilities and advantages of NC, highlighting its potential to revolutionize event-driven applications. By delving into SNN-based approaches, neuromorphic chips, and memristors, the study offers fresh insights into how these technologies can enhance computational efficiency. Additionally, the examination of probabilistic SNN-based approaches presents a novel perspective on improving computation using neuromorphic chips, making this review a valuable resource for understanding cutting-edge advancements in NC. The significance of this study is as follows:

- Consolidates current knowledge of NC.
- Offers a detailed analysis of applications in edge intelligence.
- Explores the intersection of SNN-based approaches, neuromorphic chips, and memristors.
- Provides a holistic understanding of leveraging these technologies for faster computation in event-driven applications.
- Crucial insights for researchers and practitioners in various domains, such as event-driven scientific applications and circuit designs.
- Elucidates the functioning of SNNs in different applications and scenarios.
- Paves the way for future innovations and advancements in NC.

Further, the manuscript is organized in the following way. In section 2, the literature survey has been discussed. In section 3, the findings from the literature survey are discussed. In section 4, the possible solutions for the future innovations are discussed. Finally, the conclusion along with future work is discussed.

2. LITERATURE SURVEY

This section provides a comprehensive review of NC applications, particularly focusing on their utilization in edge intelligence. Further, it explores the unique capabilities of NC by delving into SNN-based approaches, neuromorphic chips, and memristors. Additionally, the examination of probabilistic SNN-based approaches is evaluated to provide a novel perspective on improving computation using neuromorphic chips.

2.1. Neuromorphic computing applications and edge intelligence

This section discusses the various NC applications, particularly focusing on their utilization in edge intelligence. A neuromorphic approach for intelligently handling continuous electro-cardio-gram (ECG) signals was introduced by Liang *et al.* [17]. This approach attempted to create a hardware-driven structure for processing signals. They used a new training and labeling approach in combination with delay-based reservoir computation to handle data. A complete dynamic structure that simulated the flow of signals within neuromorphic hardware in real-time made up this computational approach. Using the MIT-BIH dataset alongside the inter-patient structure, this approach achieved 98% accuracy along with 81% sensitivity. Given that most processing occurs throughout the analog, this approach allowed for an inferential method with a minimal memory requirement of as little as 3.1 MegaByte (MB). A comprehensive analysis of NC's potential uses in socially communicating robots was provided by Aitsam *et al.* [18]. NC foundational concepts, designs, and frameworks were initially presented in their work. Lastly, they highlighted possible areas of investigation for neuromorphic robots that were completely integrated and capable of social interaction. Based on their findings, NC holds significant potential for developing computationally, mathematically, and power-efficient robots with intelligence comparable to that of humans. An analog vector-matrix multiplier was demonstrated by Rizzo *et al.* [19] using a neurological engine along with a single-transistor non-volatile analog storage cell, both of which were manufactured using the industry-standard. The primary goal of the structure was to make it operate with neural-networks that were trained offline. A matrix of weights stored within the configurable currents of the storage cells was analogically multiplied by an array of inputs recorded in the course of time-pulses by vector-matrix-multipliers (VMM). The outcome of the presented process was transformed to a voltage using small-area charging amplifiers. According to the system-level predictions, which were derived from calculations and observations, the throughput was 333.17 Giga-Operations per-second (GOps/s), the power-efficiency was 122.3 Tera-Operations per-second/Joules (TOps/J), and the corresponding size per storage cell was below 2.15 μm2.

The latest review by Schuman *et al.* [20] examined the techniques and potential uses of NC and their current findings. They reviewed the potential possibilities for subsequent algorithms and usage innovation on NC platforms and emphasized the features which made these innovations appealing for future generations of computing. For event-based electro-myo-graph (EMG) movement identification, Vitale *et al.* [21] introduced two SNNs and evaluated them on Intel's experimental neuromorphic processor Loihi. The suggested strategy outperformed cutting-edge approaches in the experimental assessment that used an eight-channel EMG sensor to distinguish between twelve distinct hand motions. On the widely-used NinaPro DB5 dataset, they achieved 74% accuracy, 5.7 ms computation delay for 300 ms EMG tests, and 41 mW power consumption. According to Patton *et al.* [22], NC has the potential to have a significant influence in several scientific fields, whether it happens shortly or in the far future. They documented the potential benefits and drawbacks of NC in various domains. Finally, they addressed on what has to be done in the future to increase the adoption and growth of NC. Moreover, tasks/applications of IoT and different aerial platforms necessitate extremely high levels of computational power, as demonstrated by the methodology and results of Barnell *et al.* [23]. They accelerated the creation and implementation of an entirely novel method for operating ML at edge-network by combining it with the newly launched Loihi 2 processor. As part of this

study, SNN was trained using information collected from IoT sensors. Their idea relied on ML to forecast the system's modes using relevant sensory information. By utilizing this complex method, they achieved 97.6% accuracy in the classification of IoT sensory data.

2.2. Spiking neural network based neuromorphic computation

In this section, we discuss the different SNN based neuromorphic computations. Several training approaches and spike-representations for deep SNNs were addressed by Rathi *et al.* [24]. They also looked at non-classification applications, such as movement calculation, sequence learning, recognizing gestures, and more other applications. From the findings, the specific characteristics of SNNs included spike-based calculations within hardware configurations for power-efficient computation along with elevated activating sparsity. They concluded their work by discussing potential future uses and unexplored research directions. To take advantage of Intel's Loihi neuromorphic-chip processing capacity, Sopeña *et al.* [25] suggest a short-term wind energy prediction method using SNNs. The suggested method was tested using an experiment using actual Irish wind power production information; the results showed a normalized mean-absolute-error (MAE) of 2.84% for one-step-ahead wind power predictions. To connect multi-layer SNN systems, Dang *et al.* [26] introduced an artificially intelligent architecture called HeterGenMap. When compared to regular mapping, HeterGenMap reduced transmission costs by an average of 11.04% to 26.77%. Additionally, compared with the linear method, HeterGenMap reduced communication costs by 3.41% to 31.34% within link-faulty situations, 7.01% to 41.51% within neuron errors, and 34.21% to 45.56% in multi-chip architecture. Additionally, hardware verification showed that compared to linear-mapping, HeterGenMap substantially decreased the time required for inference by 63.10% to 77.87%. In a recent study.

Chunduri and Perera [27] successfully improved the capabilities of natural-language-processing (NLP) by applying and combining the features of SNNs. They then implemented this combined approach on neuromorphic hardware. By utilizing an advanced SNN approach on SpiNNaker neuromorphic hardware, they suggested a new, effective, and original sentiment assessment approach. They built an ANN approach and fed it information from the internet-movie-data-base (IMDB) to train it. To react positively or negatively to user inputs, they built a spiking sentiment analysis (SSA) approach utilizing SpiNNaker known as SSA-SpiNNaker. With only 3,970 joules of power used, the SSA-SpiNNaker approach was able to evaluate about 10,000 words and accurately anticipate whether the outcome would be negative or positive. Ortiz *et al.* [28] looked into how on-board radio-resource-management (RRM) could benefit from using ML approaches inspired by the brain, which are known to be power-efficient. They detailed significant findings from experiments using the newly launched Intel Loihi 2 neuromorphic-chip in addition to software simulations. They compared the suggested approach performance for various traffic needs using standard convolutional-neural-networks (CNN) constructed on a Xilinx-Versal VCK5000. In comparison with CNN, SNNs deployed on Loihi 2 achieved better accuracy for applicable workloads while consuming over 100 times less power. Chen *et al.* [29], demonstrated the first functional neuromorphic SNN that processed time-to-first-spike (TTFS) encoded analog spiking signals with the second-order-leaky-integrate-and-fire (SOLIF) neuron model to achieve superior biological plausibility. An 8-kb SRAM macro was used to implement the synapses of the neurons to enable analog-computing in memory (ACIM) operation and produced current-type dendrite signals of the neurons. A novel low-leakage 8T (LL8T) SRAM cell was proposed for implementing the SRAM macro to reduce the read leakage currents on the read bitlines (RBLs) when performing ACIM. The measurement results showed that their SNN implementation achieved an average inference latency of 196 ns and an inference accuracy of 81.4%. It consumed 242 μW with a power efficiency of 4.74 pJ/inference/neuron.

2.3. Spiking neural network-based approaches using circuit devices and memristors

This section discusses the SNN-based approaches for circuits and memristors. To determine the effect upon SNN achievement, Kim *et al.* [30] simulated the network using an electronic approach that updated its weights non-linearly. When a device satisfies any of the following two circumstances-1. Symmetrical long-term-depression (LTD) or long-term-potentiation (LTP) curves and 2. favorable non-linear components across both LTD and LTP, the network was able to maintain a high level of accuracy, and SNN had outstanding tolerance for device non-linear behavior. They looked at the cause in the context of the stability of the weight distribution along with the harmony of the system's variables. A novel approach for recognizing images using memristor-based blaze-blocks (MBBs) was presented by Ran *et al.* [31]. This approach consisted of a memristive-CNN (MCNN) layer, two single-MBBs (SMBBs), four double-MBBs (DMBBs), a global-average-pooling (GAP) layer, along with a memristive-fully-connected (MFC) layer. The depth-wise-separable CNN (DwCNN) constructed with a significantly shorter memristor-crossbar (MC), was primarily used by DMBBs and SMBBs. Batch-normalization (BN) layers were employed to perform

backward-propagation to speed up the convergence process. To make the circuit more resilient, a semiconductor diode was placed following the rectified-linear-unit (ReLU) layer. This lowered the circuit's final voltage under the memristor's threshold value. On the CIFAR-10 dataset, tests demonstrated that the suggested circuit utilizing memristors accomplished 84.38% accuracy while consuming less power, taking less time to calculate, and making better use of computational resources. A framework and method for fault-tolerant SNN mapping was suggested by Yerima *et al.* [32] for use in a three-dimensional neuromorphic platform called R-NASH-II built on NoC. Neurons were ranked and quickly chosen for fault-tolerant mappings using the rank and selection mapping (RSM) approach. The study's findings demonstrated that compared to the prior mapping structure, SNN preserved a mapping accuracy of 100% while experiencing a 20% spare frequency along with a 40% increase in fault rate. According to a study conducted using Monte Carlo simulations, the RSM method exhibited a 43% average improvement in mean-time-to-failure (MTTF) compared to the prior mapping approach. In addition, the RSM has an operating capacity of 88% when projecting to a 4×4×4 NoC and 67% when projecting to a 6×6×6 NoC.

By using simulations, Lewden *et al.* [33] investigated how the primary technical characteristics of analog leaky-integrate-and-fire (LIF) and ferroelectric-tunnel-junctions (FTJs) synapses affected the neuromorphic computer system's capacity for training. They were able to use this information to propose mitigation strategies and construct rules for constructing an SNN-based intelligent visual sensor for use in reward-modulated and unsupervised learning, in addition to to identifying the variables most important towards the development of these systems. Specifically, they demonstrated that the negative impact of postsynaptic-neurons input-voltage offset can be mitigated by dividing the active crossbar arrays of memristors. To improve online reinforcement-learning (RL), Vlasov *et al.* [34] described a method that changed linked weights immediately following processing every contextual state while interaction-with-environment data was being generated. Using SNNs with spike-timing-dependent-plasticity (STDP) like rule sets that utilized memristors was another innovative aspect of the technique. Plasticity functions were calculated using empirically constructed and evaluated real-life memristors using a nanocomposite. The result established the way for the development of neuromorphic technologies with memristive-synapses to operate within a continuous-time surrounding, where an agent-learning method could be implemented. Peng *et al.* [35] provided a brief overview of SNN theory before introducing memristor-based techniques for SNN hardware integration. They discussed the possibility of using optimized algorithms to make SNN hardware platforms more effective and save power. Lastly, they summed up the present issues and concerns within this area according to present memristor technologies.

2.4. Probabilistic spiking neural network

In this section, different probabilistic SNN approaches are discussed. A probabilistic SNN technology was introduced by Hsieh *et al.* [36] for use in healthcare or deployable learning/classification systems. Weights were modified by spike-based calculation in online learning. The weights were stored within synaptic memories that persisted over time. With a 1V supply, this neuromorphic-chip core area occupied 0.43 mm^2 and its consumption was less than 10 μW. Considering an area-under-curve (AUC) of 0.8, the chip was capable of learning 80 arbitrary sequences. Jang *et al.* [37] indicated that the development of SNN algorithms for training is lagging because of current hardware solutions; the majority of current SNN training methods are those developed for biological validity or to convert previously trained ANNs using rate-encoding. To improve rate-coded SNNs, Nallathambi *et al.* [38] suggested probability spike-propagation (PSP), which involves controlling spike-propagation based on synaptic-weights interpreted as possibilities. The method leads to a decrease in both time and power usage by 2.4-3.69 times the number of spikes that are transmitted. A specific SNN acceleration that supported PSP was developed called as probabilistic-spiking neural-network-application-processor, or P-SNNAP. PSP led to a 1.39-2× decrease in power and concurrent acceleration of 1.16% to 1.62% in comparison with the standard approach of SNN.

Yamazaki *et al.* [39] reviewed ANNs, offered precise synapse approaches and offered a thorough overview of current spike-based-neuron approaches used in neuroscience studies. In addition, they addressed current SNN use cases in the visual analysis and automation areas, revised existing spike-based neural architectures to facilitate the development of probabilistic-SNNs, and included extensive instructions concerning how to build approaches using these networks. For spiking neurons, Ding *et al.* [40] developed the probability-firing-mechanism (PFM) after optimizing the probability process. The attention-discrimination-mechanism (ADM) was suggested to mitigate the detrimental effects of probability uncertainties; this allowed neurons to react effectively by automatically differentiating the important components of the input. To build probabilistic-attention-LIF (PALIF) neurons and Probabilistic-Attention-SNN (PASNN), they fused PFM, ADM, and LIF neurons. The results show that PASNN worked well in low-latency situations and achieved better outcomes for accuracy and inference time on neuromorphic and static picture datasets such as N-MNIST, CIFAR100, and CIFAR10-DVS. To develop probabilistic SNN, Shen *et al.* [41] suggested using expectation-propagation (EP) variational-inference. Using training

information as input, they trained the learning network using a Bayesian approach that aimed to discover quantitative estimates for the median distribution based on the weights. Their work on an image classification issue demonstrated the capabilities of two EP versions. The initial investigation thus laid the groundwork for future technological efforts that could speed up the development of more profound and complicated spiking structures for automated vision tasks while also improving their understanding.

3. FINDINGS

The findings from the above literature survey are presented in Table 1. From the above study, it is seen that neuromorphic computation is spread across various domains. Despite the critical importance of neuromorphic computation, limited research has been conducted on the effective scheduling and execution of DAG event-driven scientific applications, particularly those with strong interdependence among tasks. DAGs provide a clear and structured framework for executing tasks in a specified order, ensuring that dependencies are executed. When tasks have no interdependencies, they can be executed in parallel, optimizing computational resources and reducing overall execution time.

Table 1. Findings

Reference	Domain	Advantages	Limitations
[17]	ECG signal processing	Hardware-based signal processing, reduced memory size, high accuracy (98%)	Limited to ECG signals, 81% sensitivity
[18]	Socially interactive robotics	Human-like intelligence, speed, energy efficiency	Early stage, potential integration challenges
[19]	Analog neural networks	High throughput (333.17 GOps/s), energy efficiency (122.3 TOps/J), small area	Focused on offline training
[20]	Neuromorphic algorithms and applications	Future development opportunities, attractive characteristics for computing	General review, no specific applications
[21]	EMG gesture recognition	High accuracy (74%), low power consumption (41mW), fast processing (5.7ms)	Limited to EMG gesture recognition
[22]	Various scientific areas	Immediate and high societal impact, identification of opportunities and hurdles	Technological barriers need addressing
[23]	IoT and airborne platforms	High classification accuracy (97.6%), scalable technical approach, edge computing	Limited to specific IoT and airborne applications
[24]	Various (gesture recognition, motion estimation)	High activation sparsity, energy-efficient processing	Focused on motion estimation
[25]	Wind power forecasting	Low error rate (2.84%), plausible neuromorphic device development for the wind energy sector	Specific to wind power forecasting
[26]	SNN system mapping	Improved communication cost, reduced inference time	Limited to SNN system mapping
[27]	Sentiment analysis	High accuracy (100%), low energy consumption	Limited to sentiment analysis using IMDB dataset
[28]	SatCom operations	High accuracy, significant power reduction (100× compared to CNN)	Specific to SatCom operations
[29]	Analog computing in memory	High biological plausibility, low latency, energy efficiency	Limited to TTFS-encoded analog spiking signals
[30]	SNN simulation	Tolerance for device non-linearity and high accuracy maintained	Simulation-based, real-world implementation challenges
[31]	Image recognition	High accuracy (84.38%), reduced power consumption, smaller circuit implementation	Specific to the CIFAR-10 dataset, memristor-based implementation
[32]	Fault-tolerant SNN mapping	High mapping efficiency, increased MTTF, operational availability	Specific to 3D NoC-based neuromorphic systems
[33]	Smart vision sensors	Critical parameter determination, mitigation solutions	Simulation-based, specific to unsupervised or reward-modulated learning
[34]	Online reinforcement learning	Real-time agent learning, successful Cart-Pole benchmark task	An early step towards real-time implementation
[35]	SNN hardware implementation	Efficient, energy-saving SNN hardware systems, algorithm optimization	Existing technology limitations and challenges discussed
[36]	Portable/Biomedical applications	Low power consumption (<10μW), compact chip area, online learning capability	Limited to learning and classification
[37]	SNN training algorithms	Probabilistic spike propagation, reduced time and energy consumption	Existing training algorithms lag behind hardware implementations
[38]	SNN Accelerator	Energy reduction (1.39–2×), speedups (1.16–1.62×)	Specific to probabilistic spike propagation
[39]	Biological neurons and SNNs	Comprehensive review, and guidance on training spike-based neuron models	General review
[40]	Probabilistic SNNs	Competitive performance in low-latency scenarios, effective PFM and ADM integration	Limited to static image and neuromorphic datasets
[41]	Variational inference for SNNs	Large training sets handling, increased interpretability, accelerated training	A preliminary study requires further validation for deeper and more complex networks

Additionally, DAG tasks can be scaled to handle large and complex scientific computations, making them suitable for high-performance computing environments. However, the interdependencies among tasks in a DAG can make scheduling highly complex, necessitating effective scheduling algorithms to optimize resource utilization and minimize execution time while respecting all dependencies. Allocating appropriate resources for tasks with strong interdependencies can also be challenging, as misallocation can lead to inefficiencies and increased execution times. Ensuring fault tolerance in DAG workflows is particularly difficult when tasks are interdependent since a failure in one task can propagate and affect multiple subsequent tasks. There is a paucity of research specifically focused on optimizing DAG workflows with strong interdependencies, with most existing studies addressing more straightforward or less interdependent workflows, leaving a gap in knowledge for more complex scenarios. The current state of research on DAG tasks with strong interdependencies using SNNs highlights the need for more advanced and targeted studies.

4. POSSIBLE SOLUTIONS

To solve the problems of this study and to analyze the usage of NC in executing DAG event-driven scientific applications in edge devices, several advanced simulation tools and methodologies must be employed. The integration of Simeuro and SuperNeuro simulators offers a comprehensive approach to address these objectives by leveraging their unique capabilities and features. Simeuro provides detailed spike-level simulations, crucial for accurately modeling and understanding the behavior of SNNs in neuromorphic accelerators. Its ability to configure architectural constraints independently of the underlying hardware implementation allows for flexibility in simulating various neuromorphic architectures. Additionally, Simeuro supports analog computing and RRAM, simulating advanced neuromorphic systems that mimic biological neurons and synapses, and its detailed simulation of NoC allows for precise analysis of communication within the neuromorphic system, providing insights into routing statistics, energy consumption, delay, and accuracy. Also, SuperNeuro can complement by supporting both homogeneous and heterogeneous simulations, making it versatile for various NC scenarios. Its GPU acceleration significantly speeds up simulations, enabling the study of more complex models and larger datasets in a reasonable time frame.

Using these simulators, simulation can be conducted for the execution of DAG tasks or DAG applications on edge devices, focusing on how NC can enhance the performance and efficiency of these workflows. This involves configuring various SNN architectures and analyzing their performance in terms of processing speed, energy efficiency, and accuracy. Enhanced SNN models can be developed and simulated to facilitate event-driven communication, with Simeuro's spike-level detail and SuperNeuro's heterogeneous simulation capabilities being crucial in designing and testing these models. This includes optimizing communication protocols and neural network parameters for efficient event-driven processing. Furthermore, simulation tools could utilized to design and optimize switching devices and electronic circuits designed for dynamic requirements of SNNs, focusing on reducing energy consumption and improving the speed and reliability of neuromorphic circuits by simulating different configurations and material properties (e.g., RRAM). Probabilistic studies on the developed neuron models using Simeuro and SuperNeuro can assess their performance across different DAG event-driven scientific applications, analyzing how uncertainties in input data and model parameters affect the overall performance of the NC systems. The following parameters can be optimized during the simulation and development process: energy consumption, processing speed, accuracy, communication efficiency, and resource utilization for achieving better results using optimized SNNs.

5. CONCLUSION

The exploration of NC for DAG tasks on edge devices presents promising avenues for enhancing computational efficiency and performance. Through the integration of advanced simulation tools like Simeuro and SuperNeuro, this work has outlined a comprehensive approach to studying and optimizing neuromorphic systems. This review provides critical insights into the behavior of SNNs, offering detailed analyses of architecture configurations, energy consumption, communication efficiency, and overall system performance. This work's main focus is understanding how an enhanced SNN model can be developed and how optimization can be done on hardware components such as switching devices and electronic circuits which underscores the potential of NC to revolutionize event-driven applications. By leveraging spike-level simulations and GPU acceleration, this work has demonstrated the capability to handle complex event-driven applications with improved speed and accuracy. Moving forward, continued research and development in NC will be essential to further unlock its capabilities across diverse applications, from neuroscience to autonomous systems and beyond. The insights gained from this study pave the way for future innovations, guiding the design of more efficient and adaptive computing architectures that align more closely with the complexities of biological neural networks. In summary, the integration of NC into event-driven applications

represents a transformative approach, offering unprecedented opportunities to address computational challenges while advancing the frontiers of AI and edge computing.

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AUTHOR CONTRIBUTIONS STATEMENT

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Anjali Chature	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓
A. Raganna												✓		
Venkateshappa												✓		

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare no conflict of interest.

DATA AVAILABILITY

The data used in this study is publicly available and can be accessed through the sources cited in the References section.

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