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Design and simulation of a double boost switched capacitor multilevel inverter

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ABSTRACT

This article presents an innovative boost inverter configuration that produces a nine-level double voltage augmentation waveform. A significant drawback of conventional multilevel inverters (MLIs) lies in their dependence on conversion for elevating the voltage, particularly applied in conjunction with renewable energy sources. The proposed methodology, characterized by its double voltage boosting capacity, mitigates this challenge by automatically enhancing the input voltage. Switched-capacitor multilevel inverters (SC-MLIs) represent a prevalent category within the realm of MLIs. This paper presents a double boost switched capacitor inverter (DB-SCI) designed to address critical issues involving the increased use of semiconductor switches, DC sources, and capacitors. The proposed DB-SCI achieves a nine-level resultant voltage utilizing a single DC source, 8 switches, and 3 capacitors. It can amplify the output voltage with a gain of two. Moreover, the DB-SCI employs a level-shifted pulse width modulation (PWM) approach to augment the resultant voltage and enhance the output voltage's quality. The article assesses the effectiveness and feasibility of the DB-SCI under various modulation indices using MATLAB/Simulink. The comparison study of MLI topologies is presented.

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1. INTRODUCTION

Ensuring access to electrical energy in rural areas is crucial for enhancing sustainable living standards. A top priority in numerous developing countries is electromagnetic compatibility [1] when evaluating factors such as site suitability, power conversion methods, installation, maintenance expenses and complexities. Compared with wind farms, grid-connected solar photovoltaic systems (PVS) have emerged as a more favorable option [2]. To assess the system's efficacy across diverse operating conditions, this section conducts a thorough examination of grid-connected PVs. Additionally, it outlines the design of the voltage source control unit, which encompasses fuzzy rules for the current regulator [3]. Distributed renewable energy generation systems are extensively utilized to achieve net-zero carbon emissions, primarily because of their heightened reliability, diminished environmental impact, economical cost-effectiveness, and adaptable system nature [4], [5]. The schematic representation in Figure 1 illustrates the decentralized renewable

energy production system, with inverters serving as crucial components for power conversion and transmission. MLIs find widespread application across various domains, such as electric vehicles (EVs), renewable energy systems (RESs), and flexible AC transmission systems. Compared with traditional two-level inverters, MLIs offer numerous advantages, such as minimal total harmonic distortion (THD), a decreased voltage rate of change on switches, and a reduced switching frequency [6], [7]. Typically, traditional MLIs are categorized as neutral-point clamped (NPC) inverters, flying-capacitor (FC) inverters and cascaded H-bridge (CHB) inverters. Nevertheless, NPC multilevel inverters (MLIs) face challenges related to capacitor voltage imbalances, which are similar to those encountered in FC MLIs, which rely on multiple capacitors to achieve suitable output levels [8]. CHB inverters, on the other hand, can produce more levels through the utilization of multiple H-bridge cells. Nonetheless, the necessity for numerous isolated DC sources restricts their applicability. Given the rapid progression in the power sector, it is imperative to explore novel MLIs with reduced components, increased output voltage levels and enhanced conversion efficacy [9]–[11]. In recent years, the integration of switched capacitor (SC) technology with MLIs has been adopted to minimize the device count and streamline control mechanisms [12]–[16]. SC, characterized by its nonmagnetic structure comprising switching devices and capacitors, has advantages such as compact size and elevated power density. Moreover, owing to the inherent boosting capability of the SC structure, it can establish a direct connection between the DC input and the AC output, thereby mitigating the necessity for excessively high duty ratios in DC links and enhancing inverter efficiency. A five-level SC inverter was proposed in [17], which is capable of generating a multilevel voltage from a DC source and facilitating a voltage boost. However, the limited 5-level output results in increased THD. The 7-level SC topology introduced in [18] reduces the number of switching devices through collaboration among series capacitors. Nonetheless, achieving capacitor voltage balance necessitates a complex modulation algorithm [19]. New structures of multilevel converters are discussed in [20]-[22] offering the capacity to generate higher levels with fewer switches, albeit requiring substantial capacitors and voltage balancing circuits.

A novel proposal for a switched diode MLI structure was proposed by Alishah *et al.* [23]. The number of positive levels lies in the series-connected cell count. As the number of series-connected cells increases, the quantity of active or conducting switches increases, resulting in a substantial increase in conduction losses. Therefore, power dissipation may take place. An H-bridge unit is needed to produce a negative voltage level within this framework. Hosseinzadeh *et al.* [24] introduced the SDMLI, which incorporates fewer devices to produce 7 levels with equivalent source values. The authors outlined two distinct methods [25], [26] for determining the DC source value to create a high-stepped output level while reducing the switch count. In this configuration, an RL load is not suitable because of the reverse current. This issue was addressed by Alishah *et al.* [27], who presented a method that allows bidirectional flow of current, albeit requiring additional switches and driver circuits. Additionally, with increasing levels, there is an increase in switches, resulting in high conduction loss. Seifi *et al.* [28] introduced a 3-level novel CHB MLI with 5 switches, 3 sources, and 1 diode. Despite the reduced number of switches and driver circuitries, the total blocking voltage (TBV) in this system was significantly elevated [29], [30]. In this manuscript, a novel SCMLI is introduced. By employing a series-parallel conversion technique involving capacitors and a DC source, the newly designed inverter is capable of producing numerous output levels while utilizing fewer power devices. This inverter is suitable for autonomously powering inductive loads.

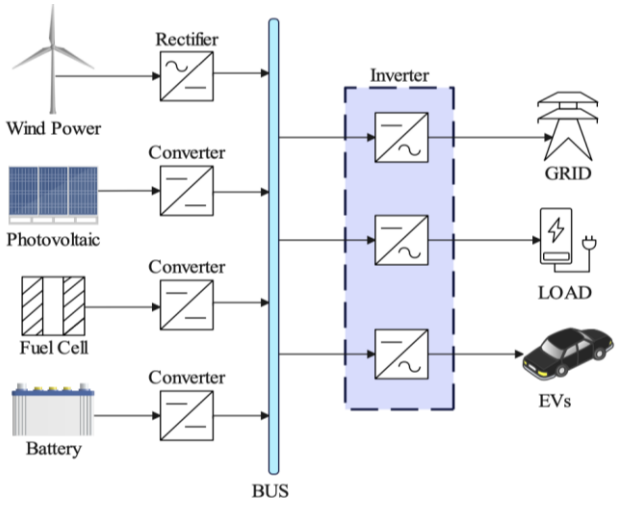


Figure 1. Distributed renewable energy generation system

This examination of the literature suggests the potential for novel topologies featuring a reduced quantity of devices in high boosting factor configurations. The principal objective of this manuscript is to introduce a novel layout of the inverter through the utilization of the switched-capacitor methodology, incorporating the following significant elements: utilization of a singular DC voltage source, ability to produce up to nine voltage levels employing 8 switches, double the voltage amplification (V_o: V_{in}=2), self-balanced voltage of the SC, spontaneous generation of polarity, and decreased voltage rating of the switch components. This article is presented as follows: Section 2 outlines the circuit description and operational modes of the proposed inverter. Section 3 presents a comparison study of MLI topologies with the proposed inverter. Section 4 presents the simulation results along with a discussion. Section 5 provides the conclusions of the article.

2. PROPOSED DB-SCI TOPOLOGY

2.1. Circuit description

A 9 L-DB SCI is shown in Figure 2, consisting of 8 switches, 3 capacitors, 2 Diodes, and 1 DC source. The selection between the IGBT (or) MOSFET for the switches is dependent on the specific applications at hand. The suggested inverter possesses the ability to increase voltage levels. The proposed 9 L-DB-SCI MLI is capable of achieving various voltage levels, including 0, ±0.5V_{in}, ±V_{in}, ±1.5V_{in}, and ±2V_{in}. The conduction states of the proposed 9 L-DB SCI MLI configuration for all voltage levels are displayed in Figure 3. In the 9 L-DB SCI, the DC-link capacitor is utilized to divide the input voltage equally, there by generating voltage levels of ±0.5 V_{in} and ±1.5 V_{in}.

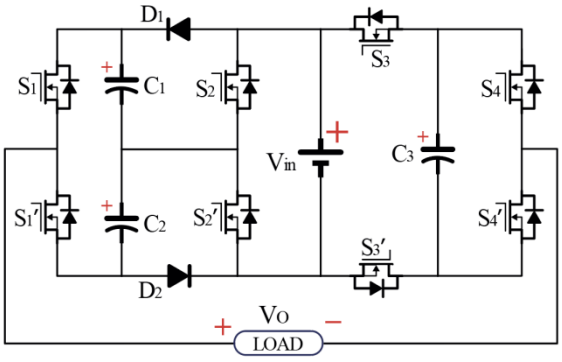


Figure 2. Proposed DB-SCI 9-level inverter circuit

2.2. Operating principle

The operational statuses of various devices are presented in Table 1, where S_1 - S_4 are compliant with S_1'-S_4', encompassing the activated and deactivated conditions of the power switches and capacitors. The operational statuses of devices are denoted by 1/0, specifically ON/OFF. Under the assumption of a pure resistive current scenario, this section concentrates on the DB-SCI modes of operation throughout the positive half cycle under constant conditions. Where:

$$S_1 S_2 = \bar{S_1}\bar{S_2}$$
$$S_3 S_4 = \bar{S_3}\bar{S_4}$$

Level 1: in this mode, a +2 V_{dc} output level is generated. Switches S_1, S_2, S_3', and S_4' are in the ON position, as shown in Figure 3(a), whereas all other switches remain OFF. Capacitor C_1 discharges, contributing to the output voltage, whereas C_2 charges. The capacitors and DC source are arranged to produce the maximum output voltage.

Level 2: in this mode, the output is +1.5 V_{dc}. Switches S_1, S_2, S_3, and S_4' are turned ON, as shown in Figure 3(b). The overall voltage is slightly lower than the maximum voltage because of C_3 discharging. Capacitor C_3 discharges alongside C_1, whereas C_2 continues to charge, resulting in a slightly lower voltage.

Level 3: this mode produces an output of +1 V_{dc}. As shown in Figure 3(c), switches S_1, S_2', S_3', and S_4' are ON, whereas the others are OFF. C_1 charges while also contributing to the output voltage. The output is lower than in previous levels since only C_1 is involved in the process.

Level 4: in this mode, C_1 and C_2 maintain a voltage of V_{in}, whereas C_3 holds 0.5 V_{in}. As shown in Figure 3(d), when S_2 turns ON, diode D_1 performs forward, clamping SC C_1 to the V_{in} level and placing it in parallel with the DC source. When the floating capacitor C_3 discharges through the load, switches S_1, S_3, and S_4 are ON, producing an output of 0.5 V_{in}.
Level 5: in this mode, the output voltage is 0 V_{dc}. As illustrated in Figure 3(e), all switches except S_1, S_3, S_4, and S_2' are OFF. With no DC supply.

Similarly, the modes of operation for negative levels of $0.5V_{dc}$, $1V_{dc}$, $1.5V_{dc}$, and $2V_{dc}$ are shown in Figures 3(f)-(i), respectively.

Table 1. Operating states of the DB-SCI inverter

States of Switches				States of Capacitors			Output Voltage and Level	
S_1	**S_2**	**S_3**	**S_4**	**C_1**	**C_2**	**C_3**	**V_L**	
1	1	0	0	D	C	-	+2 (Level 1)	Positive levels
1	1	1	0	D	C	D	+1.5 (Level 2)	
1	0	0	0	C	-	-	+1 (Level 3)	
1	0	1	0	C	-	D	+0.5 (Level 4)	
1	0	1	1	C	-	-	0 (Level 5)	Zero level
0	1	1	0	-	C	C	-0.5 (Level 6)	Negative levels
0	1	1	1	-	C	-	-1 (Level 7)	
0	0	1	0	C	D	C	-1.5 (Level 8)	
0	0	1	1	C	D	-	-2 (Level 9)	

Where C – Charging, D – Discharging, – No effect

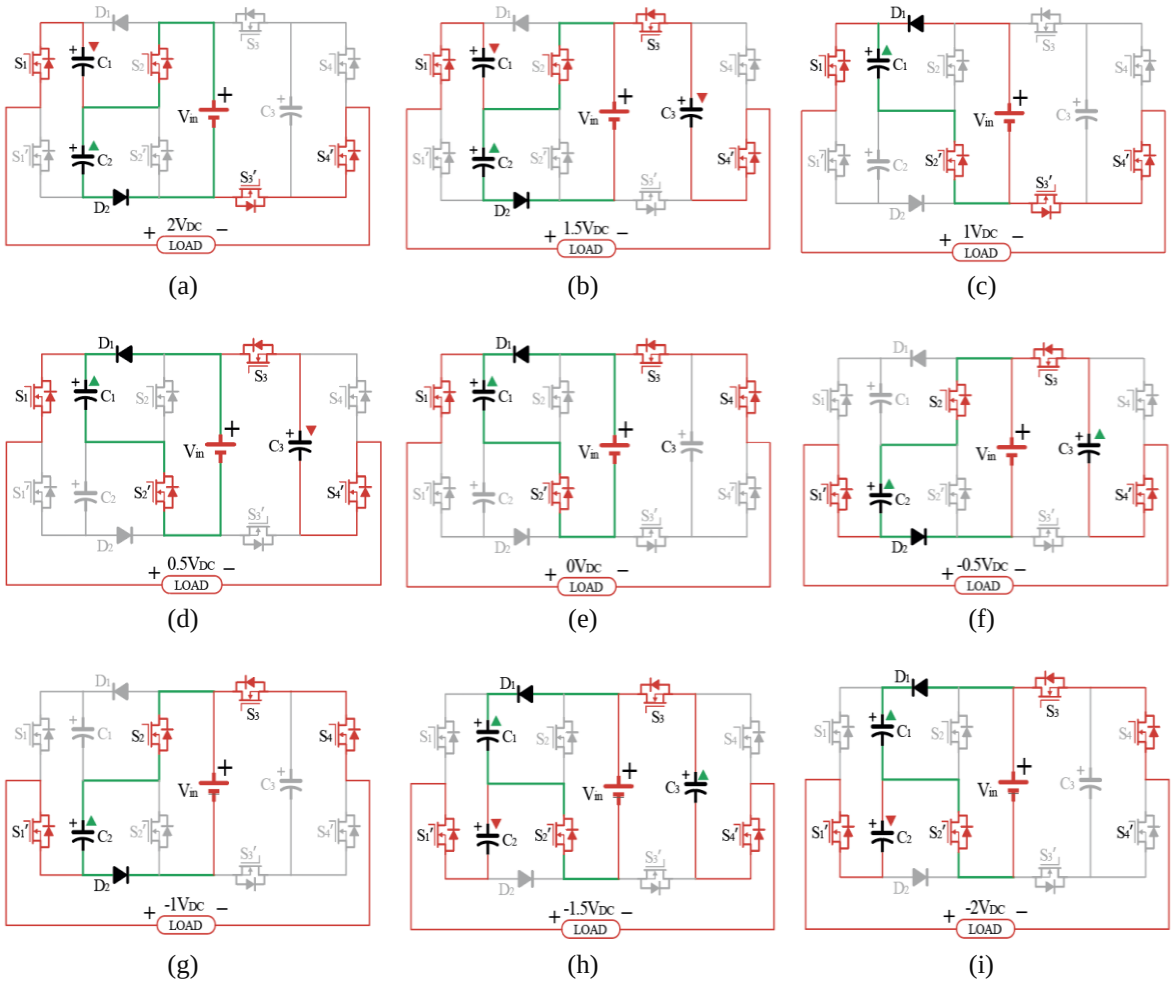


Figure 3. Switching states of the proposed DB-SCI topology: (a) $2V_{dc}$, (b) $1.5V_{dc}$, (c) $1V_{dc}$, (d) $0.5V_{dc}$, (e) $0V_{dc}$, (f) $-0.5V_{dc}$, (g) $-1V_{dc}$, (h) $-1.5V_{dc}$, and (i) $-2V_{dc}$

2.3. Capacitor voltage balancing

In SCMLIs, the inherent ability of the capacitors to balance their own voltage eliminates the need for complex control algorithms and additional voltage-balancing circuits. Voltage equilibrium across the capacitors is achieved by connecting them in parallel with the DC source during charging and in series during discharging. The proposed topology employs this same principle via the LSPWM technique to ensure self-balancing of the capacitors. In this configuration, both capacitors charge to half the input voltage at zero and $\pm V_{dc}$ voltage levels. During the positive half-cycle of 1 V_{dc} and 2 V_{dc} voltage levels, capacitor C_1 discharges, whereas C_2 discharges during the negative half-cycle of these levels. As illustrated in Figure 4, C_3 discharges during the positive cycle and charges during the negative cycle. Furthermore, the LSPWM technique guarantees ampere-second balance across both capacitors, indicating that the capacitors in the proposed MLI are self-balancing. In terms of boost and multilevel output, the proposed architecture allows for a twofold voltage increase and generates a nine-level output. This feature improves the overall performance of the inverter while enhancing its versatility and functionality.

2.4. Sizing of the capacitors

It is determined by various parameters in inverters, such as the longest discharging period, voltage ripple, output frequency, and load. In the topology being suggested, capacitors C_1 and C_2 experience equal longest discharging periods at $+1V_{dc}$ and $-1V_{dc}$ voltage levels, respectively. The longest discharging time intervals for C_1 and C_2 are noted as t_6 - t_3 and t_{14} - t_{11} from Figure 4. The discharge amount during these intervals can be calculated accordingly via (1) and (2).

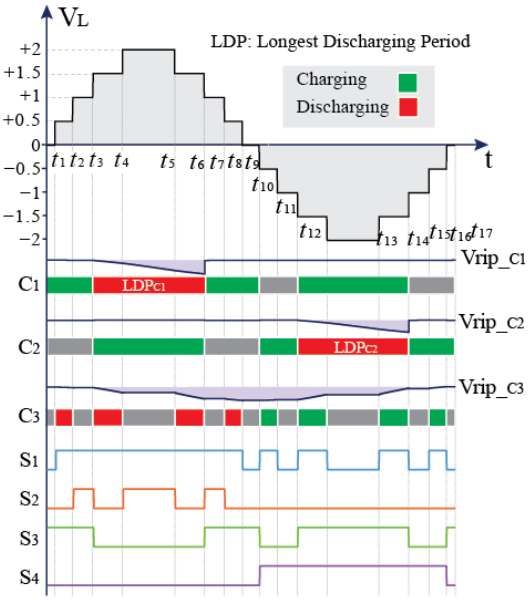


Figure 4. Capacitor waveform with 9-level output voltage

$$\Delta Q_{c1} = \int_{t_3}^{t_6} I_L \sin(2\pi f_o t)dt \quad (1)$$

$$\Delta Q_{c2} = \int_{t_{11}}^{t_{14}} I_L \sin(2\pi f_o t)dt \quad (2)$$

$$\Delta Q_{c3} = 2\left(\int_{t_1}^{t_2} I_L \sin(2\pi f_o t)dt + \int_{t_3}^{t4} I_L \sin(2\pi f_o t)dt\right) \quad (3)$$

The capacitances for the proposed configuration are derived by taking into account the maximum acceptable ripple voltage factor k. The capacitance values are determined via (3).

$$C_1 = C_2 = C_3 \geq \frac{\Delta Q_{c2}}{K V_{c2}} \quad (4)$$

Here, V_{c2} represents the rated voltage across capacitor C_2.

The voltage fluctuations of the capacitor during its charging period will result in voltage ripple loss *(Pr).* From (4), the voltage ripple for the capacitors is given as:

$$\Delta V_{c1} = \frac{\Delta Q_{c1}}{C_1}$$
$$\Delta V_{c2} = \frac{\Delta Q_{c2}}{C_2}$$
$$\Delta V_{c3} = \frac{\Delta Q_{c3}}{C_3} \quad (5)$$

Finally, the voltage ripple loss for the capacitors over one fundamental cycle period can be obtained as:

$$P_{r1} = \frac{f_o C_1 \Delta V_{c1}{}^2}{2} = P_{r2} = \frac{f_o C_2 \Delta V_{c2}{}^2}{2} = P_{r3} = \frac{f_o C_3 \Delta V_{c3}{}^2}{2} \quad (6)$$

The ripple loss is identical for both capacitors since their behavior is symmetric in both positive and negative half cycles.

2.5. Modulation strategy

There are numerous modulation techniques that can be employed to acquire the staircase output waveform for an MLI. These modulation strategies necessitate the comparison of carrier waves with a reference wave. Various carrier waveforms at different frequencies have been utilized in different LS-SPWM techniques to evaluate the THD of MLI. This suggested configuration is controlled via phase disposition (PD), phase opposition disposition (POD), alternative phase opposition disposition, variable frequency phase disposition (VFPD), variable frequency phase opposition disposition (VFPOD), and variable frequency alternative phase position disposition (VFAPOD)-SPWM techniques. The carrier waveforms employed include triangular, sawtooth, and reverse sawtooth, whereas a sine wave serves as the reference waveform throughout the entire switching process. To generate the 9-level output waveform, the control approach necessitates eight carrier waveforms encompassing both positive and negative waveforms. Within the proposed framework, a sinusoidal waveform with a frequency of 50 Hz is consistently compared with eight carrier waveforms. In the phase disposition strategy, all carrier signals are synchronized, as shown in Figure 5.

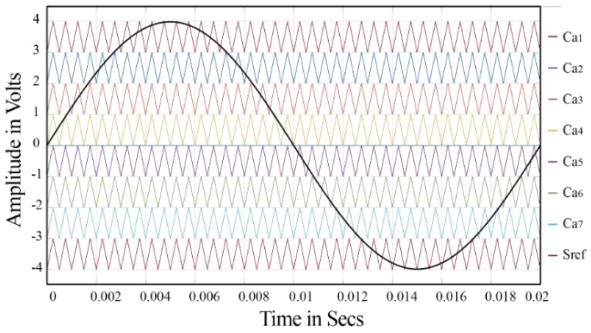


Figure 5. LS-PWM PD arrangement of carriers for 9-level inverter

This particular methodology uses eight carrier signals to produce a nine-level output voltage. Its functionality centers on comparing a sinusoidal reference waveform with vertically shifted carrier waveforms. Carrier signals above the zero axis exhibit identical frequency, amplitude, and phase alignment. On the other hand, carrier waves below the zero axis display matching frequency and amplitude but are in phase, albeit phase-shifted by 180^0 compared with carrier waveforms above the zero axis. In the context of alternative phase opposition disposition, each carrier waveform shares the same frequency and amplitude but undergoes a phase shift of 180^0 from its neighboring carrier. Notably, odd carrier waveforms are in phase but 180^0 out of phase with even carrier waves. The variable-frequency phase disposition technique involves maintaining phase synchrony among all carriers while adjusting their frequencies. Like other methodologies, this approach uses eight carrier signals to generate a 9-level output voltage through the comparison of a sinusoidal reference waveform with vertically shifted carrier waveforms. Carrier signals above the zero axis exhibit alternating frequencies with identical amplitudes and phase alignment. Conversely, carrier waves below the zero axis demonstrate alternating frequencies and equal amplitudes and are in phase but are phase-

shifted by 180^0 compared with their counterparts above the zero axis, as is the case for the VFPOD-PWM. Similarly, in VFAPOD, each carrier waveform within the variable-frequency alternative phase opposition disposition approach features alternating frequencies and amplitudes, along with a 180^0 phase shift from its adjacent carrier. Although odd carrier waveforms show phase alignment, they are 180^0 out of phase with even carrier waves.

3. COMPARISON STUDY WITH RECENT MLI TOPOLOGIES

A thorough comparative analysis of the proposed topology with previously published MLIs configurations is conducted. Table 2 presents a comparative assessment of NL, NSW, ND, NC, the number of driver circuits (NDR), the number of DC sources (NDC), the per unit TSV, VG, the need for H-bridge circuitry, and overall efficiency.

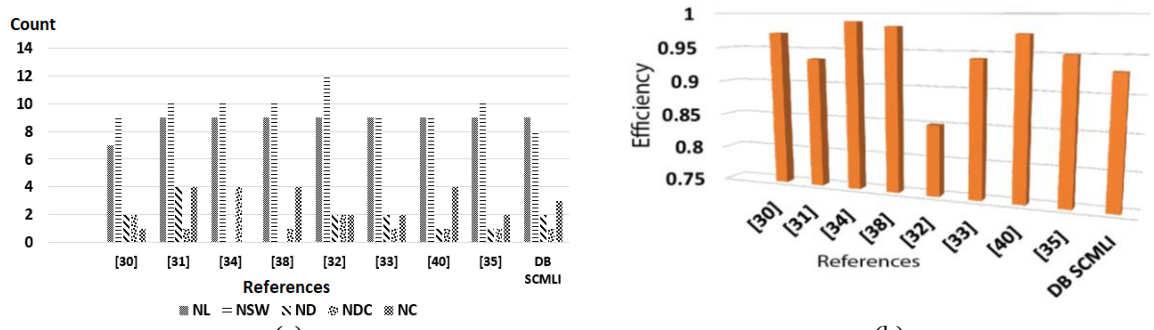
Zeng *et al.* [31], a 9-level voltage output is generated with ten switches, four diodes, four capacitors, and one DC source but lacks voltage boosting. Liu *et al.* [32] achieved double voltage enhancement with fewer capacitors but increased the number of active power switches to twelve and the per-unit TSV to ten. Liu *et al.* [33] reduces the switch count to nine for dual voltage boosting but requires an H-bridge circuit, resulting in higher switch voltage stress and TSV. Lee *et al.* [34], four DC sources generate a 9-level voltage output, eliminating voltage boosting. Barzegearkhoo *et al.* [35] creates a 9-level output voltage waveform with ten switches and two switched capacitors, with voltage boosting limited to a factor of two. Taghvgie *et al.* [36] developed a quadruple voltage-boosted 9-level output with nineteen switches and three capacitors, minimizing the switch voltage stress. The topology in [37] uses eight switches for quadruple voltage boosting but requires three switched capacitors for the 9-level output waveform. Zhang *et al.* [38] uses ten switches and three capacitors to produce a 9-level output voltage, achieving high efficiency (98.3%) while delivering 1 kW of power but without voltage boosting. The researchers [39] and [40] describe 9-level output voltage waveforms using nine switches. A quadruple boost 9-level topology in [41] employs 8 switches and two capacitors. The proposed configuration uses 8 switches with reduced voltage stress and three switched capacitors to produce a 9-level voltage with double boosting capability, featuring lower switch voltage stress and a reduced TSV.

Figure 6 depicts the comparative bar diagram representation of MLI topologies with proposed one in terms of devices as shows in Figure 6(a) with the number of devices for the references in Table 2 through a bar chart, showing the proposed inverter's lower device count than those of the other 9-level designs. Figure 6(b) compares the efficiency performance with that of other inverter topologies.

Table 2. Comparison with recently, reported similar MLIs

Ref.	NL	NSW	ND	NDC	NC	TSVpu	VG	H Bridge
[31]	9	10	4	1	4	7.25	1	Y
[34]	9	10	0	4	0	6	1	Y
[38]	9	10	0	1	4	6.25	1	N
[32]	9	12	2	2	2	10	2	Y
[33]	9	9	2	1	2	6.5	2	Y
[40]	9	9	1	1	4	5	2	N
[35]	9	10	1	1	2	6	2	Y
DB SCMLI	9	8	2	1	3	5	2	N

Where NL = number of levels, Nsw = number of switches, ND = number of the Diode, NDC=number of sources, NC = number of the capacitor, TSV -Total standing voltage, VG = Voltage gain



(a) (b)

Figure 6. Comparison of the proposed topology on the basis of (a) number of switches and (b) topology efficiency

4. SIMULATION AND RESULTS

To investigate the ability of the proposed MLI to produce a specified stepped output voltage waveform via the proposed algorithm, a simulation was conducted via MATLAB/Simulink. Figure 7 depicts the voltage and current waveforms under different loads, modulation indices, and frequencies, as shown in Figures 7(a)-(d), respectively, while Table 3 presents the parameters for various PWM techniques at different modulation indices.

The analysis assumes that the on-state resistance and forward voltage drop of the power switches are minimal and that the capacitor is sufficiently large, the voltage fluctuation is minimal, and the inverter has reached a stable condition. This investigation delineates the operational conditions of the inverter under a resistive load scenario. In the presence of an inductive load, a distinct pathway in each of the inverter's operational statuses corresponds to the forward current pathway, enabling the integration of inductive loads into the proposed framework devoid of supplementary voltage regulation requirements.

The performance verification of the DB-SCI arrangement is conducted via the PD-PWM method, which is simulated in MATLAB/Simulink. A 9-level waveform with voltages of 0, ±80, ±160, ±240, and ±320 is the resultant waveform. The parameters for the simulation study are V=160 V_{dc}, 50 mH, and 100 **Ω** Figure 7(a) shows the voltage and current waveforms, Figure 7(b) shows the output waveforms for different load conditions, Figure 7(c) shows the simulation output waveforms for different MI variations, and Figure 7(d) presents the waveforms for different MIs and frequencies. DB-SCI generates a 9-level waveform with accompanying harmonic spectra in Figure 8 at a modulation index (MI) =1. The produced voltage waveform exhibits in Figure 8(a) with THD of 13.74%, with a maximum fundamental voltage of 320.1 V. Dominant harmonic orders are observed at the 18th, 22nd, and 40th positions. Figure 8(b) Current harmonic spectra of 2.91 are observed. Similarly, for varying MIs, the data were simulated for other level-shifted PWM methods and are tabulated in Table 3. The comprehensive analysis indicates that a modulation index of 1 yields superior harmonic spectra compared with other modulation indices.

Table 3. Proposed inverter simulation parameters

S. No	Parameter	Values
1	Input voltage (V_{in})	160 V
2	Output voltage (V_{out})	320 V
3	Inductor	50 mH
4	RL Load	100 ohm
5	fc, fc2	1,000 Hz, 2,000 Hz
6	Fr	50 Hz

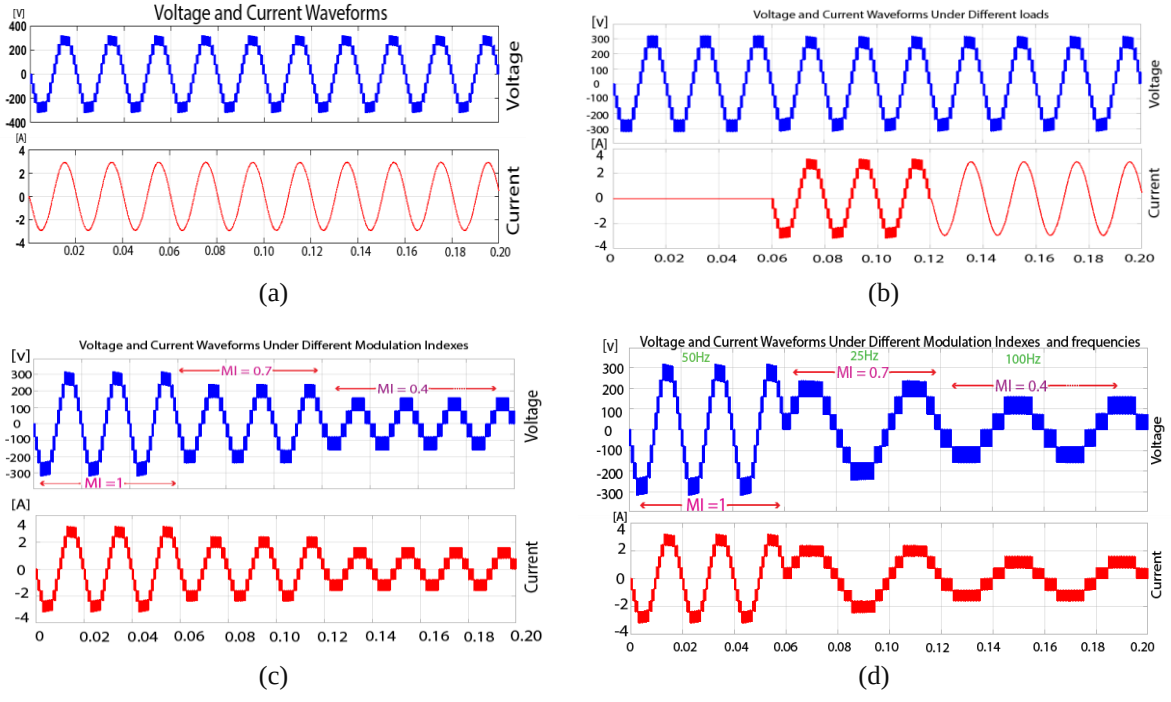
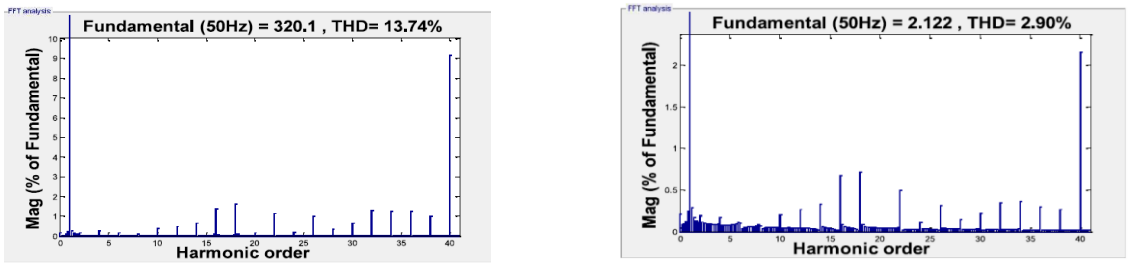
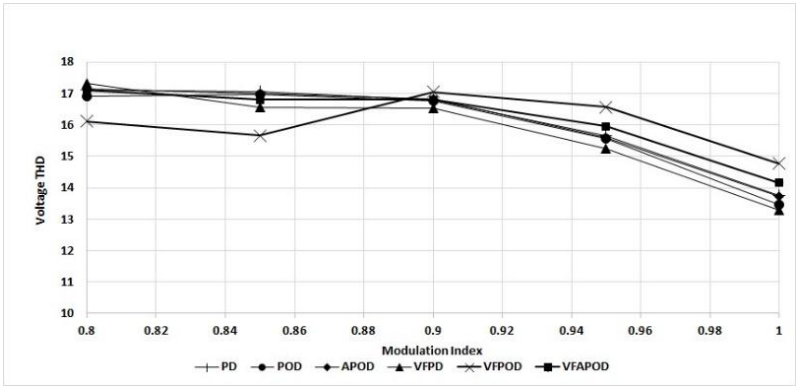


Figure 7. Voltage and current waveform of MLI under various conditions: (a) R=100 ohm, L=50 mH load, (b) different RL loads, (c) different Mis, and (d) different MIs and frequencies

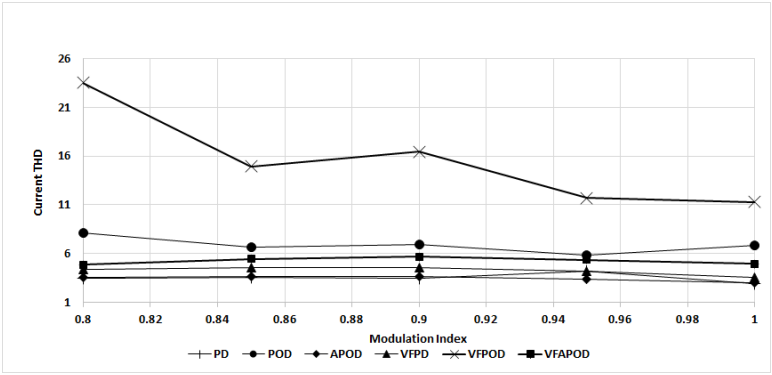


(a) (b)

Figure 8. Harmonic waveforms (a) analysis of the voltage FFT and (b) analysis of the current FFT (MI= 1)



(a)



(b)

Figure 9. Comparison representation of PWM techniques (a) voltage THD vs MI and (b) current THD vs MI

Figure 9 presents graphical charts representing the voltage THD and current THD for various PWM techniques across different modulation indices in Figures 9(a) and (b), respectively. The graphical analysis of the voltage THD and current THD for various PWM techniques across different modulation indices reveals distinct trends. For the PD technique, the voltage THD consistently increases as the modulation index decreases, whereas the current THD remains relatively stable with slight variations. The POD technique results in a similar increasing trend in the voltage THD but with more noticeable fluctuations in the current THD. The APOD technique shows a steady increase in the voltage THD with minor fluctuations in the current THD, indicating consistent performance.

VFPD demonstrates an increasing trend in both the voltage and current THD as the modulation index decreases, suggesting greater distortion at lower modulation indices. VFPOD presents significant fluctuations in both the voltage and current THD, indicating variability and potential instability across different modulation indices. Finally, VFAPOD shows a consistent increase in the voltage THD with relatively minor fluctuations in the current THD, maintaining a more stable performance than the other techniques do. These observations highlight the impact of modulation indices on THD and underscore the importance of selecting appropriate PWM techniques on the basis of specific performance criteria.

The efficacy of the proposed topology is proven through a simulation setup, where critical parameters such as the root mean square (RMS), (%THD), peak voltage and current are evaluated. Table 4 shows the simulation findings of all the techniques. The utilization of the variable-frequency PD technique with a modulation index (MI) of 1 leads to an improved THDv of 13.28% and THDi of 3.94%. The viability and efficacy of the suggested MSDBSCI are confirmed by the simulation results. A comparison of the implemented MLI with the conventional MLI is shown in Table 5.

Table 4. Simulation findings

PWM techniques	Modulation index	FFT PLOT		Harmonics level with various order			
		Voltage THD	Current THD	Voltage		Current	
				DC components	VRMS	DC components	IRMS
PD	1	13.74	2.9	0.5386	226.3	0.004461	1.501
	0.95	15.64	4.2	0.2526	215	0.01021	1.424
	0.9	16.8	3.48	0.3033	203.7	0.001234	1.351
	0.85	17.06	3.52	1.037	192.4	0.006156	1.275
	0.8	17.11	3.44	1.299	180.9	0.002835	1.2
POD	1	13.47	6.85	0.01584	226.9	0.000339	1.529
	0.95	15.56	5.82	4.427606	215.3	0.000388	1.446
	0.9	16.77	6.92	5.11E+06	203.6	0.00053	1.358
	0.85	16.98	6.62	0.01581	191.7	0.000718	1.271
	0.8	16.92	8.16	0.003954	181	0.000533	1.204
APOD	1	13.73	3	0.3325	226.3	0.0018	1.501
	0.95	15.6	3.36	0.3048	215	0.0017	1.426
	0.9	16.807	3.6	0.3205	203.7	0.0016	1.351
	0.85	17.01	3.6	0.273	192.4	0.001596	1.276
	0.8	17.14	3.51	0.2612	181.1	0.001516	1.201
VFPD	1	13.28	3.54	0.3094	226.5	0.002027	1.502
	0.95	15.25	4.2	0.2219	215.6	0.005364	1.429
	0.9	16.52	4.59	0.5428	204.4	0.007205	1.355
	0.85	16.57	4.55	0.3762	192.7	0.005986	1.278
	0.8	17.31	4.37	0.3565	181.16	0.005664	1.203
VFPOD	1	14.77	11.28	0.03569	226.5	0.001736	1.522
	0.95	16.57	11.69	0.007926	214.2	0.002243	1.431
	0.9	17.05	16.47	0.01189	202.2	0.002853	1.366
	0.85	15.66	14.95	0.01983	191	0.003022	1.258
	0.8	16.11	23.54	0.777928	180.1	0.002809	1.188
VFAPOD	1	14.15	4.96	0.5836	226.5	0.000314	1.501
	0.95	15.95	5.37	0.9325	214.8	0.01031	1.424
	0.9	16.8	5.66	1.466	203.7	0.001058	1.35
	0.85	16.8	5.44	1.027	192.4	0.007591	1.276
	0.8	17.11	4.86	1.299	170.11	0.009384	1.2

Table 5. Comparison between the proposed MLI and traditional MLIs

Parameter	CML	DCMLI	FCML	DB-SCI
NL	9	9	9	9
NS	16	16	16	8
ND	0	28	0	2
NCD	0	28	0	0
NDC	4	1	1	0
NBC	0	0	28	3
NGD	16	16	16	8

*NL, NS, ND, NC, NDC, NCD, NBC, NG: indicates the number of levels, Switches, diodes, capacitors, DC sources, clamping diodes, balancing capacitor, Gate drivers

5. CONCLUSION

This research endeavors to introduce a novel boost inverter that incorporates integrated subconscious equalization functionalities. The FCs demonstrate synchronized charging and discharging durations, thereby mitigating the requirement for substantial capacitance. The architecture, characterized by a reduced number of switches equipped with integrated polarity generators, yields advantages such as diminished power losses and enhanced efficiency in medium-voltage applications. A prominent drawback of traditional MLIs is their dependence on high-voltage DC–DC converters to increase voltage levels, particularly when harnessing renewable energy sources such as photovoltaic and fuel cells. The proposed framework effectively addresses this issue by providing a double voltage boost capability that autonomously elevates the input voltage. The developed nine-level converter undergoes simulation and validation via MATLAB software.

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AUTHOR CONTRIBUTIONS STATEMENT

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P
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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

The data that support the findings of this study are available on request from the corresponding author, Yassin Mohamed Shuaib. The data, which contain information that could compromise the privacy of research participants, are not publicly available due to certain restrictions.

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