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Power Factor Correction using Valley-Fill SEPIC Topology with Fuzzy Logic Control

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Abstract

This paper deals with a new single ended primary inductance converter (SEPIC) for power factor correction (PFC). The proposed converter is used in combination with SEPIC and a valley fill circuit. The valley fill circuit improves the efficiency of the SEPIC by reducing the harmonics in the supply mains. The power factor is also enhanced compared to the conventional PFC converters. It uses the simple control strategy for controlling the power factor of the AC mains. It can be preferred to low power applications, since it has the merits like less input current ripples and less total harmonic distortion (THD). To observe the performance of the Valley fill circuit, a model based on the SEPIC topology has been designed by using MULTISIM and MATLAB / SIMULINK environment and implemented with one cycle control (OCC) and Fuzzy logic controller. The simulations results are demonstrated in order to validate the effectiveness of the controllers in power factor improvement.

Keywords: *Valley-Fill SEPIC topology, one cycle control, fuzzy logic controller, power factor correction and total harmonic distortion*

1. Introduction

Due to the recent advancement in the LED technology, many topologies were introduced to improve the performance of the LED drivers. To ensure that the LED lights are more efficient than the conventional lighting system, the Valley-Fill circuit with SEPIC topology is proposed as a greener alternative to achieve power factor nearer to unity.

The European standard IEC 61000-3-2 (class C) instructs that the power factor and total harmonic distortion should be maintained for the lighting equipment exceeding above 25W. For incandescent lamps, the power factor is unity because it's a purely a resistive load then they are inefficient in terms of the amount of power consumed. The power factor can be improved to unity by the following two methods: 1) Passive power factor correction; 2) Active power factor correction.

For single phase applications, passive power filters and active one or two stage PFC rectifiers with SMPS (switched mode power supply) topologies [1-2] are the typical approaches to achieve higher power factor and to reduce total harmonic distortion. In passive power factor correction, the power factor can be brought near to unity using capacitors or inductors as they required. This filter needs a large value of inductors and capacitors which are bulky and pricey. The active power factor correction method is used to change the nature of input current fed to the load. The main intention is to make the load appears to be purely resistive. For example, the power factor can be improved from 0.7 to 0.9 by using the SMPS topologies. In order to achieve power factor up to 0.99, the SMPS topologies are implemented with passive power factor correction circuits. Without any power factor correction circuits, the power factor is only about 0.75 to 0.85. The single stage PFC circuits (Figure 1) were employed to drive multiple LED lamps and also to eliminate the additional DC to DC stage.

The circuit choices are buck, boost, buck-boost, flyback and single ended primary inductance converter [2-3] etc. These topologies are apposite for different power level and customer necessities. The single ended primary inductance converter has the advantages of less noise, less switching loss and it can be operated at higher frequencies than that of the flyback converter. Total number of components is similar for both the SEPIC and flyback

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converters (number of power components and supportive components). The main disadvantage of the flyback converter is required of snubber. Continual input current not only reduces ripples, it also improves the electromagnetic emissions of the system. So, this SEPIC converter can be used for high brightness LED lighting applications[4] without requiring excessive complication, component count and cost.

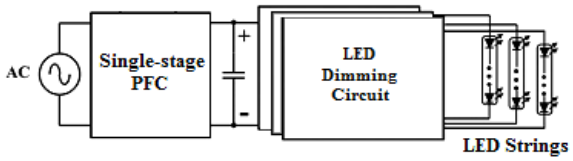
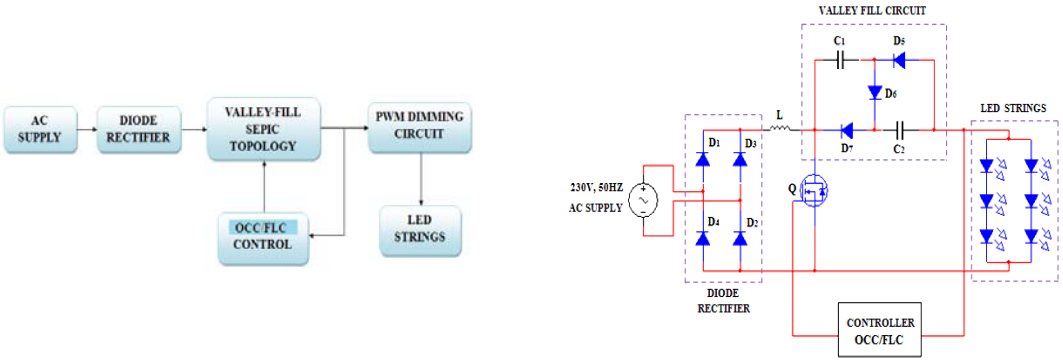


Figure 1. Single Stage LED Driver Circuit

2. Valley Fill SEPIC Topology

Figure 2 shows the block diagram of the Valley-Fill SEPIC Topology, the total harmonic distortion is reduced and power factor is improved when the converter is operated with constant ON and OFF time.



(a) (b)

Figure 2. Valley-Fill SEPIC Topology

The input source is the AC line and then some type of conversion stage must be carried out among the line and the LEDs. So the diode rectifier is the front end converter for all the LED drivers. The input 230V, 50Hz AC voltage is applied to the diode rectifier which converts the AC to DC voltage. The main problem with this diode rectifier is that it is a nonlinear device and it draws a nonlinear input current. The Valley-Fill [5-7] SEPIC topology is used to modify the wave shape of current drawn by a load. It consists of passive components and two diodes. This circuit in addition with SEPIC topology improves the power factor.

3. Control Technique for SEPIC Valley Fill Circuit

3.1. One Cycle Control (OCC)

Control circuit for One Cycle Control technique is shown in Figure 3. At the beginning of each switching period, a constant frequency clock turns ON the transistor [8-10]. The output voltage is integrated and compared with the reference value. If the integrated voltage attains the reference value, the comparator changes its state. When the integrator is reset to zero, the transistor is turned OFF. If the control reference is stable, then the average of the diode voltage and the output voltage is constant.

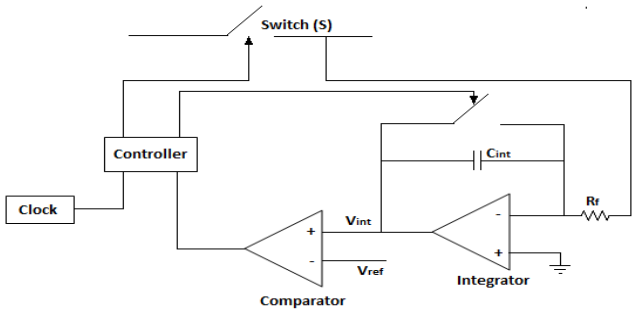


Figure 3. Control Circuit - One Cycle Control

The slope of the integration is directly proportional to the input voltage. The integrated value is always compared with the constant control reference. If the input voltage is higher, then the slope of the integration is steeper; therefore, the integration value attains the control reference quicker. As a result, the duty ratio is inversely proportional to the input voltage. If the control reference is variable, then the diode voltage is equal to the changing control reference in each cycle; therefore, the output voltage equals the reference voltage. The integrated value of the diode voltage catches the control reference immediately.

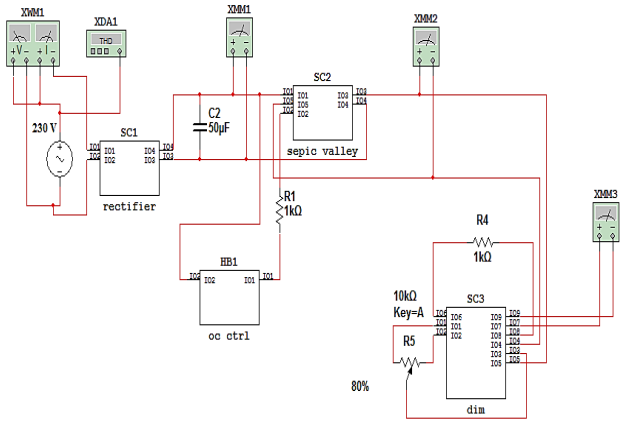


Figure 4. Simulation Circuit - Valley-Fill SEPIC Topology with OCC

The simulation circuit for one cycle control technique with Valley-Fill circuit is shown in Figure 4. Simultaneously to turn ON the transistor and to trigger the Integrator, the controller uses constant frequency pulses. Then the integrated output voltage is compared with a control reference. The instant when the integrated output voltage reaches the control reference, the transistor is turned OFF and the Integrator value is reset to zero. If the control reference is even, then they obtained average of the output voltage is invariable.

3.2. Fuzzy Controlled Valley fill SEPIC Topology

The simulation circuit for fuzzy logic controller with Valley-Fill circuit [11-12] is shown in Figure 5. The performance of fuzzy logic controller only depends on the selection of membership function variables and inference of fuzzy rules. A fuzzy logic controller is a powerful tool in coping with time varying the nonlinearities and uncertainties [13-15]. By using this, the input crisp values are converted into fuzzy variables and they are mapped as linguistic labels.

The Membership Function (MF) of the input and output variables of fuzzy are generally defined on a common universe of discourse. For having the best design of FLC, the proper selection of input and output scaling factors including the tuning of other parameters needed for controller, are very important. This, in many cases is achieved through trial and error to get best

performance. For the proposed system, triangular input and output membership functions are selected and it is shown in Fig.6. The FLC consists of two inputs and one output. The inputs for the FLC are error voltage e and change in error voltage ∆e. The output variable is u and it controls the operation of switch. Five membership functions are chosen for error (e), change in error (∆e) and for output (u).

The Membership functions are defined within the normalized range and associated with each label: NB (negative big), NS (negative small), ZO (zero), PS (positive small), and PB (positive big).

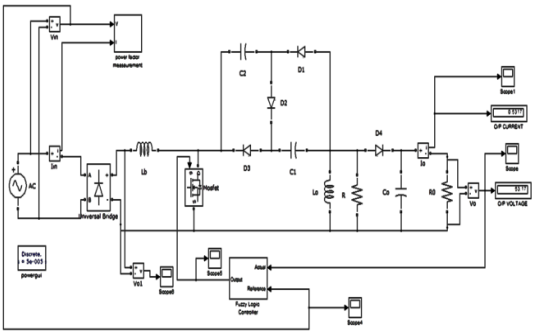


Figure 6. Simulation Circuit - Valley-Fill SEPIC Topology with FLC

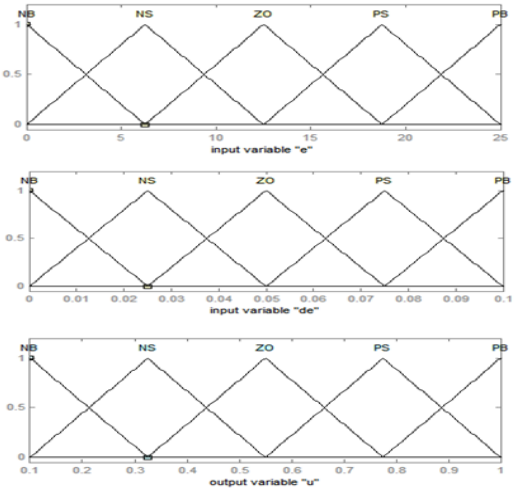


Figure 6. Membership Functions

Table 1. Rule Matrix

e \ ∆e O/P	NB	NS	Z	PS	PB
NB	NB	NB	NS	NS	Z
NS	NB	NS	NS	Z	PS
Z	NS	NS	Z	PS	PS
PS	NS	Z	PS	PB	PB
PB	Z	PS	PS	PB	PB

A knowledge base contains the definition of the fuzzy subsets for the converter operation, their triangular membership functions and the whole rules of the inference system. The fuzzy control work for such rules insisted to it. Here 25 rules are framed for controlling the SEPIC converter, thus the power factor is improved and current THD is reduced.

The centroid Defuzzification process is used convert the inference mechanism into actual inputs for the process. The Rule Viewer (Figure 7) is used to displays the whole fuzzy inference process according to the rule matrix as given in Table 1.

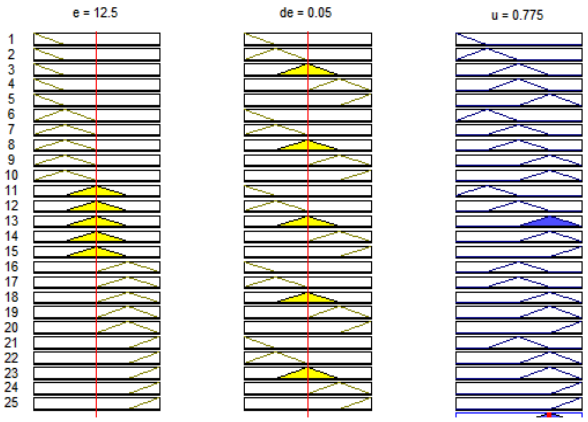


Figure 7. Rule Viewer

Some of the basic rules framed for the above power factor correction are given below,
If (e is NB) and (∆e is NB) then (u is NB)
If (e is NB) and (∆e is NS) then (u is NB)
If (e is NB) and (∆e is Z) then (u is NB)
If (e is NB) and (∆e is PS) then (u is NS)
If (e is NB) and (∆e is PB) then (u is Z)

The Surface Viewer is a GUI (graphical user interface) tool used to get a different three-dimensional view of the data and helps to examine the output surface of the system, for two input system. The inputs of the surface viewer are error voltage e and change in error voltage ∆e. The output variable obtained from fuzzy logic controller for the inputs given is indicated as u. The overall mapping has been done in single plot and is shown in Figure 8.

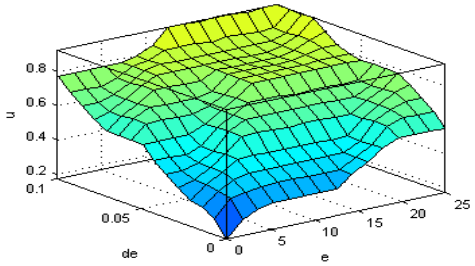


Figure 8. Surface Viewer

4. PWM Dimming Circuit

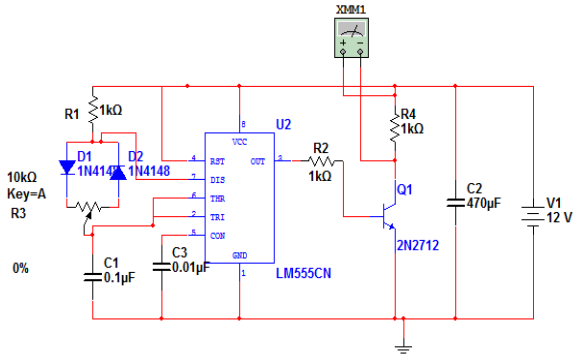


Figure 9. PWM Dimming Circuit

A PWM dimming control is employed as the second stage current regulator as shown in Figure 9. This circuit uses the LM 555 timer which generates a continuous pulse through Pin 3 as a square wave.

The stable mode has no stable state. The output changes its state continually between high and low without any interventions. LM 555 timer based dimming circuits are also used for flashing lamps and it is used as a clock pulse for other circuits also. This turns the LED lights ON and OFF. By varying the resistors R_1 and R_2, the turn ON and turn OFF speed of the LEDs can be adjusted. The longer the ON period, the brightness of the LEDs will be more. The potentiometer is varied from 5% - 95% to attain different voltage levels. When the potentiometer is adjusted to the minimum position (0%), the obtained output voltage is 11.908 Volts as shown in Figure 10(a). During this period, the brightness of the LED will be more. And the brightness of the LED will be less, if the potentiometer is adjusted to the maximum position (100%). The obtained output voltage in this position is 1.113 Volts and it is shown in the Figure 10(b).

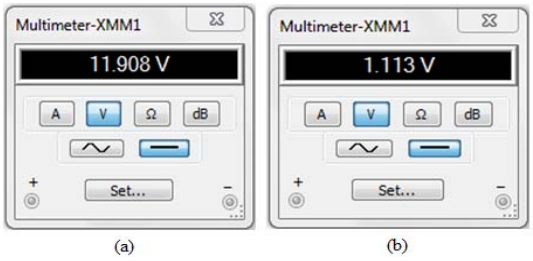


Figure 10. Different Voltage Levels

5. Simulation Results

5.1. MULTISIM Simulation Results for One Cycle Control

Figure 11 shows the Watt meter and Distortion Analyzer readings of the proposed Valley-Fill SEPIC topology with one cycle control technique. While driving the PFC topology by implementing the OCC technique, the power factor is 0.969 and the total harmonic distortion is 28.794 %.

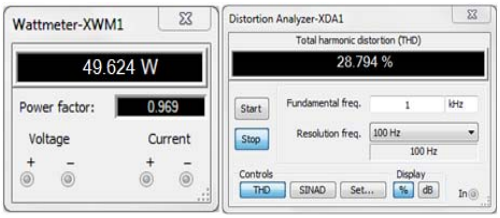


Figure 11. Measured Power Factor and THD of OCC

5.2. MATLAB simulation with Fuzzy Logic Controller

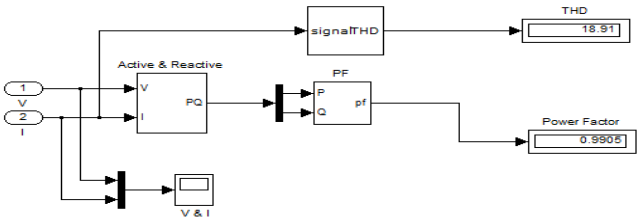


Figure 12. Measured Power Factor and THD of FLC

Figure 12 shows the power factor as 0.9905 and the total harmonic distortion as 18.91 % of the proposed Valley-Fill SEPIC topology with fuzzy logic controller.

Figure 13 shows the input voltage and current waveform of the Valley-Fill SEPIC derived topology with fuzzy logic controller.

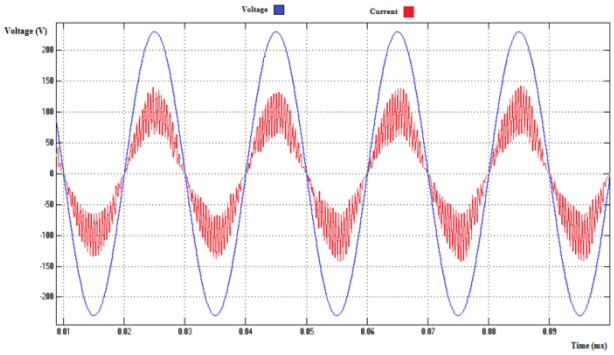


Figure 13. Input Voltage and Current Waveform

The rectified DC voltage waveform of the single phase diode rectifier is shown in Figure 14. The magnitude of the pulsated DC voltage is 230V. The duty cycle obtained from the fuzzy logic controller is shown in Figure 15 which is supplied to the MOSFET switch (Q) driving the proposed Valley-Fill SEPIC power factor correction topology. Due to high frequency operation, MOSFET is preferred often.

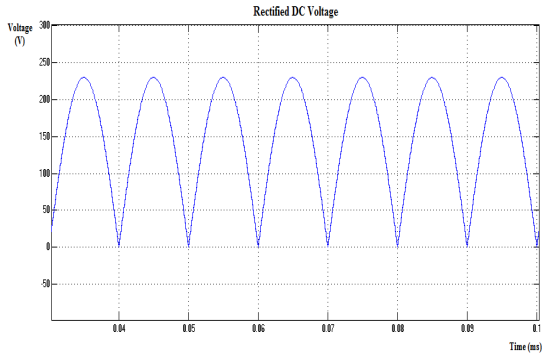


Figure 14. Rectified DC Voltage Waveform

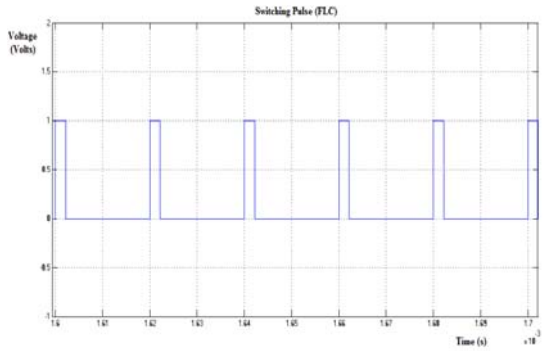


Figure 15. Waveform of the Duty Cycle

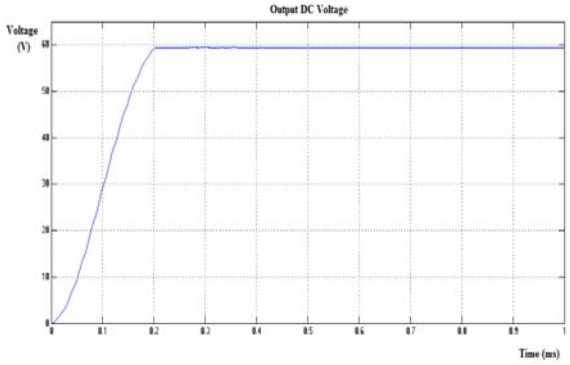


Figure 16. DC Output Voltage Waveform

Figure 16 shows the DC output voltage waveform of the Valley-Fill SEPIC derived topology with fuzzy logic controller. The magnitude of the obtained dc voltage is 59.47V. The output current waveform of the Valley-Fill SEPIC derived power factor correction topology with fuzzy logic controller is shown in Figure 17. The obtained output DC current is 0.5947A.

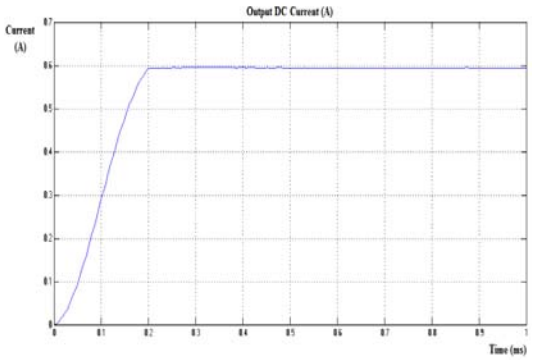


Figure 17. Output Current Waveform

5.3. Comparision of Results

The comparison of power factor and total harmonic distortion of the proposed system with one cycle control technique and fuzzy logic controller are shown in Figure 18. By this, the proposed topology is more efficient when the Valley-Fill SEPIC PFC topology is controlled using fuzzy logic controller.

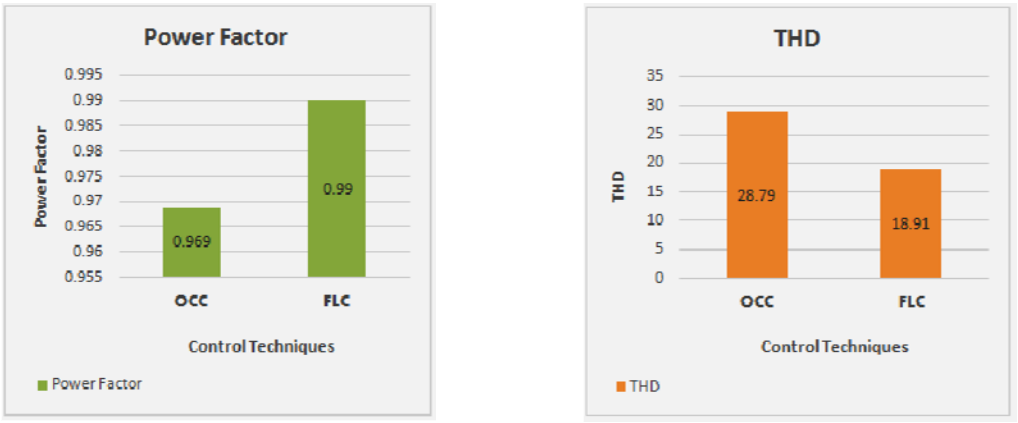


Figure 18. Comparison Chart of OCC and FLC with Valley Fill SEPIC Circuit

6. Conclusion

The simulation of Valley-Fill SEPIC derived power factor correction topology for LED lighting application using one cycle control technique and fuzzy logic controller has been carried out for reducing the input current THD and for improving the power factor. This Valley fill circuit contains only passive components and with the combination of SEPIC improves the power factor. This proposed topology is small in size, less cost, with one stage of power conversion, simple feedback control and achieves power factor is nearer to unity. The OCC and FL control techniques were employed for controlling the proposed topology. In this control setup, the fuzzy logic controller provides better power factor (0.9905) and reduced total harmonic distortion compared to OCC (PF=0.969). Thus, the MULTISIM and MATLAB Simulation results validate the effectiveness proposed system.

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