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Design of a segmented current steering digital to analog converter using PMOS cascode current source in UMC 65 nm technology

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ABSTRACT

Digital to analog converters (DAC) are the fundamental data converters used in the digital data transmission. In this paper 8-bit DAC is proposed using current cells with LSB current of 2 µA and full-scale voltage of 420 mV. Current cells mean the current sources designed using the MOSFETs. When it comes to mixed-signal and analog integrated circuits, current cells are the fundamental building blocks that are available. The optimized performance of current source is obtained with the proper biasing circuit. The performance of these current mirrors is evaluated in terms of key parameters such as output impedance, transconductance and linearity. The simulations for testing these parameters are performed using Virtuoso Cadence tool in umc 65 nm technology. After transistor characterization, various types of current sources are designed, and for each current mirror, PVT analysis is carried out for comparison and Monte-Carlo analysis is carried out to find the mismatch in current mirrors. Then different digital blocks are designed, that are D-Latch, Binary-thermo decoder and Row-column decoder which are required for designing of current steering DAC. Creating an 8-bit segmented current steering DAC by combining the ideas of 4-bit unary weighted and 4-bit binary-weighted DACs is the aim of this research. Performance measurements such as signal-to-noise ratio (SNR), effective number of bits (ENOB), spurious-free dynamic range (SFDR), differential non-linearity (DNL), and integral non-linearity (INL) are calculated to assess the proposed 8-bit segmented DAC. The analysis and designing of current mirrors in advanced CMOS technologies are critical for the development of high performance integrated circuits. An 8-bit DAC implemented using I_{LSB} current of 2µA with an accuracy of ±2%.

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1. INTRODUCTION

In recent years, designing low power and small area mixed-signal integrated circuits (ICs) has become a critical focus, especially for portable devices [1]-[3]. Modern portable telecommunication systems demand digital-to-analog converters (DACs) that are high-speed, low-power, and occupy minimal space [4]. Among the various DAC types, the current-steering DAC (CS-DAC) stands out for its high speed, low power

consumption, high resolution, and small area [5]. The advantages CS-DAC and its compatibility with CMOS processes make it a popular choice for applications in WLAN, UMTS, and GSM, though its design remains a challenging issue [6], [7].

Three architectures are available for the current-steering DAC: segmented, unary, and binary. The way that these layouts regulate the switching transistors of the current cells and weight the current sources vary. The input code in a binary weighted DAC flips a binary-weighted array of current cells. Although this architecture is straightforward and takes up little chip space, it has high glitch energy, challenging current source matching, and possible monotonicity problems [4], [8]-[10]. Unlike a binary weighted method, a unary weighted DAC uses an input code to govern the switching of a unary current source array. The switching of current cells is then managed by a binary-to-thermometer (BT) decoder, which first transforms the binary input code into a thermometer code. The benefits of this architecture include monotonicity and low integral and differential nonlinearity (INL/DNL) errors; nevertheless, it also includes a complex BT decoder, a bigger size, and a greater digital power consumption [4], [8], and [9].

With the segmented current-steering DAC, the benefits of both binary and unary designs combined. To reduce glitch power, the most significant bits (MSBs) are used in thermometer coding, while the least significant bits (LSBs) use binary weighted design to save power and chip space. This results in fewer INL/DNL errors, a smaller BT decoder, and less glitch energy [4], [9]. Traditional segmented current-steering DACs have a larger chip area, higher power consumption, and slower performance because the digital component consists of the BT decoder, latch, and driving circuits [5], [11]. Compared to the 4-bit BT decoder, this study proposes a row-column decoder that uses less power by using a current mode BT decoder instead of a voltage mode one. This reduces the size of the chip, lowers power consumption, and increases speed by doing away with the need for latch and driver circuits. The adoption of a 2-bit BT decoder further reduces chip footprint and power consumption.

The design and implementation [8] of an 8-bit segmented DAC in 180nm technology that achieves a wide range of current levels. This work [12] examines the effects of segmentation on the DNL and INL. This work discusses [13] an 8-bit segmented CS-DAC [14]. With minimal power consumption and INL error, this research proposes a partially segmented CS-DAC. In this work [15], a 4-bit high performance binary architecture is proposed using CNTFETS.

The necessity for achieving improved performance from the DAC underscores the importance of designing an optimized current cell [9]-[11]. A switch-controlled current source, appropriately biased to provide the required load current, is known as a current cell [16]-[19]. The total DAC performance depends on the accuracy of the current source. In this work the current source is designed using PMOS because the selection of PMOS current sources over NMOS counterparts is motivated by advantages such as higher voltage headroom, superior current mirroring accuracy, enhanced noise margins, improved temperature stability, compatibility with certain semiconductor processes, reduced susceptibility to process variations, and a higher output impedance, underscoring the importance of a judicious choice based on specific design requirements in optimizing circuit performance [18], [20]-[25].

Performance metrices:

The DAC's performance should be evaluated using the following criteria:

$$DNL_k = \frac{V_k^{actual} - V_{k-1}^{actual} - 1LSB}{1LSB} \quad (1)$$

$$INL_k = \frac{V_k^{actual} - V_k^{ideal}}{1LSB} \quad (2)$$

$$SNR = 10.log_{10}(\frac{P_{signal}}{P_{noise}}) \quad (3)$$

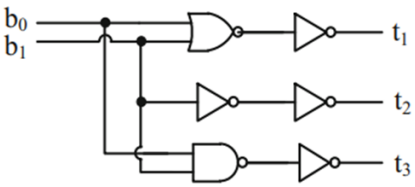
$$SFDR = 10.log_{10}(\frac{P_{signal}}{P_{spurious}}) \quad (4)$$

$$ENOB = \frac{SNR - 1.76}{6.02} \quad (5)$$

2. DESIGN OF THE PROPOSED SEGMENTED DAC

This section details the segmentation of the input bits for the proposed DAC. Traditional current-steering DACs commonly divide digital input bits into most significant bits (MSBs) and least significant bits (LSBs). Binary code is typically used for the LSBs, while thermometer code is employed for the MSBs

[4],[9]. In binary coding, each bit has a weight to the power of two, which activates its corresponding current source. The weight of b_0 is 2^0 which is 1, and this will produce I_{LSB} current. Similarly, b_1,b_2,b_3 will produce currents of $2I_{LSB}$, $4I_{LSB}$, $8I_{LSB}$ respectively. In binary-coding architecture, suppose if code changes from 0111 to 1000, then there is a huge amount of glitch produced in the output of this architecture. Here, b_0,b_1,b_2 will switch the current sources from on to off, and b_3 will switch the current source from off to on. In this example, all current sources are changing their states, which leads to a huge glitch. The design of the binary to thermometer (BT) decoder aims to overcome this glitch by switching only one current source, which the thermometer-coded architecture utilizes to eliminate it. The BT decoder converts the binary equivalent value into an equal number of unit elements, thereby producing 1 I_{LSB} of current. For an n-bit BT decoder, the number of output bits is 2^n-1. Figure 1 shows the binary values from 00 to 11, as well as the corresponding thermometer codes from t_3 to t_1.



Binary code		Thermometer code		
b_1	b_0	t_3	t_2	t_1
0	0	0	0	0
0	1	0	0	1
1	0	0	1	1
1	1	1	1	1

Figure 1. 2-bit BT decoder and its truth table

The architecture of the suggested DAC is shown in Figure 2, where b0 is the LSB and b7 is the MSB. A 2-bit BT decoder is used to transform 4-bit MSB bits into temperature codes once the 8-input bits are divided into two groups (4-bit binary and 4-bit unary). A 2-3 BT decoder converts bits [b7, b6] and [b5, b4] into thermometer code. Consequently, the three outputs from each decoder are used to control three rows and three columns of a local decoder.

An amalgam of binary and unary systems is the segmented architecture. The Binary weighted current steering DAC receives four bits and the Unary DAC receives four bits in the 4:4 segmentation proposed in this study. It is assumed that the segmented DAC's full scale voltage is 420 mV and its LSB current is 2 µA.

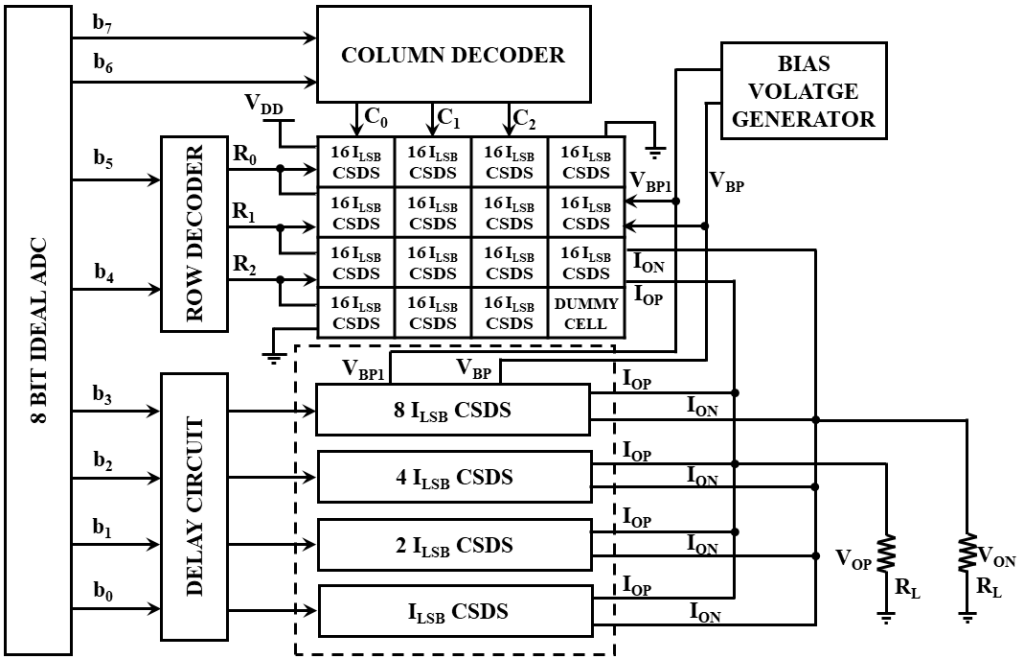


Figure 2. Architecture of the proposed 8-bit segmented CS-DAC

However, for the Unary weighted DAC, there's an additional circuitry introducing some delay. To counteract this delay and rectify timing disparities within the DAC, a delay circuit is implemented. This delay circuit, depicted in the Figure 2, is constructed using D-flip flops, effectively synchronizing the timing signals and ensuring proper alignment for seamless DAC operationIn Figure 2, we can see the 8-bit Segmented architecture.There are eight ILSB, four ILSB, two ILSB, and one ILSB current source with differential switching (CSDS) cells in the 4-bit binary CS-DAC unit. A parallel connection between two PMOS cascode current sources yields two times the ILSB current. Four times the ILSB current is obtained by connecting four PMOS cascode current sources in parallel. Similarly, for eight ILSB current sources, eight PMOS cascode current sources are connected in tandem. The error! There was no reference source found. Figure 2 depicts the CS-DAC, a 4-bit thermometer-coded device with 15 current cells and 16 x ILSB current per.

2.1. PMOS Cascode Current Source

In Figure 3, a pmos cascode current source structure design is displayed. Initially the circuit should be properly biased for the proposed current i.e., 2 µA. Here the critical factor that determines the load current is the precise configuration of biasing voltages. The two transistors' bias voltages are represented by the symbols Vcb and Vb in Figure 1, where Vb is the down transistor's gate voltage and Vcb is the top transistors.

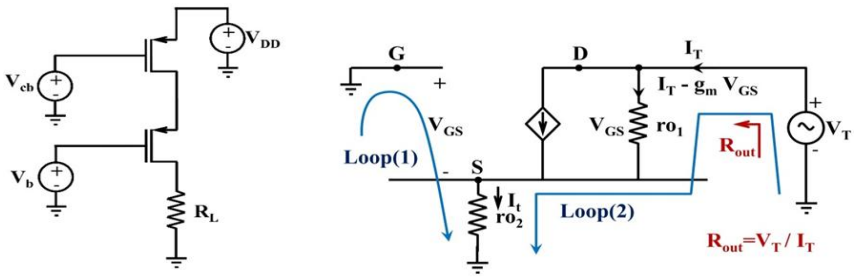


Figure 3. PMOS Cascode The current source and the model of its little signal

The output impedance is obtained from the cascode current mirror's small signal model as:

$KVL\ in\ loop\ (1): \quad -Vgs - Itro2 = 0$

$Vgs = -Itro2$

$KVL\ in\ loop\ (2): VT - (It - gm\,Vgs)\,ro1 - It\,ro2 = 0$

$VT - It\,(ro1 + ro2) + gmVgs\,ro1 = 0$

The output impedance R_{out} is obtained as $Rout = ro1 + (1 + gm1\,ro1)\,ro2$

2.2. Cascode Biasing Struture

The purpose of the Cascode biassing circuit is to solve the issues with direct biassing by biassing the Cascode current source. In Figure 4, the Cascode current source schematic with Cascode biassing is displayed.

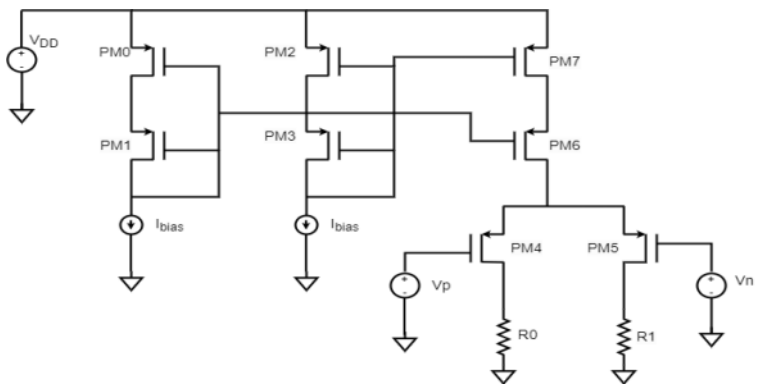


Figure 4. Circuit diagram for Cascode Biasing structure

3. CURRENT CELL

A Row-Column decoder is used to select the 15 current cells used by the 4-bit Unary weighted current steering DAC. This design adds a local decoder to the existing cell. As seen in Figure 5, the local decoder provides the binary data to the current cell. Additional pins for this circuit are R (row pin), C (column pin), and RN (row pin of previous cell) in the current cell design.

The 15 current cells of each producing 16 x I_{LSB} current specified for DAC i.e., 32 µA are arranged in a 4x4 array and the last current cell is a dummy current cell which is always in off state. The R, C and R_N pins of each current cell in array are controlled by row bits (R_0, R_1 and R_2) and Column bits (C_0, C_1 and C_2).

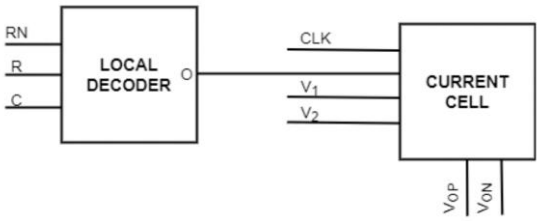


Figure 5. Current cell with local decoder

4. SIMULATION RESULTS

4.1. PMOS Cascode current source with Biasing circuit

Figure 6 displays the suggested cascode biassing structure's schematic design for the cascode current source for 2µA. The PVT analysis is done with the with fast-fast and slow-slow as it has only pmos transistors. And also, the temperature is varied from the -10 to 50 degrees. Constant voltages 800 mV and 700 mV were applied as biasing voltages to cascode current source and obtained an I_{LSB} current of 2.06 µA in nominal analysis, as shown in Table 1. However, I_{LSB} varies from 4.12 µA to 1.03 µA across the corners, resulting in more deviation from the nominal value. Designing a current cell for a DAC becomes impossible due to the increased nonlinearity. This can be modified by generating the biasing voltages from the cascode current mirror and applying it to the designed cascode current source. By using this, the obtained I_{LSB} current of 2.01 µA in nominal analysis and across the corners, I_{LSB} varies from 2.54 µA to 1.7 µA, as shown in Table 1. This deviation is in the acceptable range. The designed PMOS cascode current sources were biased using the cascode current mirror biasing circuit. From all the results obtained from the designed circuits for the current source and biasing networks as shown in the Table 1. The deviation of the load current is very less for the cascode biasing current source biased using current mirror.

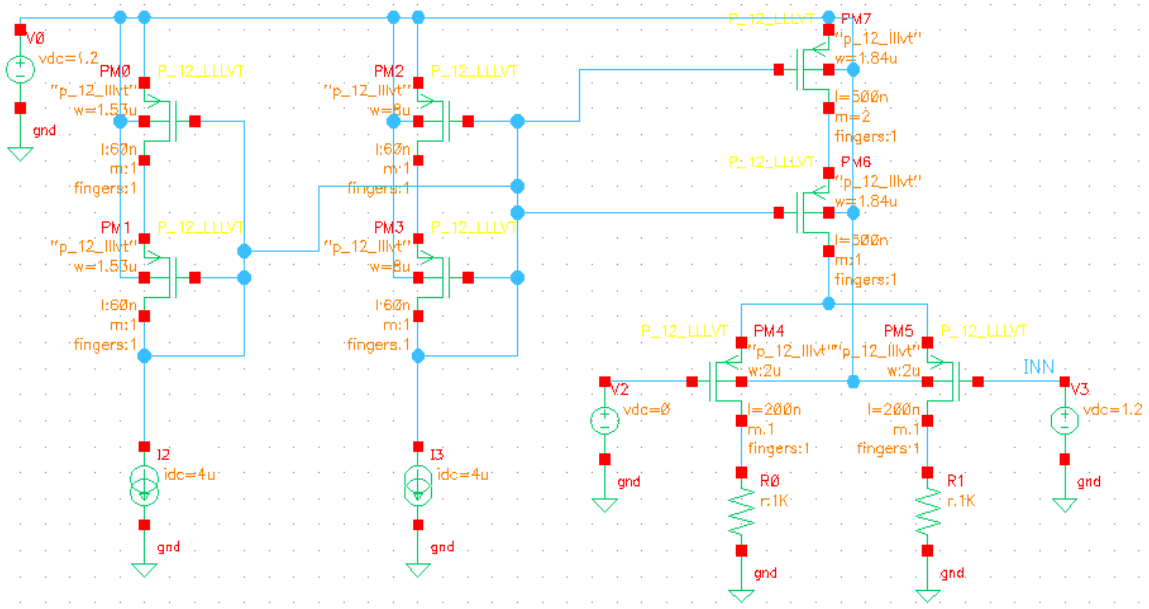


Figure 6. Schematic design of Cascode Biasing circuit

Table 1. Comparison between different Current sources

Design	Nominal Current (µA)	PVT analysis	
		Min (µA)	Max (µA)
Simple current source	1.96	0.71	4.69
Cascode current source	2.06	1.03	4.12
Cascode biasing current source	2.01	1.7	2.54

4.2. Monte carlo simulation for PMOS cascode current source

A Monte Carlo simulation for 200 samples analyzes the mismatch of the transistors for direct and cacode biasing, and Figure 7 shows the histograms for those results. For the direct biasing circuit, the mean current is obtained as 2.06 µA and standard deviation is 40.41 nA, for cascode biasing circuit the mean current is 2.01 µA and standard deviation is 73.89 nA.

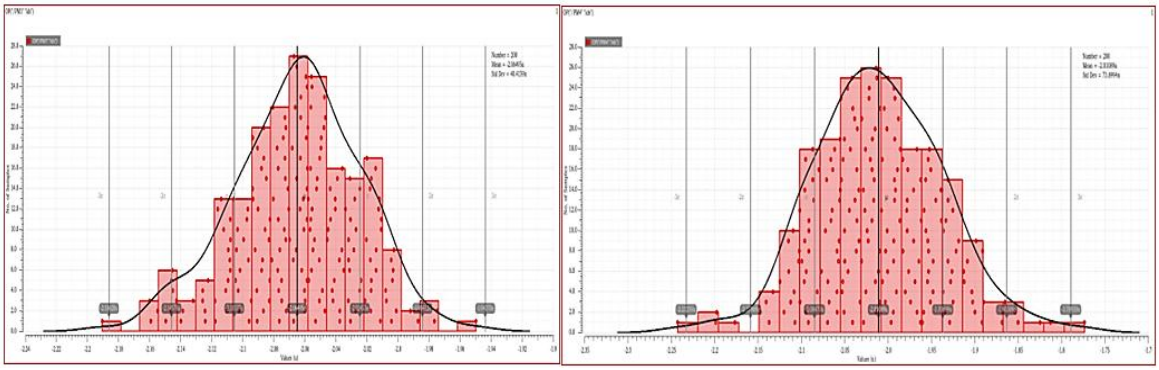


Figure 7. Cascode current source with direct and cascode biasing

4.3. 8-bit proposed segmented architecture

Figure 8 displays the 8-bit Segmented CS-DAC schematic design. The DAC is tested by giving a ramp signal to the ADC and the same ramp is observed at the DAC output. The designed DAC is operated at the frequency of 100 MHz. The differential output of the DAC for a given ramp signal is shown in Figure 9.

The transient simulation is performed for the designed circuit. The working of the DAC is tested with all the 256 different combinations of 8-bit binary data. The LSB voltage obtained from the DAC output is 1.66 mV and full scale voltage is 423 mV. The simulation result is shown in the Figure 9.

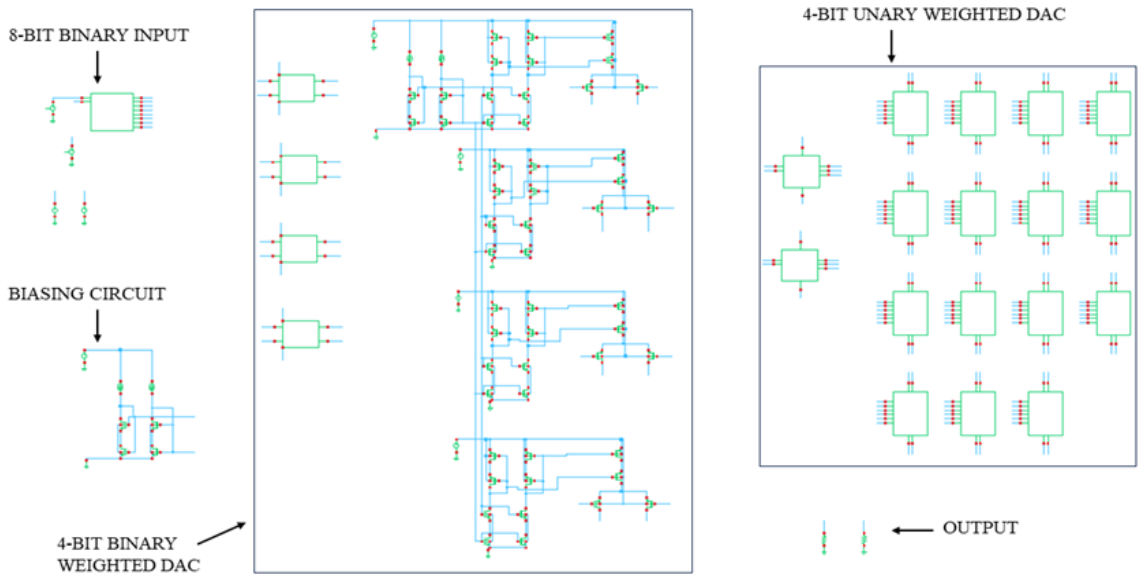


Figure 8. Schematic design of 8-Bit Segmented CS-DAC

A sinusoidal signal is also checked for in the DAC. To reconstruct the sine wave, the 8-bit ideal ADC receives a sine wave as input, and the planned 8-bit DAC receives the bitstream that is produced. The DAC's differential output for an AC signal is displayed in Figure 10.

Figure 11 displays the 8-bit segmented current steering DAC's performance metrics for the AC signal. For the intended 8-bit DAC, the ENOB (Effective Number of Bits) was 7.973 bits, or roughly 8. The SNR and SFDR obtained for the DAC, measuring 49.73 dB and 66.77 dB respectively, shows significant improvements compared to existing DAC designs. These metrics indicate the DAC's ability to operate effectively in the presence of noise, with higher SNR values representing better signal clarity and higher SFDR values indicating reduced spurious signals or distortions in the output.

The significant figures for the INL and DNL of a DAC are within ±1 LSB and ±0.5 LSB, respectively. However, the measured INL value is below ±0.4 LSB, and the DNL value is ±0.2 LSB. These results indicate superior performance of the designed 8-bit Current Steering DAC using a PMOS Cascode current source with cascode biasing. The complete segmented, binary and unary CS-DACs performance is shown in Table 2.

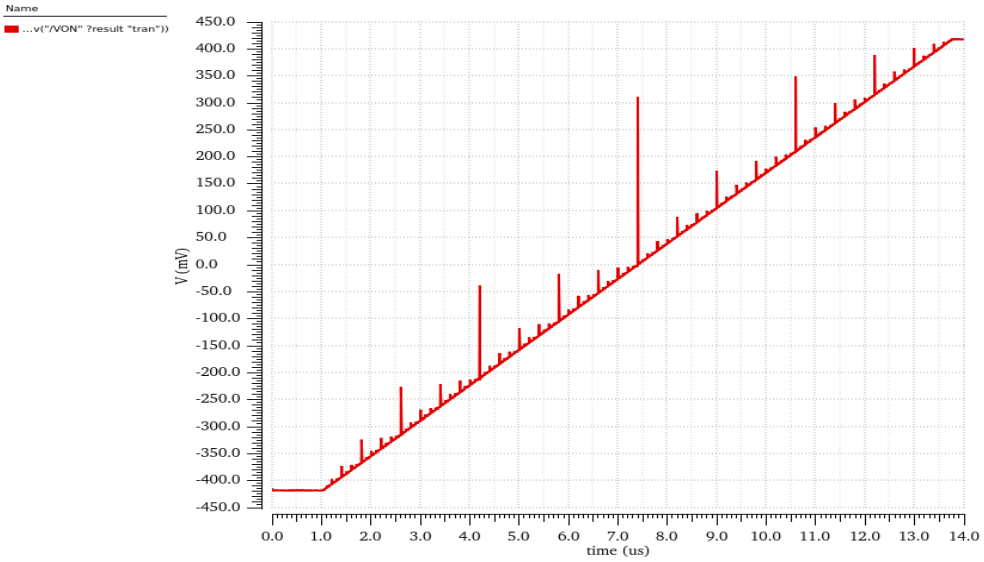


Figure 9. Differential output of 8-bit Segmented DAC for Ramp signal

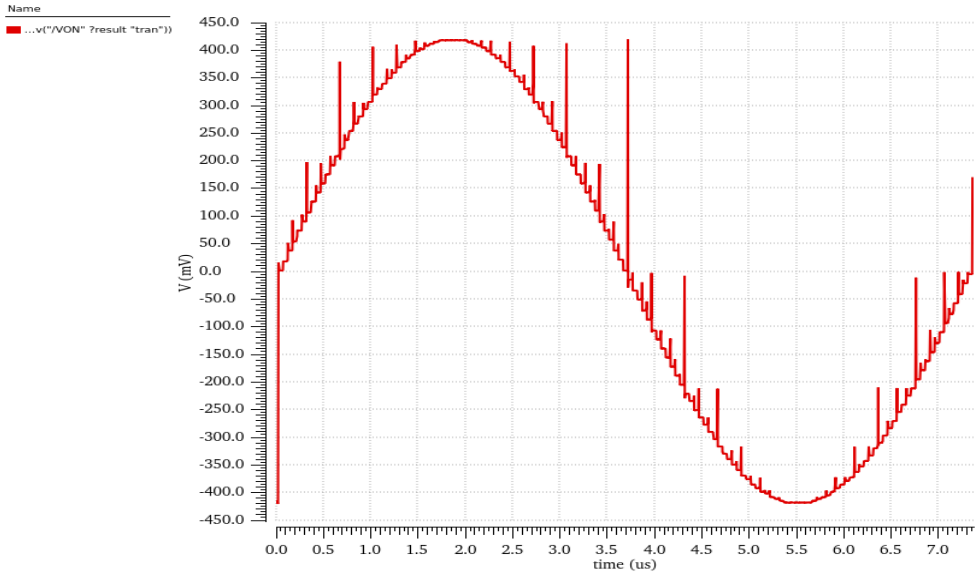


Figure 10. Differential output of 8-bit Segmented DAC for AC signal

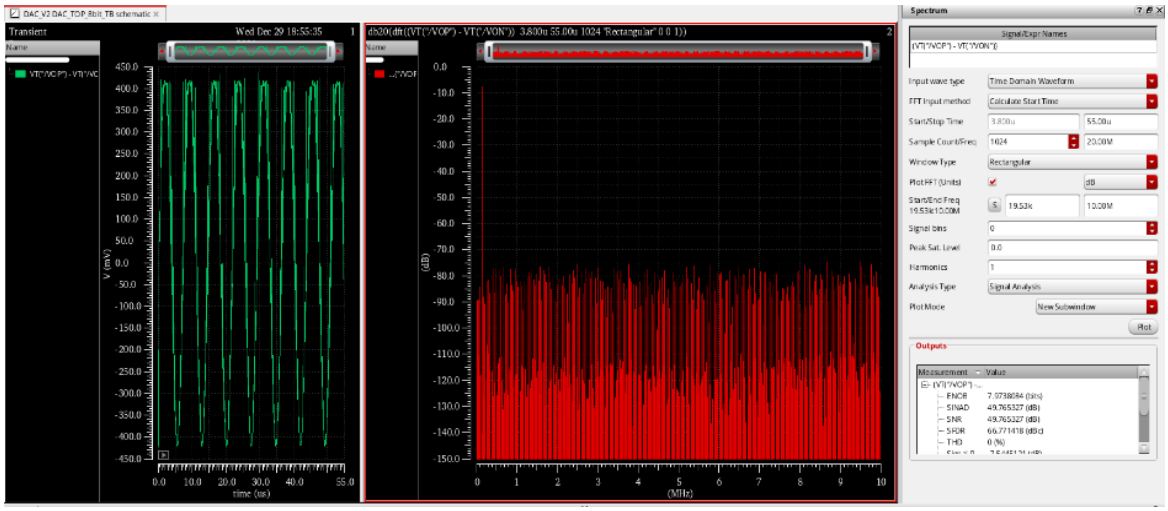


Figure 11. Performance metrices of designed 8-bit Segmented DAC

Table 2. CS-DAC performance summary

Parameters	Segmented (Proposed)	Binary	Unary
Process	65 nm	65 nm	65 nm
Resolution	8-bit	8-bit	8-bit
Sampling Frequency	100 MHz	100 MHz	100 MHz
V_{DD}	1.2 V	1.2 V	1.2 V
INL	0.4LSB	0.8LSB	0.3LSB
DNL	0.2LSB	0.6LB	0.2LSB
SFDR	66.7 dB	46 dB	65 dB
Output Swing	798 mV	780 mV	790 mV
ENOB	7.97	7.02	7.8

5. CONCLUSION

The conceptualisation of an 8-bit segmented CS-DAC that only requires two 2-bit BT decoders is presented in this work. By doing away with the latch and driver circuits that are usually found in traditional CS-DACs, this design reduces the size of the chip and uses less power. A 1.2 V supply voltage and 65nm CMOS technology were used to replicate this DAC. Each output of this differential DAC is connected to two resistors. several key components and functionalities have been addressed and analyzed. Firstly, a high-impedance current source has been designed and thoroughly analyzed, ensuring its efficacy in providing stable and reliable current outputs. Second, customised biassing circuits have been created to accommodate various current sources' load current needs. Each biasing circuit has been carefully designed and analyzed to optimize performance. Additionally, various digital blocks necessary for DAC design have been implemented, ensuring compatibility and seamless integration into the overall system architecture. Furthermore, both 4-bit unary and binary architectures have been meticulously designed and evaluated. These DACs serve as crucial building blocks for the subsequent development of the segmented DAC. Finally, the culmination of these efforts is the creation of a high-performance 8-bit segmented current steering DAC. This DAC has undergone thorough performance analysis to validate its functionality and effectiveness, ensuring it meets the requirements and specifications.

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