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Capacitor Voltage Balancing of Five Level Diode Clamped Converter based STATCOM

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Abstract

The power quality determines the fitness of the electrical power to the consumer devices. To improve the quality of the power delivered many compensating devices are used. The FACTS devices are normally used to reduce the power quality problems by inducing one or more AC transmission parameters. The static synchronous compensator (STATCOM) can act as either a source or sink of reactive AC power to an electricity network. The basic electronic block of the STATCOM is the voltage-source inverter that converts an input dc voltage into a three-phase output voltage. The STATCOM employs an inverter in order to obtain the voltage source of adjustable magnitude and phase from the DC link voltage on the capacitor. In this model, the STATCOM is designed with the five level diode clamped converter (DCC) controlled by space vector pulse width modulation (SVPWM) technique. The space vector technique with α, β frame is referred here. The dc link capacitor voltage equalization for the five level diode clamped converter was explained. The Total Harmonic Distortion of the source current will be considerably reduced.

Keywords: *Diode clamped converter, space vector pulse width modulation, Total Harmonic Distortion*

1. Introduction

The AC power transmission line operation is generally constrained by limitation of one or more network parameters which includes line impedance and operating variables such as voltages and currents. As a result, the power line is unable to direct power flow among generating stations. Therefore the transmission system has to be capable of transmitting the power generated with maximum efficiency. The major problem is with the quality of the power transmitted. The power quality depends upon various factors such as voltage, frequency and phase. Flexible AC Transmission System (FACTS) is the technology; its principal role is to enhance power transfer capability and controllability in AC power system. A static synchronous compensator (STATCOM) is a regulating device used on alternating current electricity transmission networks. It can act as either a source or sink of reactive AC power to an electricity network. It can be used for power quality improvement.

The multilevel inverters have drawn tremendous interest in the power industry. They provide a new set of features that are well suited for use in reactive power compensation. The concept of Multilevel Inverters (MLI) does not limit on just two levels of voltage to create an AC signal. Instead several voltage levels are added to each other in order to create a smoother stepped waveform, with lower dv/dt and lower harmonic distortions. With the more voltage levels, the waveform it creates becomes smoother, but with many levels the design becomes more complicated, with more components and complicated controller for the inverter is needed.

The STATCOM with Diode Clamped multilevel Converter using Space Vector Modulation is proposed and it can be used to improve the quality of the power delivered. Space vector modulation is a PWM control algorithm for multi-phase multi level inverters, in which the reference signal is sampled regularly; after each sample, non-zero active switching vectors adjacent to the reference vector and one or more of the zero switching vectors are selected for the appropriate fraction of the sampling period in order to synthesize the reference signal as the average of the used vectors.SVM is a digital modulation technique where the objective is to generate PWM load line voltages that are in average equal to a given or reference load line voltages. This is done in each sampling period by properly selecting the switch states of the

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inverter and the calculation of the appropriate time period for each state. The selection of the states and their time periods are accomplished by the space vector transformation. Capacitor voltage balancing with passive front ends is shown in [1], [6] and [8]. The sinusoidal PWM method for DCMC is given in [9]. Fast optimum predictive control for bipolar back to back converter can be seen in [2]. In [4] the capacitor voltage balancing is done with the help of current flow model. A elliptical reference frame space vector modulation is proposed here for the balancing of five level Diode clamped converter.

2. Multilevel SVPWM for DCMC based STATCOM

The multilevel converter can be connected to the power system for reactive power compensation. The load side is connected to the ac supply and the dc side is open, not connected to any dc voltage. For the control of reactive power flow, the inverter gate control is phase shifted by 180˚. The dc side capacitors act as a load. When a multilevel converter draws pure reactive power, the phase voltage and current are 90˚ apart, and the capacitor charge and discharge can be balanced.

2.1. Space Vector Modulation

Space Vector Modulation became a standard for the switching power converters. Any three-phase system (defined by $a_x(t)$, $a_y(t)$ $a_z(t)$) can be represented uniquely by a rotating vector a_S:

$$a_s=2/3[a_x(t)+a.a_y(t)+a^2.a_z(t)] \quad (1)$$

where, $\mathbf{a}=e^{j2\pi/3}$ and $\mathbf{a^2}= e^{j4\pi/3}$.

Given a three-phase system, the vectorial representation is achieved by the following 3/2 transformation:

$$\begin{bmatrix} A_\alpha \\ A_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} ax \\ ay \\ az \end{bmatrix} \quad (2)$$

where (A_α , A_β) are forming an orthogonal 2-phase system and $a_S = A_\alpha + j\ .A_\beta$. A vector can be uniquely defined in the complex plane by these components. $\mathbf{a}_x$ – can be a voltage, current or flux and does not necessarily has to be sinusoidal. It results an unique correspondence between a Space Vector in the complex plane and a three-phase system. The main advantages of this mathematical representation are:

- Analysis of three-phase systems as a whole instead of looking at each phase;
- It allows using the properties of the vectorial rotation. Using rotation with ωt leads to an analysis in DC components by withdrawing the rotational effect.

2.2. SVPWM for Five Level DCMC

Diode-Clamped Multilevel Converters (DCMCs) are one kind of multilevel converter for large scale and high voltage power conversions. Figure 1 shows the main circuit of a five-level DCMC. The converter with the other level structure has the similar circuits.

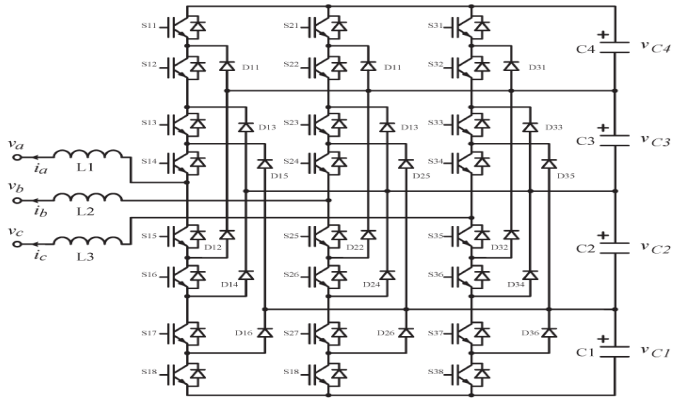

Figure 1. Structure of DCMC

No matter which level converter is used, the stabilization and equalization of dc-link capacitor voltages are important for both safe and normal operation of a DCMC. Due to the active power consumption and energy exchange between the dc-link capacitor and ac source, the unbalancing phenomenon of dc-link capacitor voltages will occurThe higher the level used in the DCMC is the more difficult the balance operation becomes. Particularly the stable area has a strict limit that the modulation index could not be higher than 0.55 approximately in active power conversion application.

3. System Configuration of STATCOM

The STATCOM is designed with the SVPWM technique to enhance the system stability by equalization of the DC link capacitor voltage. In the block diagram, the STATCOM is designed with the space vector pulse width modulation technique to control the diode clamped converter. The level of the diode clamped converter chosen is five. Here the GTO (Gate turn Off Thyristor) to control the injected current or the compensating voltage. DC link capacitance value has to be chosen. The number of the switching devices in the DCMC and the number of the capacitors are decided by the level of the inverter chosen. With higher amounts of voltage levels, the number of diodes grows quadratically with the level m following the equation (m - 1) * (m - 2).

A constant source is connected to the load through the converter/inverter circuit. The inverter block is made of IGBT (Gate-insulated bipolar transistors). To provide proper quality of power to the load and also to reduce the harmonics the STATCOM is connected as the shunt compensating device. STATCOM connected will provide compensation current for the equalization of the voltage quality. Therefore the current harmonics can be eliminated. The injection of the current depends upon the switching sequence of the diode clamped converter which is given by the space vector modulation technique.

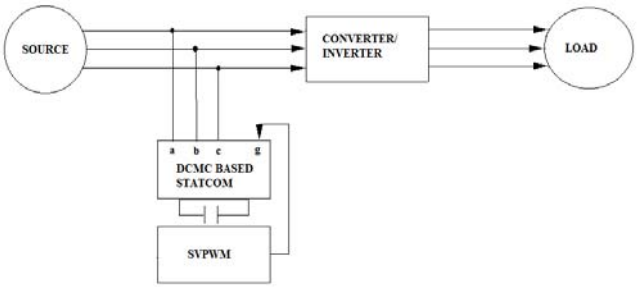

Figure 2. Block Diagram of STATCOM

3.1. System Configuration

As in the block diagram of the system, each block is designed and the system is formed. The source block is a three phase voltage source of 160*sqrt (3) i.e approximately 220 volt phase to phase rms was chosen for the operation. The operating frequency of the system is 50 Hz. The load is resistive nature. The voltage of the load is similar to the source voltage and the power rating of the load is decided as 15 kW. The load is connected with the source through converter inverter block.

The rectifier block is the three phase uncontrolled rectifier. The diode is used as switching device. The DC output of the rectifier is given to the LC circuit. Since IGBT devices are used in the three phase inverter, the generation of gate pulse is required. The method used for the triggering of the inverter is pulse width modulation. In the PWM technique for gate pulse generation the voltage regulator block and the Discrete PWM blocks are employed. The voltage regulator block has the proportional gain of 0.4 and integral gain of 500. The carrier frequency of the Discrete PWM generator is selected as 2000 Hz. The sampling time for the generation of the PWM is chosen as 0.1 μs.

The STATCOM model is connected to the system in shunt. The blocks of the STATCOM can be separated to DCMC block and gate generation block. The voltage maintained across the capacitor is 10 V. The switching method used for the switching of the GTOs is SVPWM. The frequency of operation is 50 Hz. The voltage level is 5. The operating voltage of the SVPWM technique is specified as 440 V and current value as 10 A.

3.2. Modulation of DCMC

In the DCMC topology the use of voltage clamping diodes is essential. A common DC-bus is divided by an even number, depending on the number of voltage levels in the inverter, of bulk capacitors in series with a neutral point in the middle of the line. From this DC-bus, with neutral point and capacitors, there are clamping diodes connected to an m-1 number of valve pairs, where m is the number of voltage levels in the inverter (voltage levels it can generate).

3.3. Selective Harmonic Elimination

Selective Harmonic Elimination (SHE) is a low switching frequency strategy that uses calculated switching angles to eliminate certain harmonics in the output voltage. With the help of Fourier Series analysis the amplitude of any odd harmonic in the output signal can be calculated. The switching angles must however be lower than π/ 2 degrees and for a number of switching angles harmonic components can be affected, where a-1 number of harmonics can be eliminated (one angle to set the fundamental). If angles were to be larger than π/2 a correct output signal would not be achievable. For an inverter with m levels a = m-1/2. Higher harmonics can be filtered out with additional filters added between the inverter and the load if needed. For a five-level inverter a = 2, so there are two switching angles available and a - 1 = 1 angles can be used for harmonic component elimination.

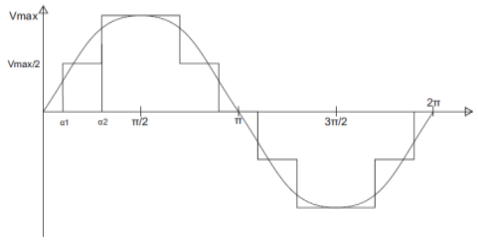

Figure 3. Switching with angles determined by Selective Harmonic Elimination for a Five-level inverter

3.4. Power Losses

Loss is an important aspect of power electronics since lower losses gives higher efficiency. Since the multilevel inverters can operate at different switching frequencies and with different balancing control schemes they will not have the same amount of power losses. To be

able to investigate the switching losses in an inverter a model for losses is needed. The switching power loss P_{sw} during one second in a switch is defined by the formula

$$\mathbf{P_{sw} = \Sigma\ ½\ V_d\ I_o\ I_t} \quad (3)$$

There V_d is the voltage over the switch when off, I_0 is the current through the switch after turned on or before turned off and t is either the turn on time ton or the switch off time t_{off}. The sum of all the switching loss event energies during one second for one switch results in that switch's switching power loss.

4. Operation of STATCOM

4.1. Operation of DCMC

In the DCMC topology the use of voltage clamping diodes is essential. A common DC-bus is divided by an even number, depending on the number of voltage levels in the inverter, of bulk capacitors in series with a neutral point in the middle of the line. From this DC-bus, with neutral point and capacitors, there are clamping diodes connected to an m-1 number of valve pairs, where m is the number of voltage levels in the inverter (voltage levels it can generate). With this configuration five levels of voltage can be generated between point a and the neutral point n; Vdc/2 , Vdc/4 , 0,-Vdc/4 and –Vdc/2 , depending on which switches that are switched on. With a higher number of voltage levels the complexity of the inverter increase. From Table 1 it can be seen that for the voltage $V_{dc}/2$ all the upper switches are turned on, connecting point a to the $V_{dc}/2$ potential. For the output voltage $V_{dc}/4$ switches S_2, S_3,S_4 and S_1 are turned on and the voltage is held by the help of the surrounding clamping diodes D_1 and $D`_1$. For voltage levels $–V_{dc}/4$ or $-V_{dc}/2$ clamping diodes $D_2$ and $D`_2$ or D_3 and $D`_3$ hold the voltage, respectively. For the voltages ±Vdc/2 the current, when both voltage and current are positive goes through the four top or bottom switches. For the other states positive current, while voltage is positive, goes through the $D_x$ diodes and negative current through the $D`_x$ diodes and also through the switches in between the clamping diodes and the load

Table 1. Switching states of one five-level phase leg '1' means turned on and '0' means turned off

Output Voltage	S_1	S_2	S_3	S_4	$S_1`$	$S_2`$	$S_3`$	$S_4`$
Vdc/2	1	1	1	1	0	0	0	0
Vdc/4	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
-Vdc/4	0	0	0	1	1	1	1	0
$-V_{dc}/2$	0	0	0	0	1	1	1	1

If there is a DC-source charging the DC-bus there are also currents flowing through the DC-bus to keep the DC-bus voltage constant. Table 5.1 also shows that some switches are on more frequently than others, mainly $S_4$and $S`_1$, as long as a sinusoidal output wave that requires the use of all voltage levels is created. When the inverter is transferring active power this leads to unbalanced capacitors voltages since the capacitors are charged and discharged unequally, partly due to different workloads.

4.2. Vector Representation

The first step in the algorithm is to transform the reference vector *V*ref (*a, b, c*) = [*Va, Vb, Vc*] into 2-D *α, β* coordinate. As is well known, the voltage vector in the *abc* frame is transferred into 2-D the *αβ* frame as

$$\begin{bmatrix} V\alpha \\ V\beta \\ Vo \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & \sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix}\begin{bmatrix} Va \\ Vb \\ Vc \end{bmatrix} \quad (4)$$

That is, $V\alpha = Va - Vc$, and $V\beta = -Va + Vb$. obviously, the calculation is a simple integral transformation. Assuming that the voltages have a form with the polar geometry as Vref = [Vr sin ωt, Vr sin($\omega t - 2\pi/3$), Vr sin($\omega t + 2\pi/3$)], the substitution of these expressions in yields,

$$\frac{(V\alpha + V\beta)^2}{\left(\frac{\sqrt{3}Vr}{Vdc}\right)^2} + \frac{(V\alpha + V\beta)^2}{\left(\frac{3Vr}{Vdc}\right)^2} = 1 \quad (5)$$

where Vdc is the voltage of the dc-link capacitor. Equation (3) is a standard elliptic equation. That is to say, a circular trajectory of Vref in the traditional $\alpha\beta$ coordinate will be transformed into an elliptical trajectory in the $\alpha\_\beta\_$ coordinate.

Assuming that floor ($*$) presents the operation that rounds each element of the input signal to the nearest integer value toward minus infinity, the vertex of $V1(\alpha1, \beta1)$ could be calculated as

$$\alpha1 = \text{floor}(V\alpha) \quad \beta1 = \text{floor}(V\beta) \quad (6)$$

Thus, the adjacent vertices $V2(\alpha2, \beta2)$, $V3(\alpha3, \beta3)$, and $V4(\alpha4, \beta4)$ could be fast ascertained as

$(\alpha2, \beta2) = (\alpha1 + 1, \beta1)$ $(\alpha3, \beta3) = (\alpha1, \beta1 + 1)$ $(\alpha4, \beta4) = (\alpha1 + 1, \beta1 + 1)$

The vertices of V1, V2, and V3, the minimum downward triangle, where V_{ref} is located in $\Delta_{1\,2\,3}$. Certainly, V_{ref} locating in the upward triangle $\Delta_{3\,4\,5}$ will be presented by the other three vertices V_2 , V_3 , and V_4. Whether V_{ref} is locating in the downward or upward triangle could be determined by the following criterion:

$$\alpha + \beta \leq \alpha_1 + \beta_1 + 1, \quad V_{ref} \quad (7)$$

$$\alpha + \beta > \alpha_1 + \beta_1 + 1, \quad V_{ref} \quad (8)$$

Obviously, it is also a simple algorithm for digital implementation.

4.3. Dwelling Time Calculation

Assuming that Vref does not change its amplitude in one module period Ts, its average effect in one module period might be equivalent to the three most adjacent vectors with respective dwelling times as

$$V\text{ref}\ Ts = V1T1 + V2T2 + V3T3, \text{ if } V\text{ref in } \Delta123 \text{ or} \quad (9)$$

$$V2T2 + V3T3 + V4T4, \text{ if } V\text{ref in } \Delta\ 234 \quad (10)$$

Because $T1 + T2 + T3 = Ts$, the dwelling time when Vref is locating in _123 could be obtained as,

$$\begin{cases} T2 = (\alpha - \alpha1)\ Ts \\ T3 = (\beta - \beta1)\ Ts \\ T1 = Ts - T2 - T3 \end{cases} \quad (11)$$

If Vref locates in $\Delta234$, the calculations become

$$\begin{cases} T2 = (\beta1 + 1 - \beta)\ Ts \\ T3 = (\alpha1 + 1 - \alpha)\ Ts \\ T4 = Ts - T2 - T3 \end{cases} \quad (12)$$

Therefore, the basic processing of dwelling time and location criterion are all simplified. Once the T_s are normalized by the system clock period, all of these equations could be realized by fast calculations, such as addition, subtraction, comparison, and truncation, which are time and area efficient in digital fixed-point application.

4.4. Minimum Energy Property

Assuming that all dc-link capacitors of the *n*-level DCMC have the same capacitance and voltage, the mathematical conditions are

$$C1 = C2 = \cdots = Cn = C$$
$$VC1 = \cdots = VCn-1 = V\text{dc}/(n-1) \quad (13)$$

The total energy stored in the capacitors would reach the minimum value when their voltages are balanced

$$E = \frac{1}{2}\sum_{i=1}^{n-1} C_i V_{Ci}^2 \Big|_{\substack{C_1=\cdots=C_{n-1}=C \\ V_{C1}=\cdots=V_{Cn-1}=\frac{V_{\text{dc}}}{(n-1)}}} = \frac{CV_{\text{dc}}^2}{2(n-1)} \quad (14)$$

Define a positive-definite cost function *J* to indicate the energy drift from the minimum

$$J = \frac{1}{2}C\sum_{i=1}^{n-1} \Delta V_{Ci}^2 \quad (15)$$

Where,

$$\Delta V_{Ci} = V_{Ci} - \frac{V_{\text{dc}}}{(n-1)} \quad (16)$$

which is the voltage deviation of capacitor *Ci*. If a definite negative Δ*J* could be guaranteed through the proper PWM outputs, the voltages would fluctuate toward the balanced values. That is

$$\frac{dJ}{dt} = C\sum_{i=1}^{n-1} \Delta V_{Ci}\frac{dV_{Ci}}{dt} = C\sum_{i=1}^{n-1} \Delta V_{Ci} i_{Ci} \leq 0 \quad (17)$$

where *iCi* is the current charge into capacitor *Ci*. This condition is called the minimum energy property for a balanced *n*-level DCMC. It could be used as the basic principle for dc-capacitor voltage balancing and control.

5. Simulation and Results

To verify the above design and analysis, a simulation model was designed using Mat lab\Simulink. A load of 15 kW is set. The load will be activated at 0.02s. The values of current, voltage can be varied with the connection of the STATCOM. The simulation results are shown in Figure 4. The Simulink model was designed with the configuration mentioned. The generation of gate pulse is done with the help of SVPWM method. The reference signal is formed and then it undergoes transforms to calculate the sample time. The respective Simulink output waveforms for the given model are shown in figures 4 to 8.The analysis of total harmonic distortion was done for the source current. The IEEE standard for the THD is below 5%. The obtained THD level is 2.61%. This is shown in the figure 8. Initially the load is not connected to the system. With the connection of the load with the circuit after 0.1 s the change in current and the voltage values are noted.

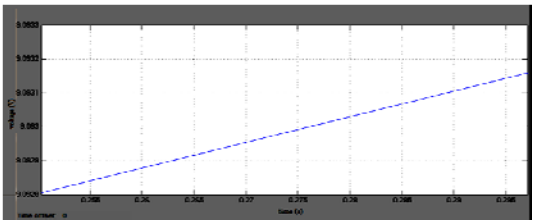

Figure 4. Voltage waveform across the capacitor

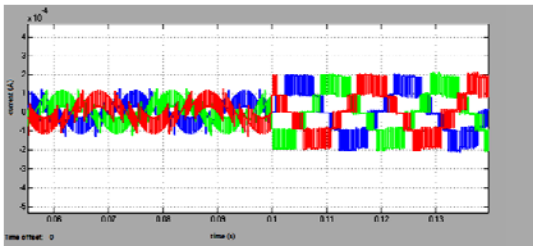

Figure 5. Compensation current from the STATCOM

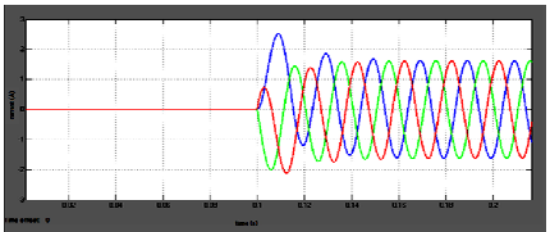

Figure 6. Waveform of the source current

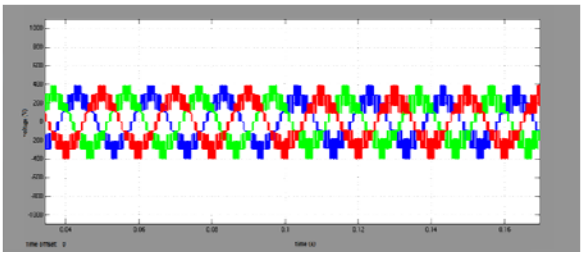

Figure 7. Output voltage waveform of the STATCOM

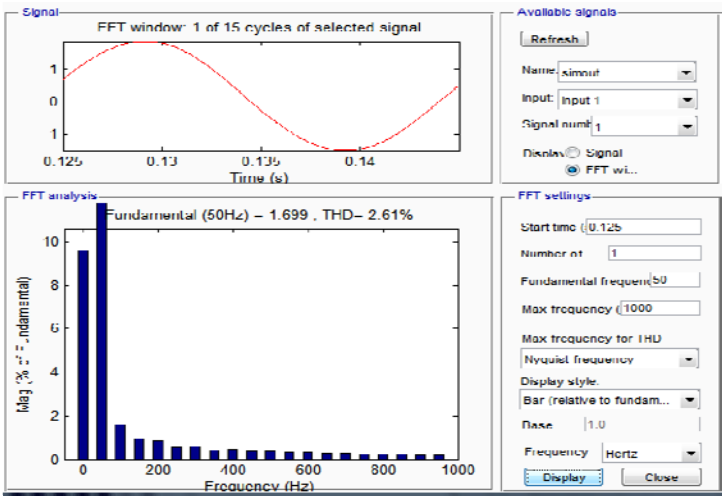

Figure 8. THD analysis of source current

6. Conclusion

DCMC can be used in reactive power compensation without voltage unbalance problem and have a common DC-bus and are possible in back-to-back configurations. With aspect to industrial popularity, design simplicity, suitability for back-to-back and reactive power compensation the DCMC have been chosen for simulation for the Electric Grid System case in this work. With the proposed SVPWM control method in and the capacitor voltage unbalance can be controlled which makes the DCMC an attractive choice. This paper presents an SVPWM algorithm in the αβ frame with dc-link capacitor voltage balancing control for diode clamped multilevel STATCOM. The five-level converter generates almost sinusoidal voltage and current waveforms even at fundamental switching frequency. The dc link capacitors voltages are well balanced with very small ripple. The system has low harmonics in the input current. Each switch in the converter can switch only once per cycle when performing fundamental frequency

switching which will results in high efficiency. Simulation results conclude that the proposed SVM strategy is able to carry out the voltage-balancing task, with no requirement for additional power circuitry, within the specified range of operation.

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