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Analysis of VFDPC for three-level neutral point clamped AC-DC converters with capacitor balancing solution

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ABSTRACT

This paper presents an analysis of the dynamic performance of a three-level neutral point clamped (NPC) AC-DC converter utilizing the advanced control technique of virtual flux direct power control (VFDPC). VFDPC estimates the three-phase grid voltage and instantaneous active and reactive power components, eliminating the need for an AC input voltage sensor used in conventional direct power control (DPC). This reduction in sensors decreases system complexity and cost while mitigating high-frequency noise and interference. Integrating VFDPC into 3L NPC AC-DC converters significantly enhances overall performance, leading to more efficient and robust power conversion systems. However, a significant challenge in the three-level NPC topology is the voltage imbalance in the neutral point of the DC-link capacitor, which can cause excessive voltage stress on switching devices and degrade system performance. To address this, a novel lookup table has been developed, incorporating strategies to balance the capacitor voltage. The results of this study demonstrate that VFDPC generates nearly sinusoidal line currents with reduced current total harmonic distortion (THD). Additionally, VFDPC ensures unity, lagging, and leading power factor operation, while providing flexibility to adjust the DC-link output voltage and accommodate load variations. These capabilities highlight VFDPC effectiveness in managing power quality and system stability, even under varying load conditions.

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1. INTRODUCTION

In modern electrical systems, the demand for efficient and reliable power conversion is increasing. Among the various converter topologies, Three-level neutral point clamped (3L NPC) AC-DC converters stand out due to their high efficiency, reduced harmonic distortion, and enhanced power handling capabilities [1], [2]. These attributes make this topology particularly suitable for applications requiring high power and precision, such as industrial drives, renewable energy systems, and grid-connected converters [2], [3]. The ability of 3L NPC converters to operate at higher voltages and power levels while maintaining low harmonic distortion is indispensable in high-demand environments [4]. Furthermore, the capability to reduce the size and cost of passive components, such as filters, enhances the appeal for large-scale industrial applications [5].

However, maintaining voltage balance across the dc-link capacitors in 3L NPC converters is a significant challenge and have been received a large amount of attention in recent decade [6], [7]. Voltage imbalances can lead to increased stress on power semiconductors, higher losses, and potential system instability [8], [9]. Therefore, balancing the dc-link capacitor voltage in 3L NPC converters is crucial for maintaining system stability and performance, while various strategies have been developed to address this challenge. For instance, Sinusoidal pulse width modulation (SPWM) attempts to achieve neutral-point balance by injecting a zero-sequence signal into the modulation signal. However, this approach is often ineffective under dynamic load conditions, leading to instability and low-frequency oscillations in capacitor voltages [10], [11]. Similarly, space vector modulation (SVM) uses redundant switching states to control capacitor voltages, but its effectiveness is limited by the complexity and computational demands of the algorithm [12], [13]. Other methods, like selective harmonic elimination PWM (SHE-PWM), target specific harmonics by solving non-linear equations for switching angles. Although SHE-PWM can improve voltage balance, the complexity of real-time calculations often limits its effectiveness, particularly in high-power applications [14], [15]. In high-speed applications, virtual space vector modulation (VSVPWM) can reduce switching losses but struggles with the complexity of real-time vector adjustments, leading to potential delays in voltage balancing [16].

Virtual flux direct power control (VFDPC) emerges as a robust solution [17], [18] to these challenges. Unlike traditional strategies [19], VFDPC directly controls the power flow through the converter, stabilizing the neutral point voltage without relying on complex modulation or predictive models. Integrating a capacitor balancing solution within the VFDPC framework is crucial for the stable operation of 3L NPC converters. The capacitor balancing algorithm works by adjusting the redundant switching states to ensure even voltage distribution across the DC-link capacitors [20]. This approach helps to mitigate the adverse effects of voltage drifts and ripples at the neutral point, ensuring consistent and balanced operation [21]. By maintaining the voltage balance, the converter can operate more efficiently and reliably, reducing stress on the components and extending their lifespan. This integrated approach addresses the key issues that traditional control strategies struggle with, providing a comprehensive solution for high-power applications.

The findings from this paper indicate that implementing VFDPC with a capacitor balancing solution significantly improves the performance and reliability of 3L NPC converters [22]. The VFDPC method provides precise control over power flow, effectively maintains capacitor voltage balance, and reduces the voltage stress on power semiconductors. This leads to lower switching losses, enhanced system stability, and a more robust performance in high-power applications. By addressing the technical challenges associated with voltage balancing and power control, this study contributes to the advancement of multilevel converter technology. The enhanced performance and reliability of 3L NPC converters with VFDPC make them an attractive option for demanding applications, paving the way for more efficient and reliable power conversion in modern electrical systems.

2. MODELLING

Figure 1 shows the topology of a grid-connected 3L-NPC AC-DC converter with an L-type filter. The converter consists of twelve switching cells and six clamp diodes. Any given output phases of the converter can be connected to the negative (S_{a1}=0, S_{a2}=0), neutral ((S_{a1}=0, S_{a2}=1), or positive (S_{a1}=1, S_{a2}=1) points of the dc-link, which results in a different current path between the DC side and AC side.

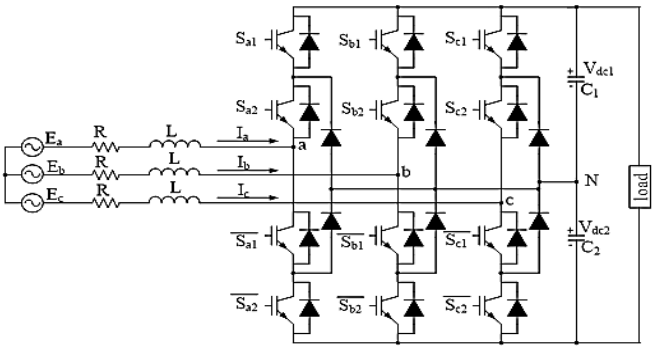


Figure 1. NPC converter topology

At the dc-link side, two capacitors are connected in series to form a neutral point *N*. The diodes D_{z1}, and D_{z2} are connected to the neutral point, *N* is the clamping diodes. When switching $S_{a\,2}$ and $\bar{S}_{a1}$ are turned

on, the converter input terminal *a* is connected to the neutral point through one of the clamping diodes. The voltage across each of the DC capacitors is $V_{dc}/2$, which is normally equal to half of the total DC voltage Vdc. With a finite value for C_1 and C_2, the capacitor can be charged or discharged by neutral current, causing neutral-point voltage deviation. The switches S_{a1}, S_{a2} , $\bar{S}_{a1}, \bar{S}_{a2}$, S_{b1} , S_{b2} , $\bar{S}_{b1}$, $\bar{S}_{b2}$, S_{c1}, S_{c2} and $\bar{S}_{c1}, \bar{S}_{c2}$ are complimentary in operation. Next, the switching state definitions in NPC are shown in Table 1. The term *[P]* denotes that the upper two switches in leg *A* are turned on. *[O]* indicates the inner two switches S_{a2} and $\bar{S}_{a1}$ are on, while S_{a1} and $\bar{S}_{a2}$ are operate in a complementary manner.

Table 1. Switching states for NPC

Switching state	Switching status (phase A)			
	S_{a1},	S_{a2}	S_{a1},	S_{a2}
P	ON	ON	OFF	OFF
O	OFF	ON	ON	OFF
N	OFF	OFF	ON	ON

The three-phase 3L NPC has a total of 27 combinations of switching states as can be seen in the voltage vectors [23]. Those vectors are arranged into four categories, as given in Table 2. The 27 switching states listed in the table correspond to 19 voltage vectors that are based on their magnitude (length) compute the vector representation in the space vector [24]. The the sub-index *L*, *M*, and *S* are related to large, medium, and small vectors as illustrated in Figure 2 [25].

Table 2. Different switching states of three-level converters

Switching states	Vector classification	Vector magnitude
V0(PPP,NNN,OOO)	Zero vector	0
VS_1(POO/ONN) ;VS_2(PPO/OON)	Small vector	1/3Vd
VS_3(OPO/NON) ; VS_4(OPP/NOO)		
Vs_5(OPP/NNO) ; VS_6(POP/ONO)		
VM_1(PON) ; VM_2(OPN);VM_3(NPO)	Medium vector	$\sqrt{3}$/3Vd
VM_4(NOP) ;VM_1(ONP) ; VM_6(PNO)		
VL_1(PNN) ; VL_2(PPN) ; VL_3(NPN)	Large vetor	2/3Vd
VL_4(NPP) ; VL_5(NNP) ;VL_6(PNP)		

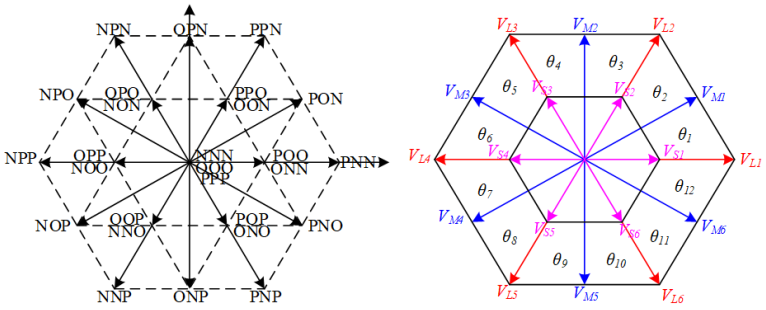


Figure 2. Sector decomposition of three-level space vector diagram

3. THREE-LEVEL NPC VIRTUAL-FLUX DIRECT POWER CONTROL (3L NPC VFDPC)

The block diagram of the proposed VFDPC in NPC AC-DC converters is shown in Figure 3. It is apparent to see that the voltage sensor has been eliminated. The virtual flux concept for multilevel converters NPC topology the converter pole voltage, $V_{con,an}$, $V_{conv,bn}$, and $V_{conv,cn}$ can be obtained by using the input from the switching states of the converters, $S_{a1,b1,c1}$, $S_{a2,b2,c2}$ and capacitor voltages, v_{dc1}, v_{dc2} from upper and lower. Then, the converter pole voltage, $V_{con,an}$, $V_{conv,bn}$, and $V_{conv,cn}$ has been transformed from the *abc*-reference frame into the *αβ*-reference frame using Clark-transformation. The input from grid virtual flux and current from alpha-beta reference-frame are used to measure the instantaneous active P_{inst} and reactive power Q_{inst}. Meanwhile, the reference active power P_{ref} is produced by multiplying the DC-link output voltage V_{dc} with the output signal from the PI controller while the reference reactive power Q_{ref} is set to zero to demonstrate a unity power factor operation. Subsequently, the command active power P_{ref} and reactive power Q_{ref} values are subtracted with calculated active and reactive power to produce the instantaneous active power error and

reactive power error denoted by ΔP and ΔQ respectively. The error signals are processed by two hysteresis controllers to produce the power error status signals shown by d_P and d_Q. By using the information of power error status and the increasing or decreasing of v_{dc1} and v_{dc2}, the hysteresis controller produces an output signal which is known as a balancing status B_s.

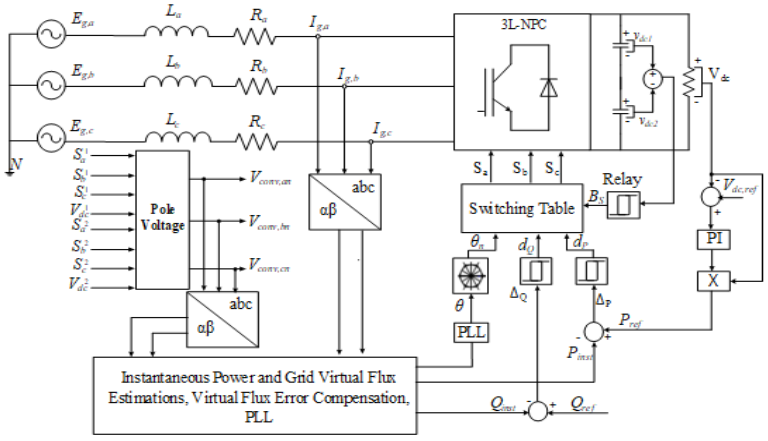


Figure 3. Block diagram for 3L NPC VFDPC

With the balanced three-phase input voltages and currents, the input complex power in a stationary reference frame can be written as:

$$S_{in} = \frac{3}{2}\bar{E}_{g,\alpha\beta}\bar{I}^{*}_{g,\alpha\beta} \tag{1}$$

the derivation of input instantaneous active and reactive powers in a stationary $\alpha\beta$-reference frame is performed by applying the virtual flux differentiating equation to the complex power of (1). The derivation procedure is as follows:

$$\begin{aligned}
S_{in} &= \frac{3}{2}\bar{E}_{g,\alpha\beta}\bar{I}^{*}_{g,\alpha\beta} \\
&= \frac{3}{2}\left\{\left(\frac{d}{dt}(\bar{\psi}_{g,\alpha\beta})\right)\bar{I}^{*}_{g,\alpha\beta}\right\} = \frac{3}{2}\left\{|\bar{\psi}_{g,\alpha\beta}|\left(\frac{d}{dt}(e^{j\omega t})\right)\bar{I}^{*}_{g,\alpha\beta}\right\} \\
&= \frac{3}{2}\left\{(j\omega|\bar{\psi}_{g,\alpha\beta}|e^{j\omega t})\,\bar{I}^{*}_{g,\alpha\beta}\right\} = \frac{3}{2}\left\{j\omega\left(\psi_{g,\alpha}+j\psi_{g,\beta}\right)\left(I_{g,\alpha}-jI_{g,\beta}\right)\right\} \\
&= \frac{3}{2}\left\{j\omega(\psi_{g,\alpha}I_{g,\alpha}+j\psi_{g,\beta}I_{g,\alpha}-j\psi_{g,\alpha}I_{g,\beta}+\psi_{g,\beta}I_{g,\beta})\right\} \\
&= \frac{3}{2}\left\{j\omega(\psi_{g,\alpha}I_{g,\alpha}+\psi_{g,\beta}I_{g,\beta})-j\left(\psi_{g,\beta}I_{g,\alpha}-\psi_{g,\alpha}I_{g,\beta}\right)\right\} \\
&= \frac{3}{2}\omega\left\{(\psi_{g,\alpha}I_{g,\beta}-\psi_{g,\beta}I_{g,\alpha})+j\left(\psi_{g,\alpha}I_{g,\alpha}+\psi_{g,\beta}I_{g,\beta}\right)\right\}
\end{aligned} \tag{2}$$

where $E_{g,abc}$is the three-phase voltage supply, $I_{g,abc}$ is the three-phase line current, and $V_{conv,abc}$is the three-phase converter pole voltage. Then, the phase voltages at the poles for each phase of the converter are equal as in (3) to (6) where $S_{a,b,c}$ the switching state of the converter is and V_{dc} is the link-output voltage.

$$\begin{bmatrix}E_{g,a}\\E_{g,b}\\E_{g,c}\end{bmatrix} = R\begin{bmatrix}I_{g,a}\\I_{g,b}\\I_{g,c}\end{bmatrix} + L\frac{d}{dt}\begin{bmatrix}I_{g,a}\\I_{g,b}\\I_{g,c}\end{bmatrix} + \begin{bmatrix}V_{conv,a}\\V_{conv,b}\\V_{conv,c}\end{bmatrix} \tag{3}$$

$$V_{conv,an} = \frac{2S_{a1}-(S_{b1}+S_{c1})}{3}V_{dc1} + \frac{2S_{a2}-(S_{b2}+S_{c2})}{3}V_{dc2} \tag{4}$$

$$V_{conv,bn} = \frac{2S_{b1}-(S_{a1}+S_{c1})}{3}V_{dc1} + \frac{2S_{b2}-(S_{a2}+S_{c2})}{3}V_{dc2} \tag{5}$$

$$V_{conv,cn} = \frac{2S_{c1}-(S_{a1}+S_{b1})}{3}V_{dc1} + \frac{2S_{c2}-(S_{a2}+S_{b2})}{3}V_{dc2} \tag{6}$$

next, any three-phase electrical quantities in *abc*-coordinates which are defined by $x_{a,b,c}$ can further be transformed into stationary $\alpha\beta$-coordinates by using the transformation matrix.

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \sqrt{\frac{3}{2}} & -\sqrt{\frac{3}{2}} \end{bmatrix}\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix}$$

the grid virtual flux vector in a stationary frame $\overline{\Psi}_{g,\alpha\beta}$ is defined as the integration of the grid voltage vector in a stationary reference frame $\overline{E}_{g,\alpha\beta}$ as shown in (7):

$$\psi'_{conv,\alpha\beta} = \int V_{conv,\alpha\beta} \tag{7}$$

by applying the of virtual flux in (7), the grid virtual flux vector can be estimated as shown in:

$$\psi_{g,\alpha\beta} = \int\left(\overline{V}_{conv,\alpha\beta}dt + RI_{g,\alpha\beta}\right) + LI_{g,\alpha\beta} \tag{8}$$

in practice, the value of internal line filter resistance R can be neglected since its value is much smaller than the value of the line inductance impedance Z_L. Therefore, in (8) can be rewritten in the stationary coordinates for acquiring the magnitude of grid virtual flux at both real and complex axes as shown in (9) to (10).

$$\psi_{g,\alpha} = \int V_{conv,\alpha}dt + LI_{g,\alpha} \tag{9}$$

$$\psi_{g,\beta} = \int V_{conv,\beta}dt + LI_{g,\beta} \tag{10}$$

then, the ideal integration that is used to calculate the grid virtual flux as shown in (9) to (10) might be saturated due to dc offset which is present in the sensed current or voltage. Thus, a low-pass filter is selected to replace the pure integrator. However, a simple low-pass filter reduces the system performance because it produces errors in the phase and magnitude of the virtual flux components calculations. To minimize these errors, in (11) and (12) are analyzed and adopted in the virtual flux estimation procedure which provides a low-pass filter characteristic at all frequencies. The $\alpha\beta$-components of the actual converter virtual flux $\Psi_{conv,\alpha\beta}$ are calculated based on the operating frequency with a given notation of ω_e or ω the low-pass filter cut-off frequency ω_c, and the estimate of the converter pole flux vector $\Psi'_{conv,\alpha\beta}$ as shown in Figure 4.

$$\Psi_{conv,\alpha} = \Psi'_{conv,\alpha} + \Psi'_{conv,\beta}\left(\frac{\omega_c}{\omega_e}\right) \tag{11}$$

$$\Psi_{conv,\beta} = \Psi'_{conv,\beta} - \Psi'_{conv,\alpha}\left(\frac{\omega_c}{\omega_e}\right) \tag{12}$$

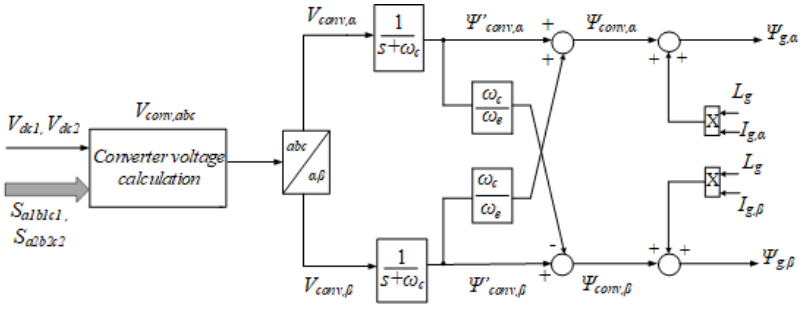


Figure 4. Control blocks for virtual flux estimation in 3L NPC VFDPC

Hence, by separating the real and imaginary components, the input instantaneous active power, P_{in} and reactive power, Q_{in} of the PWM AC-DC converter in a stationary frame can be written as:

$$P_{in} = \frac{3}{2}\omega\left(\Psi_{g,\alpha}I_{g,\beta} - \Psi_{g,\beta}I_{g,\alpha}\right) \tag{13}$$

$$Q_{in} = \frac{3}{2}\omega\left(\Psi_{g,\alpha} I_{g,\alpha} + \Psi_{g,\beta} I_{g,\beta}\right) \quad (14)$$

accordingly, the differentiation of active and reactive power can be represented as shown in (15) and (16), respectively:

$$\frac{dP}{dt} = \frac{3}{2}\omega\left(\Psi_{g,\alpha}\frac{dI_{g,\beta}}{dt} + \frac{d\Psi_{g,\alpha}}{dt} I_{g,\beta} - \Psi_{g,\beta}\frac{dI_{g,\alpha}}{dt} - \frac{d\Psi_{g,\beta}}{dt} I_{g,\alpha}\right) \quad (15)$$

$$\frac{dQ}{dt} = \frac{3}{2}\omega\left(\Psi_{g,\alpha}\frac{dI_{g,\alpha}}{dt} + \frac{d\Psi_{g,\alpha}}{dt} I_{g,\alpha} + \Psi_{g,\beta}\frac{dI_{g,\beta}}{dt} + \frac{d\Psi_{g,\beta}}{dt} I_{g,\beta}\right) \quad (16)$$

The illustration of the plotted waveform is shown in Figure 5 for the active power and Figure 6 for the reactive power are adopt to subject the response of an instantaneous of active and reactive power towards the particular converter voltage vector, V_n. Therefore, to generate the most compatible lookup table as shown in Table 3, the response of the sign and magnitude acquiring in each sector has been implemented due to the change of active and reactive power. For example, for the angle in the range 0° to 30°, the application of short voltage vectors (V_{S_3} V_{S_4} V_{S_5} V_{S_6}), medium voltage vectors (V_{M_3} V_{M_4} V_{M_5}), long voltage vectors (V_{L_3} V_{L_4} V_{L_5}), and zero voltage vectors (V_0 V_7) capable to produced for positive time-derivative for the active power. Thus, the active power tends to increase while those vectors are applied. However, through the implementation of voltage vector (V_{S_1}) for short, medium (V_{M_6} V_{M_1}), and long (V_{L_1} V_{L_2}) generate a negative-time derivative that intends to decrease the active power. That information is being applied to the remaining 11 sectors. This operating is carry on for the reactive power characteristics when the implementation from short (V_{S_2} V_{S_3} V_{S_4}), medium (V_{M_1} V_{M_3}), long (V_{L_2} V_{L_3} V_{L_4}), and zero (V_0 V_7) voltage vectors decide on to deliver a positive time-derivative of reactive power. Then by applying the voltage vectors from short (V_{S_5} V_{S_6}), medium (V_{M_5} V_{M_6}), and long (V_{L_5} V_{L_6}) bring to a negative time-derivative which reduce the reactive power. The same operating has been applied for the remaining 11 sectors in reactive power derivatives.

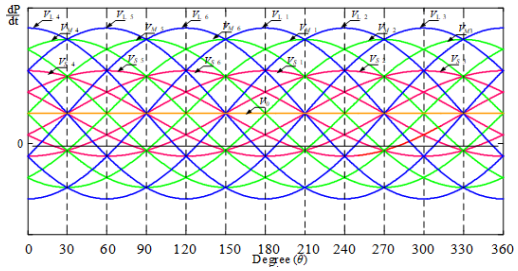


Figure 5. Differentiation characteristics under different voltage vector V_n for active power

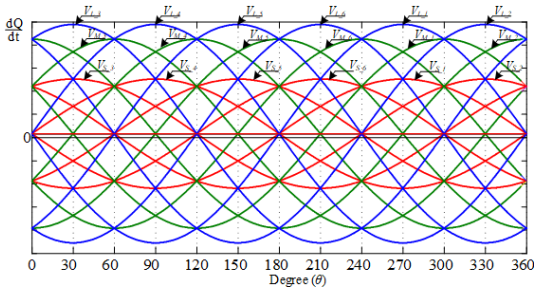


Figure 6. Differentiation characteristics under different voltage vector V_n for reactive power

4. THE PROPOSED BALANCED CONTROL STRATEGY

Operating a three-level NPC AC-DC converter involves by applying a short-amplitude voltage vector, which can potentially disrupt the balance between the upper and lower capacitor voltages, specifically V_{c1} (upper capacitor voltage) and V_{c2} (lower capacitor voltage). These voltage vectors are represented within an "inner hexagon" in the voltage space vector diagram as shown in Figure 2, where each vector offers two possible switching states: P-type and N-type. Selecting the appropriate switching state is crucial, as P-type and N-type states produce opposite effects on the capacitor voltages as can be seen in Table 3.

Table 3. Switching states for NPC

Type of switching state	Switching state	Effect toward capacitor voltage
P-type	[PPO], [POO], [POP], [OOP], [OPP], [OPO],	$V_{c1} < V_{c2}$
N-type	[OON], [ONN], [ONO], [NNO], [NOO], [NON]	$V_{c1} > V_{c2}$

The P-type switching state decreases the voltage across the upper capacitor (V_{c1}) by causing it to discharge, which results in V_{c1} dropping below V_{c2}. In contrast, the N-type switching state increases V_{c1} by discharging the lower capacitor (C_2), potentially causing V_{c1} to exceed V_{c2}. This voltage imbalance between V_{c1} and V_{c2} can significantly affect the converter's performance and stability. Achieving and maintaining a balanced voltage between V_{c1} and V_{c2} is essential to avoid issues such as short circuits. These issues can arise if the voltage difference between the capacitors becomes too large, leading to potential damage to the power switches and compromising the converter's functionality. Effective management of the switching states is therefore vital for the safe and efficient operation of the converter.

To mitigate these challenges, the balancing strategy block diagram is shown in Figure 7. This diagram represents a signal processing or control system model, where two input signals, V_{c1} and V_{c2}, are first subtracted to produce a difference signal. This difference is then passed through a relay block, which likely introduces decision-making logic, such as activating or deactivating the signal based on a specific threshold, 1 or 0. The converted signal is then multiplied by a constant value of 1 and another data type conversion follows, preparing the signal for output, which is labeled "Bs" to represents the balancing status and is directed to the MATLAB Function block for switching states.

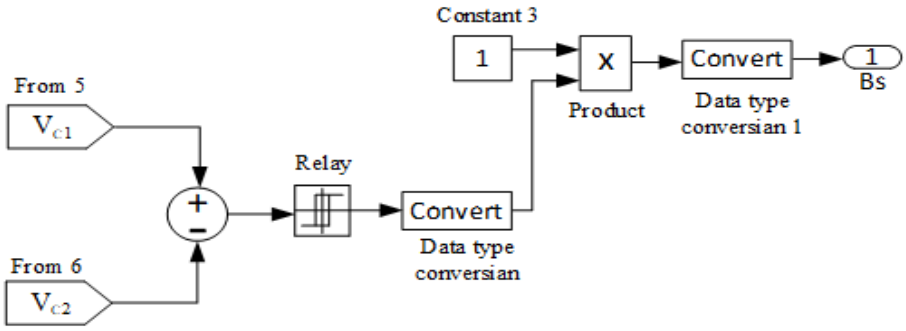


Figure 7. Block diagram for balancing strategy

An optimized switching table, presented in Table 4, has been developed for the three-level NPC AC-DC converter. This table is the result of extensive analysis, taking into account the effects of different voltage vectors on both active and reactive power flows, as well as their impact on the balancing status (Bs) of the capacitors. The Bs parameter directs the choice of switching state: Bs = 1 indicates that the P-type switching state should be employed. In this state, the upper capacitor voltage (V_{c1}) will decrease, helping to prevent Vc1 from becoming too high relative to V_{c2}. Meanwhile, Bs = 0 sate signal the application of the N-type is appropriate. Here, the upper capacitor voltage (V_{c1}) will increase, ensuring that V_{c1} does not fall too low compared to V_{c2}. By using this optimized switching table, the converter can dynamically adjust the switching states to maintain a balanced voltage between Vc1 and V_{c2}. This not only prevents potential short circuits and damage to power switches but also ensures the overall stability and efficiency of the converter's operation.

Table 4. Switching states for NPC

Power error status			Sector position (θ_n) and converter voltage vector (V_n)											
d_P	d_Q	B_S	θ_1	θ_2	θ_3	θ_4	θ_5	θ_6	θ_7	θ_8	θ_9	θ_{10}	θ_{11}	θ_{12}
0	0	-	V_{L_1}	V_{M_1}	V_{L_2}	V_{M_2}	V_{L_3}	V_{M_3}	V_{L_4}	V_{M_4}	V_{L_5}	V_{M_5}	V_{L_6}	V_{M_6}
0	1	-	V_{M_1}	V_{L_2}	V_{M_2}	V_{L_3}	V_{M_3}	V_{L_4}	V_{M_4}	V_{L_5}	V_{M_5}	V_{L_6}	V_{M_6}	V_{L_1}
1	0		V_{S_5}	V_{S_5}	V_{S_6}	V_{S_6}	V_{S_1}	V_{S_1}	V_{S_2}	V_{S_2}	V_{S_3}	V_{S_3}	V_{S_4}	V_{S_4}
		1	OOP	OOP	POP	POP	POO	POO	PPO	PPO	OPO	OPO	OPP	OPP
		0	NNO	NNO	ONO	ONO	ONN	ONN	OON	OON	NON	NON	NNO	NNO
1	1		V_{S_4}	V_{S_4}	V_{S_5}	V_{S_5}	V_{S_6}	V_{S_6}	V_{S_1}	V_{S_1}	V_{S_2}	V_{S_2}	V_{S_3}	V_{S_3}
		1	OPP	OPP	OOP	OOP	POP	POP	POO	POO	PPO	PPO	OPO	OPO
		0	NNO	NNO	NNO	NNO	ONO	ONO	ONN	ONN	OON	OON	NON	NON

5. SIMULATION RESULT

The three-level AC-DC converter system using the proposed switching look-up table in 3L NPC VFDPC is simulated in MATLAB/Simulink block diagram. The main parameter used in the simulation is given in Table 5. Therefore Figure 8 show the results that obtain from the simulation and consists of six subplots from different aspect of electrical signals. The first subplot Figure 8(a) illustrates the phase voltages Va, Vb, and Vc over time, depicted as sinusoidal waveforms with 120° phase shifts, characteristic of a balanced three-phase AC system. The voltages exhibit consistent amplitude and frequency, indicating a stable source. Subplot Figure 8(b) shows the phase currents I_a, I_b, and I_c over time, which also follow sinusoidal patterns. In Figure 8(c) represents the unity power factor operation where the phase *A* voltage and current are in phase. Meanwhile, the estimated instantaneous active power and reactive power are shown in Figure 8(d). It is clear to see that the reactive power is kept at 0 VAr to achieve unity power factor operation. The dc output voltage V_{dc} follows the dc reference which is set to 150 V as shown in Figure 8(e). Finally, in Figure 8(f) presents a harmonic analysis of the system, focusing on total harmonic distortion (THD) for input current, which is calculated at 1.34%. This value of THD complies with the specification of *IEEE-519* where the current THD should be less than 5%.

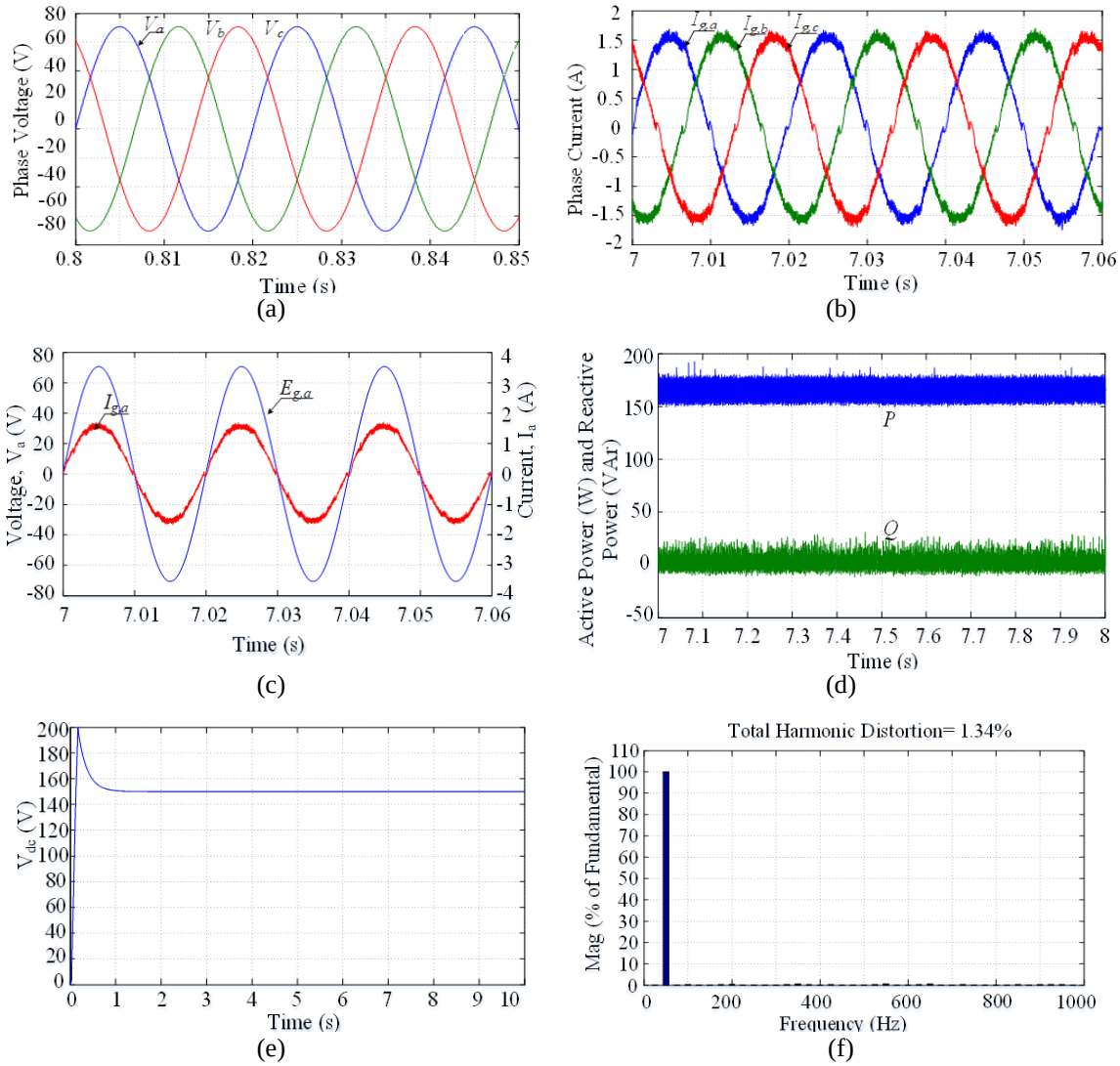
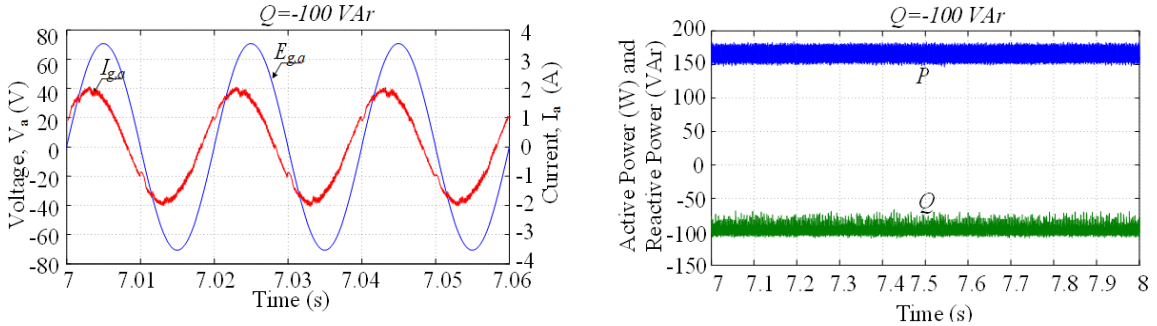


Figure 8. Simulation results from 3L NPC VFDPC (a) three-phase supply voltage, (b) three phase input current, (c) phase *a* voltage and current at unity power factor operation, (d) estimated input instantaneous active and reactive power at unity power factor operation, (e) generated dc-link output voltage, and (f) harmonic spectrum of the input line current

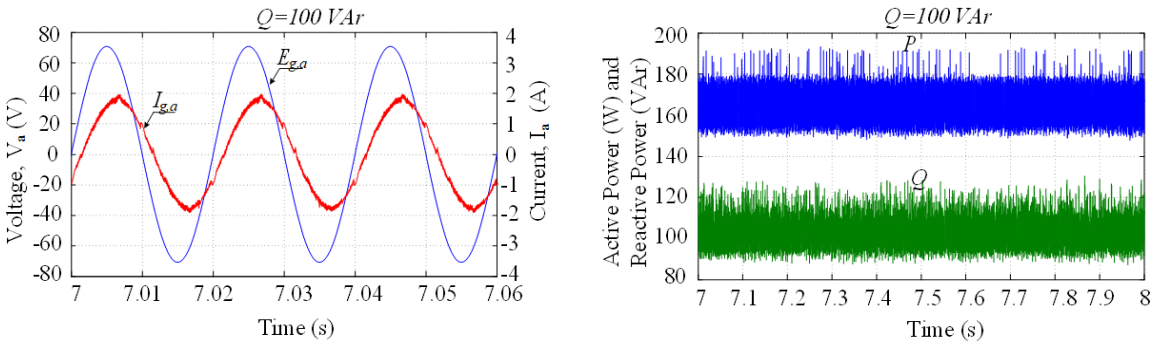
Table 5. The parameters used in 3L NPC VFDPC

Parameter	Value
Input phase voltage (peak) E_g	70.71V
Source voltage frequency f	60Hz
DC-link voltage reference $V_{dc.ref}$	150V
Resistance of reactors R	0.2Ω
Inductance of reactors L	15mH
DC-link capacitor C	10.8mF
Load resistance R_{load}	140Ω
Sampling time T_s	20μs
Sampling frequency $fs=1/T_s$	50kHz

The input reactive power reference Q_{ref} is set to zero to operate the PWM rectifier at unity power factor mode. In some applications, controller is required to be operated at leading or lagging power factors modes as shown in Figure 9. The value of Q_{ref} is being set either 100 VAr or -100 VAr to demonstrate lagging or leading power factor operations, respectively. In leading power factor operation mode, the phase *a* current leads the phase *a* supply voltage while the instantaneous reactive power Q_{inst} tracks the reference value of Q_{ref} which is -100 VAr as shown in Figure 9(a). The magnitude of the active power is maintained at 150 Watt. Lagging power factor operation mode is activated by shifted up the Q_{ref} from 0 to 100 VAr which will result the phase *a* current lags the phase *a* voltage. Meanwhile, the instantaneous of reactive power Q_{inst} tracks the reference value of Q_{ref} successfully, while maintaining the magnitude of the instantaneous active power $P_{inst.}$ as can be seen in Figure 9(b).



(a)



(b)

Figure 9. Power factor mode (a) leading power factor and (b) lagging power factor

The control method is also evaluated under the transient response during load variation and once the DC voltage reference command changes from 150 V to 180 V at 5s and back to 150 V at 8s as shown in Figure 10. In load variation, a 100 Ω resistor is connected in parallel with the existing resistor across the dc-link at 3s to create a sudden disturbance to the load current. A breaker is used in the simulation for connecting the additional resistor to the existing resistor. It is apparent to see that the DC output voltage is experiencing a sudden drop with small dip but it recovers to the original value 150 V forced by the voltage *PI* regulator as shown in Figure 10(a). Then, in Figure 10(b) the estimated active power, *P* follows the change in load as it increases suddenly at 3s due to the load disturbance. Meanwhile, the overshoot and oscillation are not obvious

for reactive power, *Q*. Lastly, at the time of 3s in Figure 10(c) the line current waveform from phase *a* started to increases once the disturbance occurs at time of 3s regarding to the relationship of current and resistance in ohm's law. Next, Figure 10(d) shows the transient response when the dc voltage reference varies. With the calculated quantities of the DC-link voltage *PI* regulator, the dc output voltage V_{dc} follows the V_{dcref} with less overshoot. The estimated active power also increases and decreases rapidly to new values during the step changes of the output voltage while keeping the reactive power at 0 VAr as shown in Figure 10(e). Lastly, the line current I_a is obviously increased and decreased as shown in Figure 10(f) which accommodate to the increasing and decreasing of the converter dc output voltage.

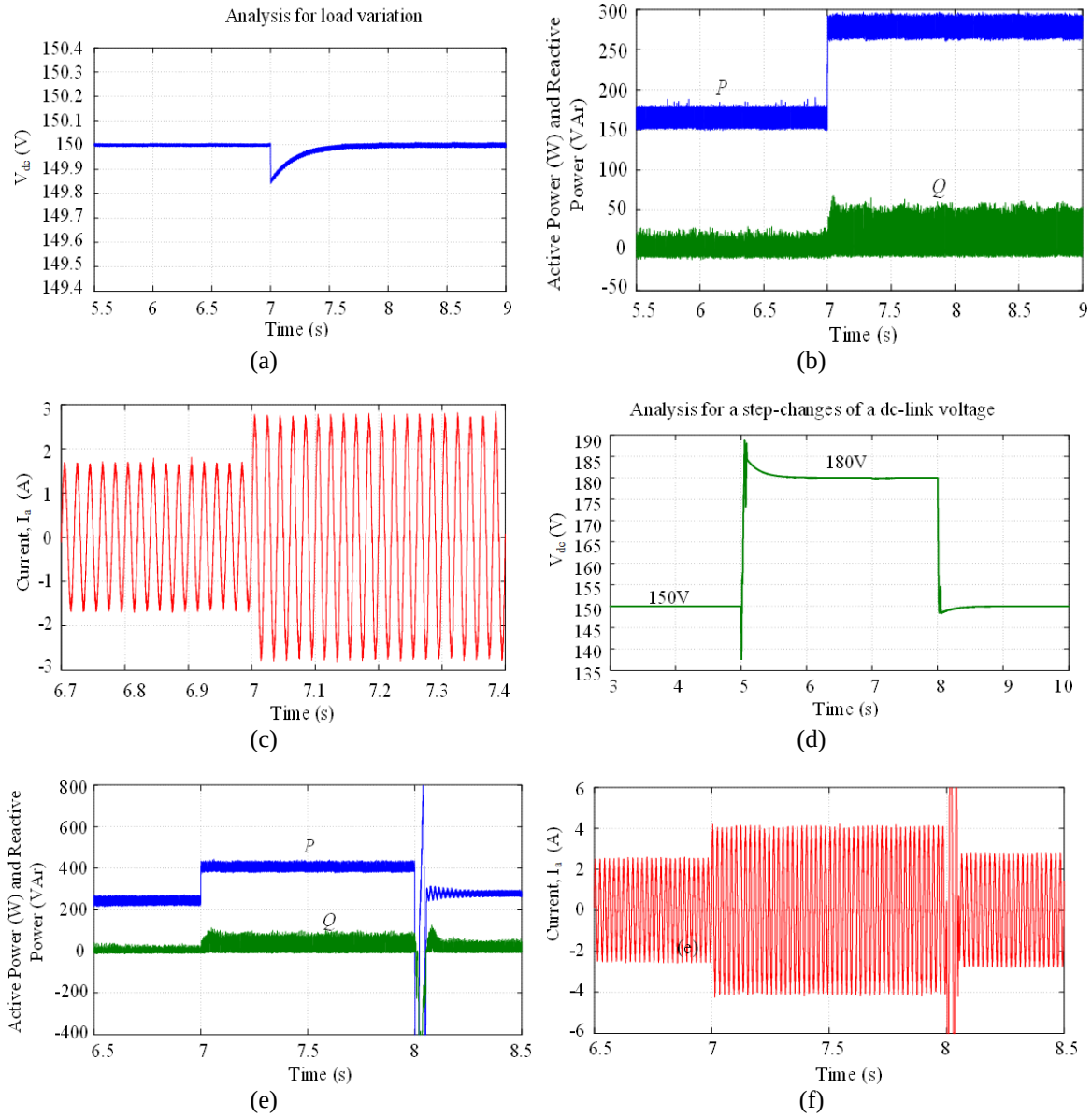


Figure 10. Analysis for load and dc-link variation (a) to (c) transient response for load variation from low to high power demand and (d) to (f) transient response for dc output voltage changes; (a) and (d) Dc-link output voltage (b) and (e) estimated active and reactive power (c) and (f) phase *a* current

6. CONCLUSION

The present paper, therefore has shown that the proposed VFDPC integrated onto a three-level NPC topology to improve dynamic behavior and robustness of operation. VFDPC: using direct estimates of grid voltage and power components, this solution entirely eliminates the use of traditional AC input voltage sensors

simplifying system design by removing complexity as well significantly reducing sensitivity to high-frequency noise and interference. This will result in reduction of material costs and more reliable power conversion systems. In addition, a lookup table strategy is proposed to tackle the voltage imbalance of the DC-link capacitor in NPC topology at its origin so that balance under applicable SV conditions can be achieved with lower switch stress on all devices. The results highlight several benefits of VFDPC, generating the line currents very close to be sinusoidal having limited THD, realizing unity power factor operation and handling both lagging as well as leading power factor states. In addition, VFDPC is able to control DC-link output voltage independent of loading condition which results in applicability for a wide range loads configurations. The results capture the complementarity of VFDPC characteristics and their collective benefits in power quality improvements, system stability support under various dynamic or increasing load conditions. Hence, VFDPC presents a viable control strategy for emerging AC-DC conversion applications providing high efficiency and improved power electronic system reliability.

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