

Higher Efficiency Switching Mode Power Amplifier Design using the Third-Harmonic Peaking Turning Mode

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Abstract

This paper provides the design approach of one stage switching-mode based class F power amplifier (PA). The device's nonlinear behavior was analyzed to reduce the dissipated power over the active device and therefore the PA efficiency was increase without having to compromise the power amplifier's size. The load harmonics were controlled so that the drain voltage and the drain current do rarely coincide with each other, thus greatly increase the power performance of the device. Taking the device size and cost parameters into consideration, the design of load harmonic trap circuit was reduced only to the 2nd and 3rd harmonics. The GaN HEMT transistor, for its high-speed switching ability, is used in our design to maximize the output power and the optimized circuit operating at 5.8GHz with output power of 50.98W was simulated. A power added efficiency of 60% with the power gain of 14dB was obtained.

Keywords: class-F, loadPull, harmonic trap, RF power amplifier, third-harmonic peaking

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1. Introduction

The radio frequency (RF) power amplifier are one of the most important element in transmitter units of communication systems. The requirements on the power amplifier have become more important regarded to the system performance. For good performance, not only a considerable gain with high efficiency is required but also a suitable output power is expected to be provided. For the reliable transmission the PA output power must be sufficient.

As communication market growing up, digital signal processing modules and the radio frequency integrated circuits (RFIC) are usually integrated into portable electronics in order to ensure multimedia applications in small sized devices. Linear RF power amplifiers because of their low power efficiency they have some drawbacks as they consume large amounts of energy, dissipate great heat, and occupy big space in base stations. Cell-phones and other portable communication device or base-stations are in an increasing pursuit of the efficiency to satisfy the requirement of long standby time and low cost, all these requirements depend on the power amplifier in these devices. So the high efficiency PA draws much more attentions in this research field. Significantly more efficient PA technology is necessary to the evolution of mobile systems. To achieve high efficiency it is necessary to minimize losses which are largely dissipated in the active device especially when the amplifier is operating at high current and voltage levels. The power dissipated in the active device increases as the overlap of voltage and current waveforms increases. To deal with the power dissipated thought the active device we need to ensure that there is non-overlapping region of the current and voltage waveforms at the active device; once this condition is reached the higher power efficiency can be obtained. In this paper we used the non-linear device. PAs operating in the switch-mode domain exploit the nonlinear region of the device to impose a highly efficient set of non-overlapping current and voltage drain waveforms [1]. The drain voltage waveform will be shaped to a square wave and current waveform will be shaped to a half-sinusoidal wave. Therefore, across the active device there will be no overlap between drain voltage and current waveforms, as a result, zero power dissipation is created while achieving in the same time the theoretical 100% drain efficiency. In practice, to simplify the circuit design only the 2nd and 3rd harmonics have been considered since the number of harmonics that can be effectively controlled is finite.

The main purpose of this paper is to provide a design procedure for simplified broadband higher frequency Class-F power amplifier design. In this design the Advance system design (ADS) software was used along the design process and simulations from the transistor modeling to the final circuit optimization.

2. Class-F PA Architecture and Design Techniques

2.1. Switching Mode Power Amplifier Architecture

To substantially increase the efficiency of a class F power amplifier, we need to produce an open circuit at the odd harmonics and the short circuit at even harmonics at the active device output. With such required harmonic tuning, the simultaneous appearance of the voltage across the active device output and current through it containing the harmonics of the same order is to be avoided. By analyzing Fourier series expansion of the voltage and current waveforms as expressed in the Equation (1) and (2) respectively, we can define the output impedance, the condition at which the power dissipated through the active device is minimized and then the maximum practical drain efficiency can be reached.

$$V(\theta) = V_{DD} + V_1 \sin \theta + \sum_{n=3,5,7,\dots}^{\infty} V_n \sin n\theta \quad (1)$$

$$I(\theta) = I_o - I_1 \sin \theta - \sum_{n=2,4,6,\dots}^{\infty} I_n \sin n\theta \quad (2)$$

Mathematically taking an infinite number of harmonics into account, the obtained shape of waveforms is a square wave (odd harmonic) and a half sinusoid wave (even harmonic) for the voltage or current respectively.

The waveforms shown in Figure 1 result in 100% of drain efficiency. When we come to the practice in the real world, to control impedances for an infinite number of harmonics becomes very difficult.

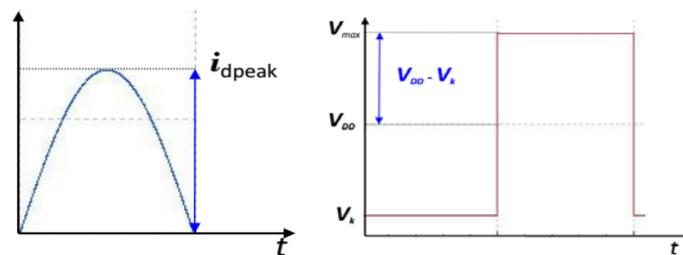


Figure 1. Waveforms which Result in an Efficiency of 100%

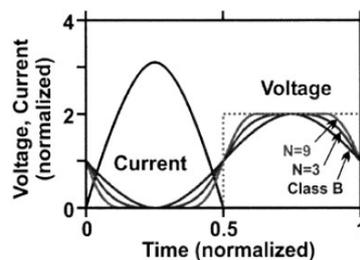


Figure 2. The Drain Waveforms in Practice

Greater the number of harmonics is, better the efficiency is. To achieve a noticeable increase in efficiency we need a higher number of harmonics also to be taken into account as the Figure 2 shows [2], but as we increase the number of harmonics the circuit become complex and the final device size is also engaged, for this reason we typically use the Third-Harmonic peaking [3, 7] tuning mode in which the input impedance of the output network is only controlled up to third harmonic.

The output network design should also involve the acceptable matching circuit at the fundamental frequency to achieve high efficiency. The two fundamental balance conditions should be satisfied to achieve 100% drain efficiency (η_d): as described in the Equation (3), the power dissipations at the higher harmonic frequencies must be zero and the DC power supply must be equal to the power generated at the fundamental frequency.

$$\eta_d = \frac{P_1}{P_{DC}} \times 100\% \quad (3)$$

Where P_1 is power generated at the fundamental frequency. P_{DC} is DC power supply.

The first condition to be realized the load impedance at odd harmonics is therefore supposed to be tuned to open circuit ($Z_{load} \approx \infty$) and the load impedance at even harmonic should be tuned short circuited ($Z_{load} \approx 0$). For the second condition some adjustments are carried out for maximizing drain efficiency.

In this method, the phase between voltage and current at the harmonics is always ± 90 degrees, so that the power factors at all harmonic frequencies become zero [4].

2.2. Class F Power Amplifier Design Procedure

CGH40045 GaN HEMT is the transistor used in our design. It is biased as $V_{DS} = 28$ V, $I_{DQ} = 741$ mA and $V_{GS} = -2.1$ V (Figure 3), a stable factor of 1.975 was computed over our design central frequency of 5.8 GHz (Figure 4).

The software used is Advanced Design System. The following subsections illustrate the design procedure we used.

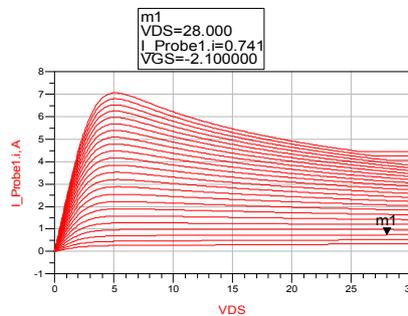


Figure 3. Bias Point Determination

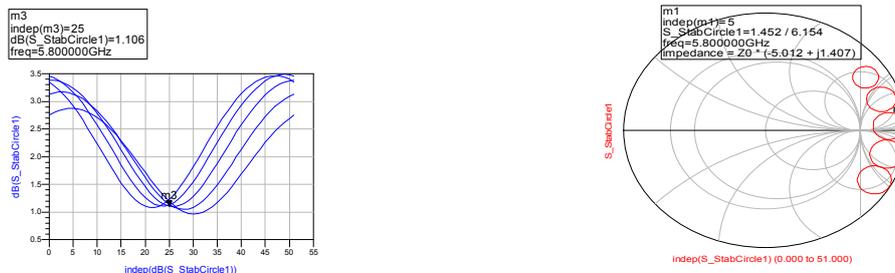


Figure 4. Stability Factor Plot as Function of Frequency

2.3. Harmonic Networks Architecture

The common practice in Class F power amplifier design involves the design of a tuning network for load harmonics basically designed up to a certain order harmonics as shown by the Figure 5, the design of matching network at the fundamental frequency is also engaged (Figure 6(b)). The tuning network at the odd order harmonic looks like an open circuit, at the even order harmonics it presents a short circuit. Taking the complexity of the circuit and the possibly loss introduced by the higher order harmonics into the design in consideration, in this paper we only considered the second and third order harmonics (Figure 6(c)).

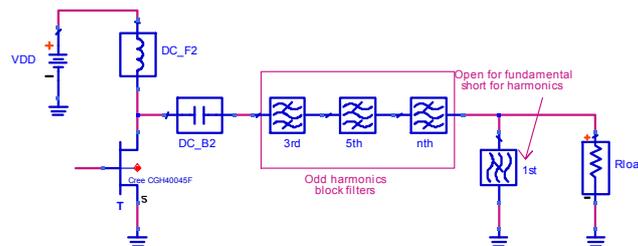


Figure 5. The Load Harmonic Tuning Network Design

Saturated drain currents, breakdown voltages are some of the characteristics of the radio frequency power transistors.

To find the load impedance corresponding to the maximum power the two extreme values of drain voltage and current are engaged, resulting to their excursions from near zero to nearly the maximum values. Using the Smith chart, for a given delivery amount of RF power we can find that for a specified maximum drain voltage the corresponding load impedances lie along parallel-resistance lines. Similarly for a specified maximum current we can find that the impedances follow a series-resistance line.

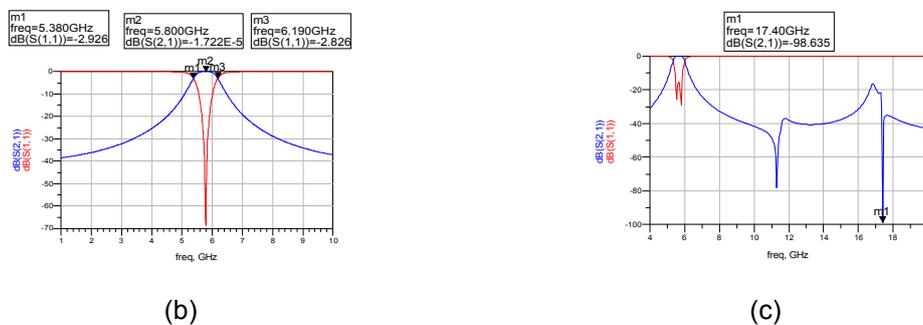


Figure 6. (b) First harmonic trap, (c) Harmonic networks response

Constant-power contour for an ideal power amplifier has a football shape. In a real power amplifier, due to the parasitic elements such as the drain capacitance and bond-wire or package inductance we have an embedded “virtual drain”. The drain impedance transformation affects the constant-power contours which become rotated even distorted. These addition of second-order effects, lead the power-contours to the elliptical shape.

When designing the output matching circuit of traditional RF amplifier, such as LNA, we need to design an output matching circuit which is the conjugate match with the output of the transistor. Because conjugate matched circuit let the amplifier gets the maximum gain, but gain is not the only consideration when we are design power amplifier; the more important consideration of power amplifier is the Power Added efficiency (PAE) which the expression is given in Equation (4).

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{4}$$

Where P_{out} , P_{in} and P_{DC} stand, respectively, for RF power output, input drive power and DC power supply.

The transistor parasitic elements are the major factor that disturbs the open-load and the short-load conditions for the harmonics, to minimize their effect on the device performance we used the load pull technique to find out the best load impedance of our power amplifier to operate in the maximum power efficiency with a certain high gain. Load pull is a technique wherein the load impedance seen by the device under test (DUT) is varied and the performance of the DUT is simultaneously measured [5, 6].

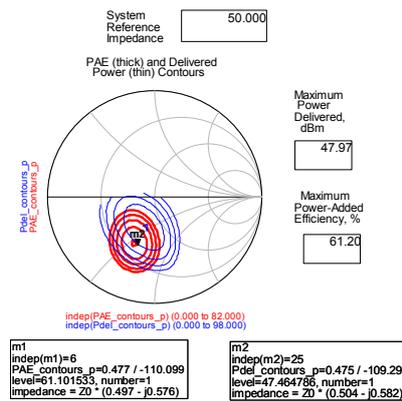
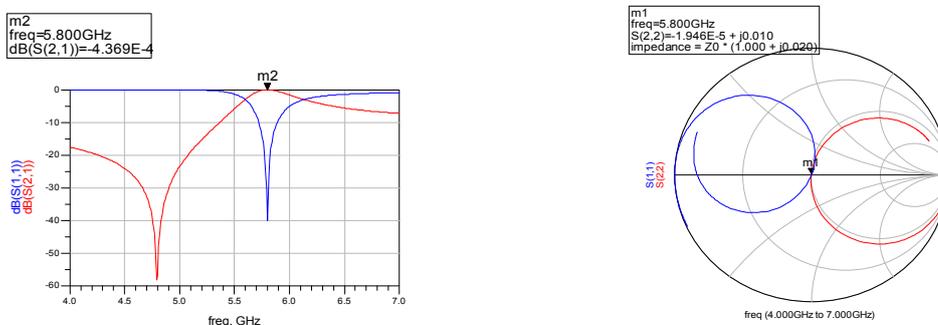


Figure 7. The Best Load Impedance of the Amplifier

As the Figure 7 shows, we find that to achieve the desired output power of 50W, we found that the load impedance corresponding the required output power is $20.877-j25.384$; in this case the PAE above 60% was obtained.

2.4. Input/output Networks Matching and Design Optimization

For the frequencies beyond 500MHz designing the filter with discrete components becomes difficult to realize as the wavelength and the physical dimension of the filter become comparable, this results in various losses which may cause several degradation of the circuit performance. Thus, in order to realize the practical filter and network matching circuit, in this design the lumped component were converted into distribution element. We adopt the use of micro-strip lines.



(a) Output circuit optimization (b) The output impedance matching
Figure 8. S21 and S11 Parameters

After designing the harmonic networks we need to match the network designed to the load impedance computed by the load pull simulation. This is realized in two steps. The first step is to find the impedance formed by the load of 50Ω and the harmonic networks at the output network. The value of impedance obtained is $46.629+j0.3052$. In the second step the task to perform is to transform the $46.629+j0.3052$ impedance into the impedance seen by the transistor as a DUT which corresponds to $20.877-j25.384\Omega$. This impedance matching is realized by using the Smith chart. After the circuit optimization as we can see it on the Figure 8, the output is pretty well matched.

The final designed output network is shown at the Figure 9. The input network matching we designed uses the same techniques as performed above but this is done after the output network and the load are all connected to the transistor output port. The Figure 10 shows the input network circuit of this design. Simulated output power gain vs. frequency offset and factor of stability vs. frequency are presented in the Figure 11 and shows that the obtained gain is 12.972dB when the reachable maximum gain is 14.468dB.

So the optimization of the micro-stripe line parameters must be performed in order to increase the gain of this power amplifier.

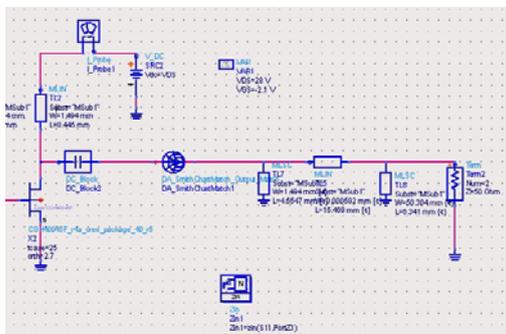


Figure 9. The Matched Output Network

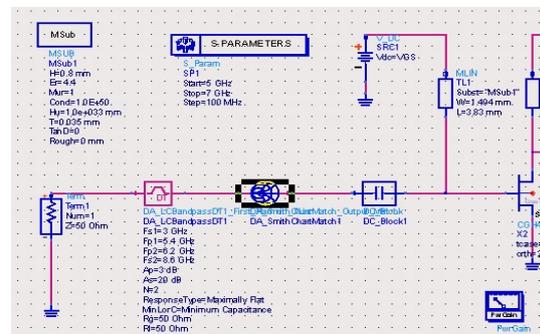


Figure 10. Input Network

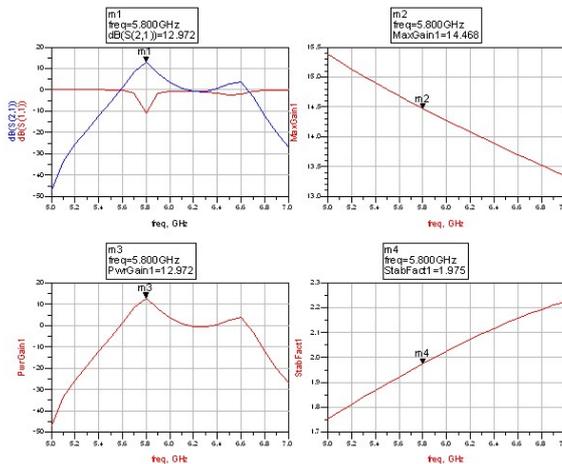


Figure 11. Power Gain vs. Frequency Offset and Factor of Stability vs. Frequency

The S parameters simulation results after optimization are given by the Figure 12 and the final designed circuit is given in the Figure 13.

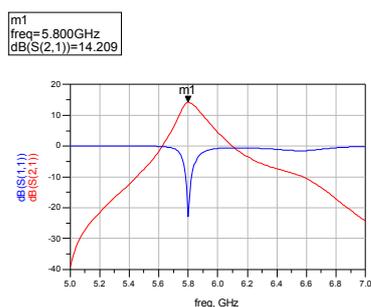


Figure 12. S11 and S21 Simulation Results after Optimization

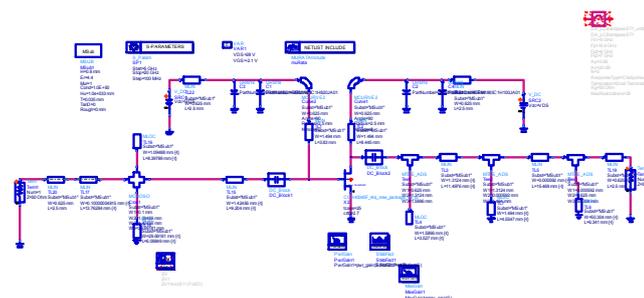


Figure 13. The Final Designed Circuit

3. Conclusion

Based on simplified class F architecture third-harmonic peaking turning mode was used to design a PA operating at 5.8GHz using a GaN HEMT transistor. In this design it is shown how the load pull and source pull techniques are very indispensable to reduce the impact of the transistor parasitic elements on the power performance of a switching-mode PA, the importance in the control of voltage and current waveform to reduce the power dissipated at the harmonic frequencies was also presented. Transmission lines are utilized to design the harmonics trap network taking only three harmonics into account. The simulated maximum output power of 50.98W with the optimum gain of 14dB is presented. Excellent performance was achieved over the bandwidth of 100MHz, for the power variation less than 1dB the value of the drain efficiency remains higher than 50%. Through the results obtained, we can conclude that the designed Class F PA is suitable for the fields where the higher output power and higher efficiency are the main demands.

References

- [1] Tuffy, Neal. A Simplified Broadband Design Methodology for Linearized High-Efficiency Continuous Class-F Power Amplifiers, *IEEE Transactions on Microwave Theory and Techniques*. 2012.
- [2] David M Snider. A Theoretical Analysis and Experimental Confirmation of the Optimally Loaded and Overdriven RF Power Amplifier. *IEEE Trans. On Electron Devices*. ED-14,
- [3] Muthuswamy Venkataramani. Efficiency Improvement of WCDMA Base Station Transmitters using Class-F power amplifiers. M.S. thesis, Dept. Elect. Eng., Virginia Polytechnic Institute and State Univ., Blacksburg, Virginia. 2004.
- [4] Kazuhiko Honjo. *Ultra High Efficiency Microwave Power Amplifier for Wireless Power Transmission*. Proceedings of the 42nd European Microwave Conference, Amsterdam, Netherlands. 2012.
- [5] SC Cripps. *RF Power Amplifiers for Wireless Communications*. Artech House, Norwood, MA. 1999.
- [6] Dehao Wu, E Korolkiewicz, Q Lu, LLiu. *To Design and Model a Class F Amplifier and Investigate the Effect of Losses on the Efficiency of dc to ac Power Conversion*. Communication Systems Networks and Digital Signal Processing (CSNDSP), 7th International Symposium on. 2010.
- [7] Joon Hyung Kim, Gweon Do Jo, Jung Hoon Oh, Young Hoon Kim, Kwang Chun Lee, Jae Ho Jung. Modeling and Design Methodology of High-Efficiency Class-F and Class-F Power Amplifiers. *IEEE Trans. On microwave theory and techniques*. 2011; 59(1).