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Advanced generalized integrator based phase lock loop under complex grid condition: a comparative analysis

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ABSTRACT

Integration of renewable energy systems (RESs) to the grid leads to various power quality issues. A proper control approach for the interfaced inverter is required to mitigate the uncertainties caused in the grid due to the RESs association to maintain the grid stability. The presence of harmonics and DC offset in the input grid voltage of a phase lock loop (PLL) leads to inaccurate phase estimation due to fundamental frequency oscillations. Though many advanced generalized integrators (GI) based PLLs have been developed still there is a need for a robust PLL for synchronization with faster dynamic response, both the harmonics and DC offset rejection ability with precise estimation. This paper proposes some simple yet effective advanced PLLs employing low pass filters (LPFs) in the existing GI based PLLs for faster and accurate phase angle estimation for seamless synchronization under complex grid circumstances. These advanced generalized integrators with LPFs (GI-LPF) based PLLs will provide enhanced and robust synchronization for the grid integrated RESs thereby addressing multiple power quality issues like voltage unbalance, harmonics and DC offsets. The simulation based comparative analysis of the proposed controllers confirm their effective disturbance rejection capability under complex grid conditions by providing advanced and precise response.

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1. INTRODUCTION

The rising demand for electricity, combined with environmental concerns, has significantly integrated RESs into the grid, causing various power quality issues. Generally, an inverter is used as an interface for the integration of the RESs with the existing grid [1], [2]. To achieve proper grid synchronization with RESs, robust control of the interfaced inverter through PLL is necessary. A strong PLL is essential for grid synchronization and mitigating power quality issues. It extracts grid frequency, phase angle, and voltage amplitude for coordination and power flow control between RESs and the grid. PLL is basically a close loop control system consisting of phase detector (PD), loop filter (LF) and voltage controlled oscillator (VCO) [3]-[6]. The main purpose for PLL is to have an accurate phase angle estimation during normal or complex grid condition. Many PLL schemes have been studied and proposed by the researchers to estimate the phase angle accurately under non ideal grid circumstances [7]-[11]. Most of the PLL schemes are found with the synchronous reference frame PLL (SRF PLL) [12], [13] as the base for the proposed PLL design. The fundamental SRF PLL tracks phase angle well under ideal grid conditions, but during distorted or unbalanced grid situations, it introduces double frequency oscillations, causing synchronization errors. So, this necessitates the need for advanced SRF PLLs for synchronization.

The rise in nonlinear loads and RES integration has caused unbalanced voltage, voltage distortion, and DC offset in power lines, impacting PLL response and reducing power quality. Advanced PLL algorithms using generalized integrator (GI) for orthogonal signal generation (OSG) have become essential for synchronization, offering resilience in non-ideal grid voltage conditions. A comparative analysis of OSG based PLLs is outlined in [14], showcasing their effectiveness in mitigating diverse power quality concerns. To obtain enhanced PLL response with efficient and faster phase detection, advanced GI based PLL algorithms as orthogonal signal generators have been developed [15]-[20].

Though different solutions for power quality issues through PLL like frequency jump, phase jump, unbalanced grid conditions, sags, swells and harmonics present in grid voltage are there, still there is a research gap to overcome the issue of phase estimation during DC offsets with harmonics existence in the grid voltage and hence needs to be bridged. Notable solutions proposed by the researchers include dual second order generalized integrator phase lock loop (DSOGI PLL) [21], [22], dual third order generalized integrator phase lock loop (DTOGI PLL) [23]-[25] and dual mixed second and third order generalized integrator phase lock loop (DMSTOGI PLL) [26], [27]. The DSOGI PLL technique segregates the positive and negative sequence components of unbalanced voltage originating from the PLL's output for accurate phase estimation and synchronization. In scenarios of grid voltage with DC offset and harmonic components presence, a steady state error arises in the output of DSOGI PLL which hampers it's effectiveness in robust synchronization due to inaccuracy in estimation. The extraction of the fundamental grid voltage component is vital for synchronization amidst adverse conditions. By implementing modifications in the DSOGI based PLLs, it's possible to offset power quality issues and enhance PLL performance. Enhancing the filter's order to sharpen the passband (resulting in increased narrowness) for greater attenuation of higher and lower order dominant harmonics and nullification of DC offset was found out to be one of the possible solutions. The DTOGI PLL proposed in literature as an alternative method that exhibits superior harmonic filtering capabilities compared to DSOGI PLL due to it's third order transfer function but is still being sensitive to DC offsets presence. For overcoming the impact of DC offsets and harmonics in the grid voltage affecting the PLL accuracy in phase estimation, the DMSTOGI PLL effectively addresses these two issues in the grid with RESs synchronization but still has a slower dynamic response.

The PLLs mentioned above lacks the capability to effectively tackle the challenge of simultaneously rejecting harmonic voltage and DC offset voltage within the PLL while also maintaining satisfactory dynamic characteristics. Hence, this paper proposes some advanced GI based PLLs under complex grid conditions for accurately obtaining the phase of the fundamental positive sequence components of the voltage with fastest dynamic response and higher robustness. Other solutions in literature include placing different filters [8], [11], [13], [14], multiple filters or more filters in combination to the aforementioned GI based filters [15], [16], [18]-[20], [22], [24] but were either incapable of rejecting the effects of both the issues or else the increased system complexity hampered the system response furthermore. The proposed PLLs in this paper use the concept of employment of low pass filter (LPF) after the GI based adaptive filters in the PLL's control loop for performance improvement with system simplicity and faster response with precise phase estimation. An effective yet simple technique of DC offset elimination based on use of adaptive LPF has been proposed to remove the DC offsets with harmonics from the input voltage signal before passing it on to the SRF PLL for precise phase extraction. It is basically an add-on to any GI based PLLs without altering the GI filter's bandwidth design. Unlike previous methods, the application of the proposed method for DC offset removal has a minimal effect on the dynamic performance of the PLL under study. The superiority and effectiveness of the proposed PLL methods named as dual second order generalized integrator-low pass filter PLL (DSOGI-LPF PLL), dual third order generalized integrator-low pass filter PLL (DTOGI-LPF PLL) and dual mixed second and third order generalized integrator-low pass filter PLL (DMSTOGI-LPF PLL) has been verified by the simulation results in MATLAB environment and a proper comparative result analysis. This paper provides a comprehensive performance analysis of the advanced GI based PLLs based on the enhancement of the system performance in terms of system dynamics and disturbance rejection abilities named as GI-LPF based PLLs with respect to the GI based PLLs.

This paper is structured like this: section 2 presents an Overview of the GI based filters for OSG used by the SRF PLL for the accurate phase extraction during grid disturbances to achieve robust synchronization. Section 3 introduces the proposed novel advanced GI based PLLs with LPF in the PLL control loop for performance enhancement, faster system response and accurate phase estimation during grid disturbances with DC offsets and harmonics presence. Section 4 conducts a simulation based comparative result analysis in MATLAB environment for performance evaluation of the proposed PLLs against the other GI based PLLs known for their excellent performance under two test conditions which include the two phase voltage sag with 5^{th} and 7^{th} harmonics and the presence of DC offsets in the grid voltage. Finally, section 5 provides the conclusion implicating the most suitable PLL to be used for grid with RESs synchronization under weak grid condition.

2. OVERVIEW OF GENERALIZED INTEGRATOR BASED FILTERS

In the context of OSG based filtering approach for extracting the synchronizing signals amidst grid voltage disturbances, GI based methods hold preference. An overview of the implementation of different GIs as adaptive filters for phase estimation in PLLs has been provided in this section. Figures 1-3 illustrate the structures of the standardized second order generalized integrator (SOGI) [21], [22] filter, third order generalized integrator (TOGI) filter [23]-[25] and mixed second and third order generalized integrator (MSTOGI) [26], [27] filter which serve as OSG throughout the PLL's prefiltering stage for accurate phase extraction. It generates the orthogonal signals (v' and qv') as filtered outputs of v as the input signal with $\hat{\omega}$ and *k* as the estimated frequency and damping coefficient, respectively [3].

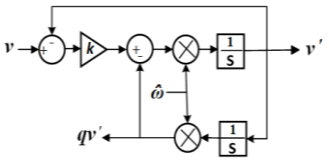

Figure 1. SOGI OSG filter

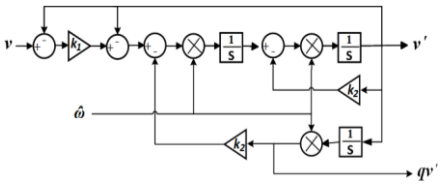

Figure 2. TOGI OSG filter

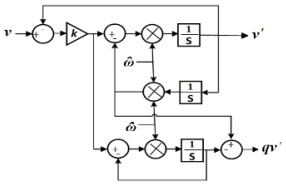

Figure 3. MSTOGI OSG filter

2.1. Second order generalized integrator

The optimized gain (*k*) value of the SOGI filter is 1.414 which determines the bandwidth (BW) of R(s). A lowered *k* value enhances the filtering capacity of R(s) but increases dependance on the resonantly extracted grid frequency ($\hat{\omega}$). Conversely, a lower k value improves the filtering effect of Q(s) but may affect the dynamic response or settling time. The transfer functions of the SOGI filter are defined as:

$$R(s) = \frac{v'}{v}(s) = \frac{k\hat{\omega}s}{s^2+k\hat{\omega}s+\hat{\omega}^2} \quad (1)$$

$$Q(s) = \frac{qv'}{v}(s) = \frac{k\hat{\omega}^2}{s^2+k\hat{\omega}s+\hat{\omega}^2} \quad (2)$$

2.2. Third order generalized integrator

The optimized TOGI filter gain (k_1 and k_2) values are 2.82 and 1.1 each. The k_1 parameter controls the filter BW, while k_2 determines the filter's dynamic response. Increasing k_1 broadens the filter's bandwidth, thus lowering the harmonic attenuation. Conversely, an increased k_2 value results in slower filter's response with a decreased overshoot. The transfer functions of the TOGI filter are defined as:

$$R(s) = \frac{v'}{v}(s) = \frac{k_1\hat{\omega}^2 s}{s^3+k_2\hat{\omega}s^2+(k_1+1)\hat{\omega}^2 s+k_2\hat{\omega}^3} \quad (3)$$

$$Q(s) = \frac{qv'}{v}(s) = \frac{k_1\hat{\omega}^3}{s^3+k_2\hat{\omega}s^2+(k_1+1)\hat{\omega}^2 s+k_2\hat{\omega}^3} \quad (4)$$

2.3. Mixed second and third order generalized integrator

The MSTOGI filter is constructed with an additional component in the generalized SOGI to attenuate the effect of the DC offsets present in the input grid voltage signal, thereby producing a TOGI. The SOGI and TOGI together form the MSTOGI adaptive filter where $\hat{\omega}$ denotes the estimated grid frequency, while *k* stands for the gain of the MSTOGI filter with an optimized value as 1.414. A larger value of *k* indicates a faster dynamic response and enhanced stability, although at the potential cost of compromised filtering capability. The transfer functions of the MSTOGI filter are defined as:

$$R(s) = \frac{v'}{v}(s) = \frac{k\hat{\omega}s}{s^2+k\hat{\omega}s+\hat{\omega}^2} \quad (5)$$

$$Q(s) = \frac{qv'}{v}(s) = \frac{k\hat{\omega}s\,(\hat{\omega}-s)}{(s+\hat{\omega})\,(s^2+k\hat{\omega}s+\hat{\omega}^2)} \quad (6)$$

3. PROPOSED GENERALIZED INTEGRATOR-LOW PASS FILTER BASED PLLS

The proposed novel enhanced generalized integrator-low pass filter based PLL (GI-LPF PLL), addresses the issues of DC offset and harmonics, based on the GI based PLL structure. The generalized GI based PLL utilizes two numbers of respective GIs in the $\alpha\beta$ frame of the PLL's prefiltering stage. Hence, the

GI based PLLs are named as DSOGI PLL, DTOGI PLL and DMSTOGI PLL respectively. The proposed modified and enhanced GI-LPF based PLL is shown in Figure 4 which can be named as DSOGI-LPF PLL, DTOGI-LPF PLL and DMSTOGI-LPF PLL respectively. The GI-LPF based PLLs utilize two GIs and two adaptive LPFs in $\alpha\beta$ frame for enhanced and accurate phase estimation. Initially, the three phase input voltage v_{abc} is transformed from the *abc* frame to the $\alpha\beta$ frame using the Clark transformation, resulting in the v_α and v_β. Subsequently, v_α and v_β are fed into the dual GIs, producing orthogonal signals v'_α, v'_β, qv'_α and qv'_β are then passed on to the positive sequence calculation (PSC) unit to extract the fundamental frequency positive sequence (FFPS) components. The corresponding FFPS components (v^+_α and v^+_β), are derived through the instantaneous symmetrical components (ISC) method [21] which is crucial for the precise and efficient operation of the PLLs for accurate phase estimation for synchronization purpose:

$$v^+_\alpha = 0.5\,(v'_a - qv'_\beta) \tag{7}$$

$$v^+_\beta = 0.5\,(qv'_a + v'_\beta) \tag{8}$$

The GI outputs v^+_α and v^+_β are then inputted into the SRF PLL in synchronously rotating (dq) frame for estimating the frequency and phase angle of the utility grid voltage in case of GI based PLLs. The proposed improved model is constructed with the employment of an adaptive LPF after the extracted FFPS components v^+_α and v^+_β by the GI filter prior to sending the input signal to the SRF PLL. Now, the extracted signals v^{++}_α and v^{++}_β after the LPF act as inputs for the SRF PLL for accurate phase tracking. The GI-LPF PLL design exhibits better filtering capacity along with effective DC offset elimination which results in accurate phase tracking. Other solutions in literature include placing different filters [8], [11], [13], [14], multiple filters or more filters in combination to the aforementioned GI based filters [15], [16], [18]-[22], [24] but were either incapable of rejecting the effects of both the issues or else the increased system complexity hampered the system response furthermore. The proposed PLLs in this paper use the concept of employment of LPF after the GI based adaptive filters in the PLL's control loop for performance improvement with system simplicity and faster response with precise phase estimation. An effective yet simple technique of DC offset elimination based on use of adaptive LPF has been proposed to remove the DC offsets with harmonics from the input voltage signal before passing it on to the SRF PLL for precise phase extraction. It is basically an add-on to any GI based PLLs without altering the GI filter's bandwidth design. Unlike previous methods, the application of the proposed method for DC offset removal has a minimal effect on the dynamic performance of the PLL under study. The proposed simple yet effective solution for enhanced synchronizing ability is achieved through an adaptive first order LPF whose cut-off frequency (ω_c) has been set to a higher value for disturbance rejection ability [28]. The value of ω_c has been set to 50pi rad/s as the value of cut-off frequency (f_c) of the LPF is 25 Hz. The transfer function expression of the used LPF is expressed as follows:

$$LPF(s) = \frac{\omega_c}{s + \omega_c} \tag{9}$$

By choosing an optimal *k* value [21], the GI-LPF based PLL ensures enhanced dynamic response and filtering capacity and also frequency adaptability under any complex grid condition by sending the extracted grid frequency $\hat{\omega}$ as an input to the GI filters leading to accurate phase angle tracking. The upcoming result section will confirm the bridging of the research gap through the simulation-based results of the existing GI based PLLs and the proposed GI-LPF based PLLs showcasing the enhanced DC offset and harmonics effect attenuation of the proposed GI-LPF PLLs with a detailed performance evaluation of all the PLLs. The efficacy and robustness of the GI-LPF PLLs over the GI based PLLs will be validated in terms of faster system dynamic response, precission in phase tracking along with the DC offset and harmonics rejection ability to avoid estimation errors for an enhanced synchronization under complex grid condition.

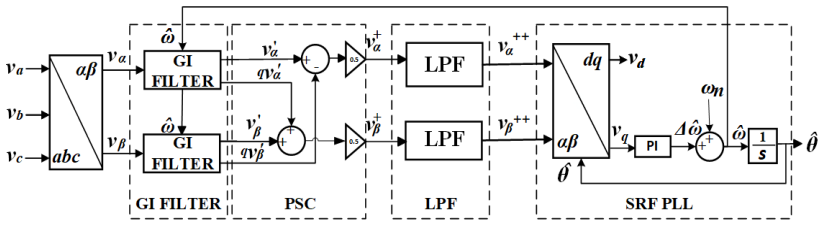

Figure 4. Structure of GI-LPF based PLL

4. COMPARATIVE RESULT ANALYSIS AND DISCUSSION

In this section, the performance of the proposed GI-LPF based PLLs (DSOGI-LPF PLL, DTOGI-LPF PLL and DMSTOGI-LPF PLL) with the standard GI based PLLs (DSOGI PLL, DTOGI PLL and DMSTOGI PLL) has been evaluated in the MATLAB/Simulink environment to analyze their robustness amidst two distorted grid cases. The objective is to check their robustness in phase angle tracking accuracy amidst the grid disturbances occurring between 0.2 seconds and 0.4 seconds, with a total duration of 0.6 seconds. At 0 seconds, the input comprises a balanced utility voltage of amplitude 1 per unit (p.u.) and grid frequency of 50 Hz which is recovered again at 0.6seconds. The investigated two test cases are: test case 1: A two phase voltage sag with 5th and 7th harmonics and test case 2: DC offset present in the grid voltage. For all the PLLs taken into consideration, the actual grid frequency w_n is 100π rad/s, considering actual grid frequency as 50 Hz. The optimized PI parameters values of SRF PLL are proportional gain (k_p=180) and integral gain (k_i=3200) for a fair comparison among all the PLLs. Table I recapitulates evaluation of all the PLLs under the considered test conditions based on settling time (dynamic response), total harmonic distortion (THD) obtained through the fast fourier transform (FFT) analysis and frequency overshoot.

4.1. Two phase voltage sag with 5th and 7th harmonics

A balanced two phase voltage sag with a magnitude of 1 p.u. for a phase and 0.7 p.u. each for b and c phase along with, a 5th harmonic component with amplitudes of (1/5 p.u., 0.7/5 p.u., and 0.7/5 p.u. for each phase), and 7th harmonic component with amplitudes of (1/7 p.u., 0.7/7 p.u., and 0.7/7 p.u. for each phase) is introduced from 0.2 seconds to 0.4 seconds. The Figure 5 represents the simulation responses of all advanced PLLs during a two phase voltage sag with harmonics test case. In Figure 5(a), the three phase grid voltage is depicted, contaminated with a two phase voltage sag, as well as 5th and 7th harmonics. The extracted *dq* outputs of all the PLLs in the *dq* frame are illustrated in Figures 5(b)-(d). The magnitude of extracted d voltage component ((v_d) as 1 p.u.) and q component ((v_q) as 0 degrees) affirm the effectiveness of the PLLs. Figure 5(e)-(g) demonstrate the PLLs precision in tracking the frequency by comparing the grid's actual frequency with the PLL's estimated frequency. Overally, the proposed GI-LPF PLLs demonstrate significant enhancement and superior dynamic performance with enhanced filtering capacity, minimal frequency overshoots and accurate frequency estimation compared to the standard GI based PLLs counterparts. The DTOGI-LPF PLL is the superior one followed by the DMSTOGI-LPF PLL with minimum settling time, overshoot and THD content in the extracted outputs. All the detailed comparative information can be found in Table 1.

In this test case, the SOGI filter based PLLs (DSOGI PLL and DSOGI-LPF PLL) showcase quickest dynamic response due to lower order of the filter and design simplicity. Yet, they exhibit high steady state ripples and more harmonics content in the extracted signals with THD content as 3.35% (DSOGI PLL) and 0.06% (DSOGI-LPF PLL) respectively which is obtained through the FFT analysis. The TOGI filter based PLLs (DTOGI PLL and DTOGI-LPF PLL) showcase slower dynamic response due to increase in order of the filter and complexity. Yet, they exhibit minimum harmonics content in the extracted signals with THD content as 1.35% (DTOGI PLL) and 0.04% (DTOGI-LPF PLL) with least steady state ripples. The MSTOGI filter based PLLs (DMSTOGI PLL and DMSTOGI-LPF PLL) showcase slower dynamic response, more THD content and same steady state ripples as the SOGI based PLLs but faster dynamic response than TOGI based PLLs. The THD content in the extracted signals as 4.25% (DMSTOGI PLL) and 0.23% (DMSTOGI-LPF PLL) respectively are obtained through the FFT analysis. Overally, the proposed methods exhibit roughly faster dynamic response or responsiveness in terms of settling time and better harmonics filtering ability than the standard GI based PLLs. This marks a significant enhancement. Additionally, it boasts the lowest frequency overshoot. Here, the DTOGI-LPF PLL acts as the superior one followed by the DMSTOGI-LPF PLL. Further information can be found in Table 1.

4.2. DC offset present in the grid voltage

From 0.2 seconds to 0.4 seconds, a DC offset is injected of magnitudes of 0.2 p.u. (phase a), 0.1 p.u. (phase b), and -0.2 p.u. (phase c) in the input *abc* grid voltage. The Figure 6 represents the simulation responses of all advanced PLLs during a DC offset affected grid voltage test case. Figure 6(a) illustrates the polluted three phase voltage because of the DC offsets existence. The extracted *dq* outputs of all the PLLs in *dq* frame are depicted in Figures 6(b)-(d). Figures 6(e)-(g) demonstrate the accuracy in tracking the frequency with a comparison of each PLL's estimated frequency with the fundamental grid frequency that is 50 Hz. The MSTOGI filter based PLLs are proficient in estimating the grid's phase angle accurately under DC offset conditions. The SOGI and TOGI filter based PLLs with and without the LPF fail in estimating the grid variables accurately under this test condition exhibiting high steady state oscillations. The DMSTOGI-LPF PLL proves to be the best for faster phase estimation and precise synchronization with nill frequency overshoot and a faster response with least settling time than the DMSTOGI PLL. The detailed analysis can be found from Table 1.

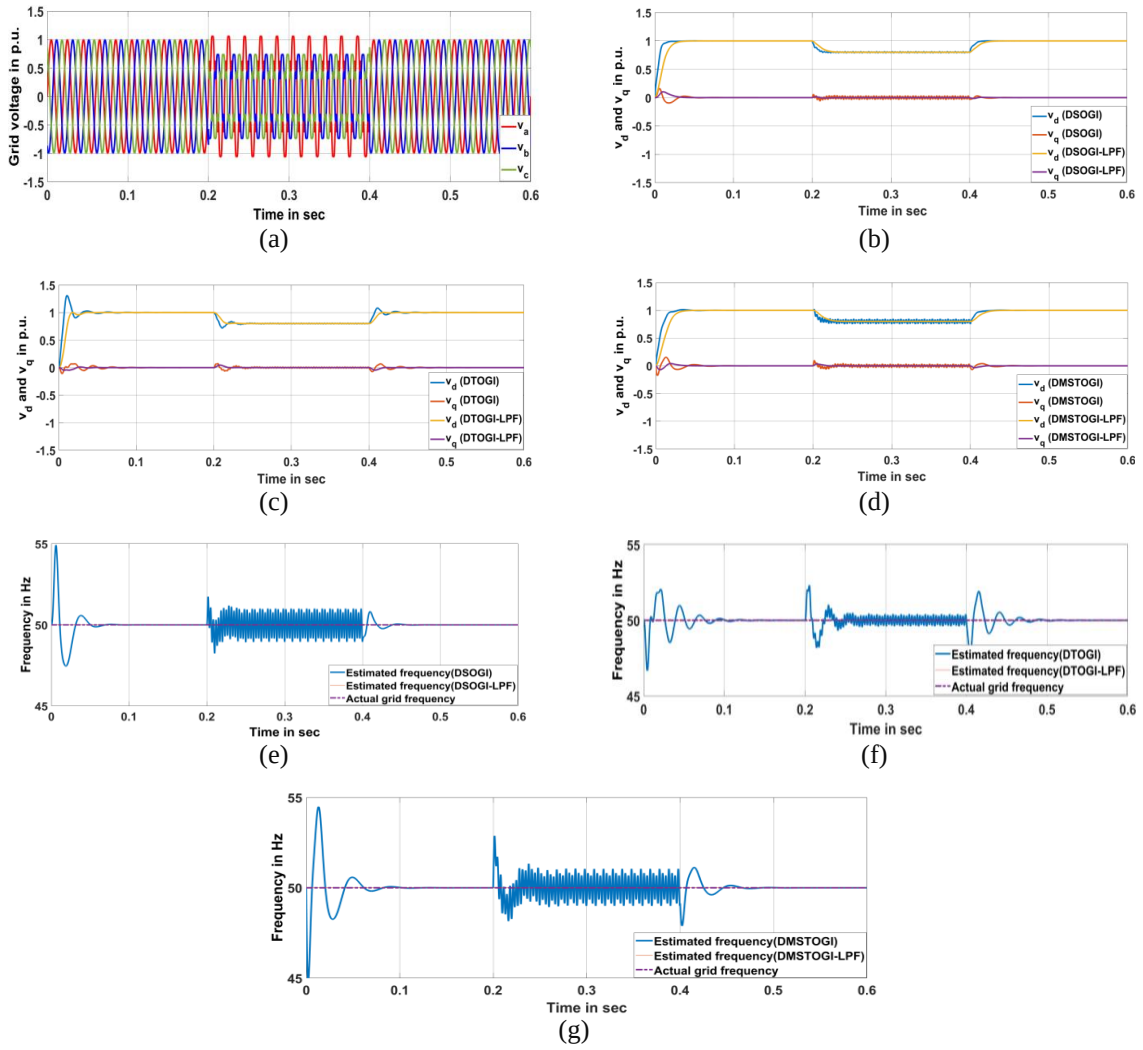

Figure 5. Simulation responses of all advanced PLLs during two phase voltage sag with harmonics: (a) polluted grid voltage in *abc* frame, (b) DSOGI and DSOGI-LPF PLLs response in *dq* frame, (c) DTOGI and DTOGI-LPF PLLs response in *dq* frame, (d) DMSTOGI and DMSTOGI-LPF PLLs response in *dq* frame, (e) actual and estimated frequency comparison of DSOGI and DSOGI-LPF PLL, (f) actual and estimated frequency comparison of DTOGI and DTOGI-LPF PLL, and (g) actual and estimated frequency comparison of DMSTOGI and DMSTOGI-LPF PLL

Table 1. Comparative results analysis

	DSOGI PLL	DSOGI LPF PLL	DTOGI PLL	DTOGI LPF PLL	DMSTOGI PLL	DMSTOGI LPF PLL
Test case 1: A two phase voltage sag with 5th and 7th harmonics						
Settling Time (After step change)	0.02 secs	0.01 secs	0.03 secs	0.018 secs	0.025 secs	0.018 secs
THD	3.35%	0.06%	1.35%	0.04%	4.25%	0.23%
Peak to peak frequency error	2.0 Hz	_	0.8 Hz	_	2.0 Hz	_
Frequency Overshoot	_	0 Hz	_	0 Hz	_	0 Hz
Test case 2: DC offset present in the grid voltage						
Settling Time (After step change)	_	_	_	_	0.06 secs	0.02 secs
Peak to peak frequency error	_	_	_	_	0 Hz	0 Hz
Frequency Overshoot	_	_	_	_	2 Hz	0 Hz

Under this test case, the response of the MSTOGI filter based PLLs (DMSTOGI PLL and DMSTOGI-LPF PLL) stands out superior there by having an ability to reject the impact of DC offsets present in grid voltage for an accurate phase estimation and grid synchronization. Whereas, it is evident that SOGI based PLLs (DSOGI PLL and DSOGI-LPF PLL) and TOGI based PLLs (DTOGI PLL and DTOGI-LPF PLL) exhibit steady state oscillations in response to the DC offset. The DMSTOGI-LPF PLL displays nill frequency overshoot as 0 Hz and a faster response or a settling time within a very less time as 1 cycle. While, the DMSTOGI PLL displays a frequency overshoot of 2 Hz and a slower response with settling time as 3 cycles in comparison to the DMSTOGI-LPF PLL. In contrast, both the SOGI and TOGI filters based PLLs fail to operate in tracking the grid frequency and phase when the DC offset is present in the input signal. The MSTOGI filter based PLLs prove their efficacy in an enhanced phase tracking ability with DC offset rejection. The proposed DMSTOGI-LPF PLL presents excellent performance with fastest response, minimum overhoot, accurate and faster phase estimation and precise synchronization.

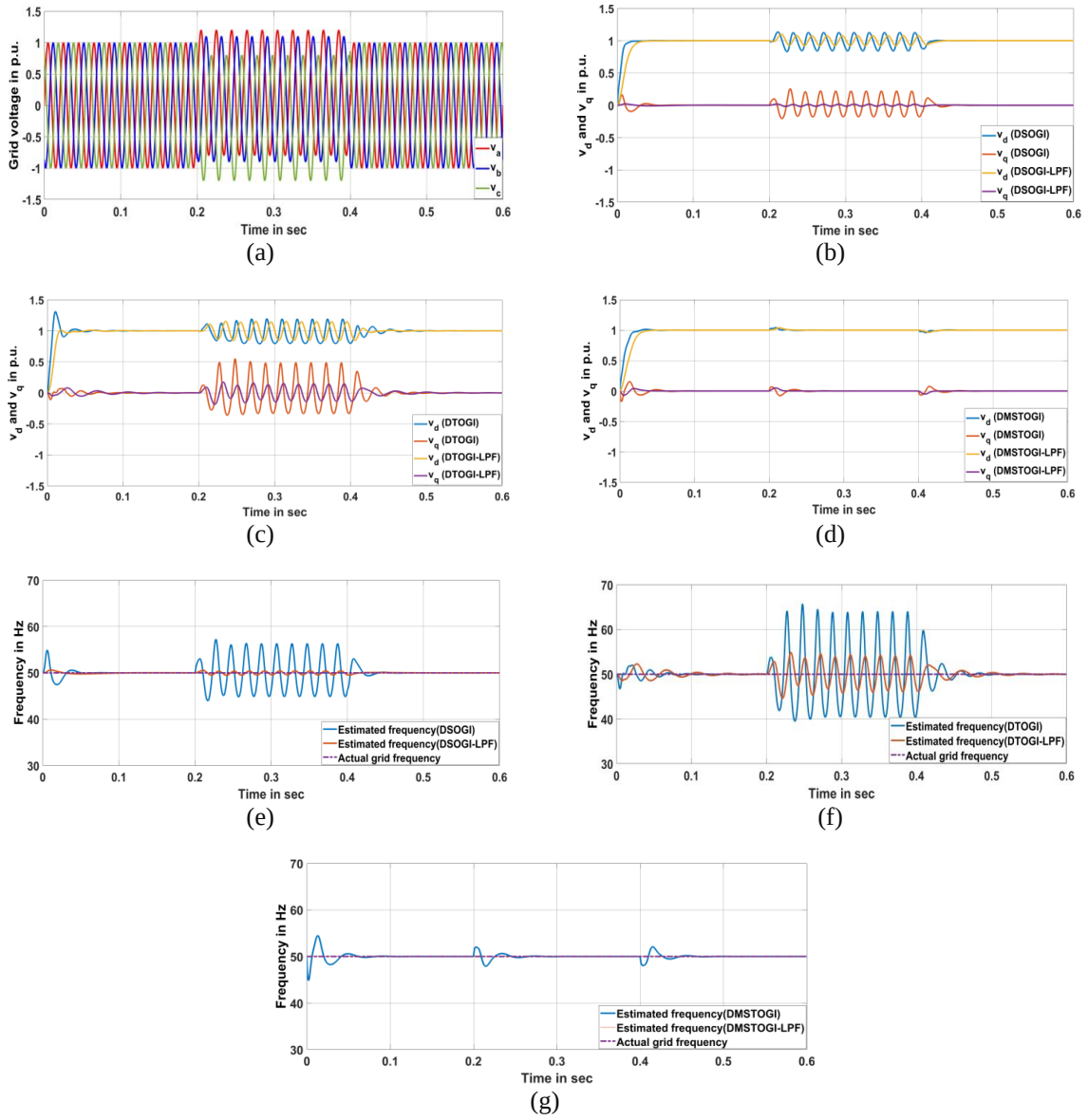

Figure 6. Simulation responses of all advanced PLLs during DC offset in grid voltage: (a) polluted grid voltage in *abc* frame, (b) DSOGI and DSOGI-LPF PLLs response in *dq* frame, (c) DTOGI and DTOGI-LPF PLLs response in *dq* frame, (d) DMSTOGI and DMSTOGI-LPF PLLs response in *dq* frame, (e) actual and estimated frequency comparison of DSOGI and DSOGI-LPF PLL, (f) actual and estimated frequency comparison of DTOGI and DTOGI-LPF PLL, and (g) Actual and estimated frequency comparison of DMSTOGI and DMSTOGI-LPF PLL

5. CONCLUSION

This paper presents an analysis and evaluation of the standard GI based PLLs and proposed novel GI-LPF based PLLs, considering two distorted utility conditions such as two phase voltage sag with 5th and 7th harmonics and the DC offsets present in the grid voltage. The proposed GI-LPF PLLs (DSOGI-LPF PLL, DTOGI-LPF PLL and DMSTOGI-LPF PLL) demonstrate superior dynamic performance with enhanced filtering capacity, minimal frequency overshoots and accurate frequency estimation compared to the standard GI based PLLs (DSOGI PLL, DTOGI PLL and DMSTOGI PLL). It is observed that under two phase voltage sag with 5th and 7th harmonics, the dynamic response and THD content of extracted signals through FFT analysis determine the filtering efficiency of DTOGI-LPF PLL as the superior one followed by the DMSTOGI-LPF PLL. On the other hand, the DMSTOGI-LPF PLL demonstrates strongest performance in the presence of DC offset. The proposed GI-LPF based PLLs enhance the standard GI based PLLs performance in terms of improved dynamic response, harmonics filtering and precise phase tracking. Consequently, it is inferred form the simulation results-based analysis carried out in MATLAB for comparison that among all the PLLs, the proposed DMSTOGI-LPF PLL exhibits superior performance under the two test cases with two phase voltage sag with 5th and 7th harmonics and DC offset rejection capabilities, enhanced phase tracking and dynamic response. The findings shed light on the performance accomplishment of GI-LPF based PLLs under various disturbance conditions making them appropriate for robust grid synchronization techniques.

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AUTHOR CONTRIBUTIONS STATEMENT

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Poonam Tripathy	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓			
Banishree Misra				✓	✓					✓		✓		
Byamakesh Nayak					✓					✓		✓		

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

- The authors confirm that the data supporting the findings of this study are available within the article [and/or its supplementary materials].

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