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An investigation of different low-power circuits and enhanced energy efficiency in medical applications

Prabhu R., Sivakumar Rajagopal
Department of Sensor and Biomedical Technology, School of Electronics Engineering, Vellore Institute of Technology, Vellore, India

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ABSTRACT

This research investigates the application of low-power circuits in medical devices and imaging systems. The primary goal is to address the growing demand for energy-efficient solutions in medical applications. There is an increasing need for energy-efficient solutions due to the development of medical technologies, particularly implanted and battery-operated medical devices. This paper explores the integration of adiabatic logic as a critical enabler for achieving low power consumption in medical applications. The study looks into different low-power circuit designs and technologies that optimize power usage without sacrificing performance. Adiabatic circuits offer a promising substitute for conventional circuitry in low-energy design. The research examines several low-power circuit designs and technologies that maximize power efficiency without compromising functionality. In low-energy design, adiabatic circuits present a possible alternative to traditional circuitry. Adiabatic logic aims to create energy-efficient digital circuits that consume significantly less power than conventional complementary metal-oxide-semiconductor (CMOS) circuits. We accomplish this by recovering and recycling energy that would otherwise be lost as heat and carefully controlling energy flows during switching events. Adiabatic logic is precious in battery-operated and energy-constrained devices.

Corresponding Author:

Sivakumar Rajagopal
Department of Sensor and Biomedical Engineering, School of Electronics Engineering,
Vellore Institute of Technology
Vellore, India
Email: rsivakumar@vit.ac.in

1. INTRODUCTION

The continuous evolution of medical technologies has propelled the development of sophisticated devices that play a pivotal role in patient monitoring, diagnostics, and therapeutic interventions. In portable, implantable, and battery-operated medical devices, energy efficiency is paramount for prolonged operation, reduced intervention, and enhanced patient comfort [1]. This paper investigates integrating low-power techniques, with a specific emphasis on adiabatic logic, to address the growing energy challenges in the medical domain. The challenge of reducing power consumption in medical devices, which is critical for extending battery life and improving patient comfort. Adiabatic logic, distinguished by its capacity to reduce energy dissipation during logic operations, offers a potentially advantageous approach to attaining notable decreases in power consumption in medical equipment. Despite being widely used, conventional complementary metal-oxide-semiconductor (CMOS) circuitry frequently has power efficiency issues, mainly when longer battery life is essential [2]. There are still problems that need to be handled, such as the requirement for more power consumption reduction and better component integration for downsizing, despite these advances.

Adiabatic logic is a desirable option for energy-sensitive medical applications since it is designed to minimize dynamic power dissipation during charging and discharging cycles [3]. To enhance the functionality of these circuit designs, specific design approaches are used nowadays to preserve the circuit's scalability and dependability without sacrificing their original characteristics. The general benefits of having a circuit model based on VLSI's are shown in Figure 1 [4].

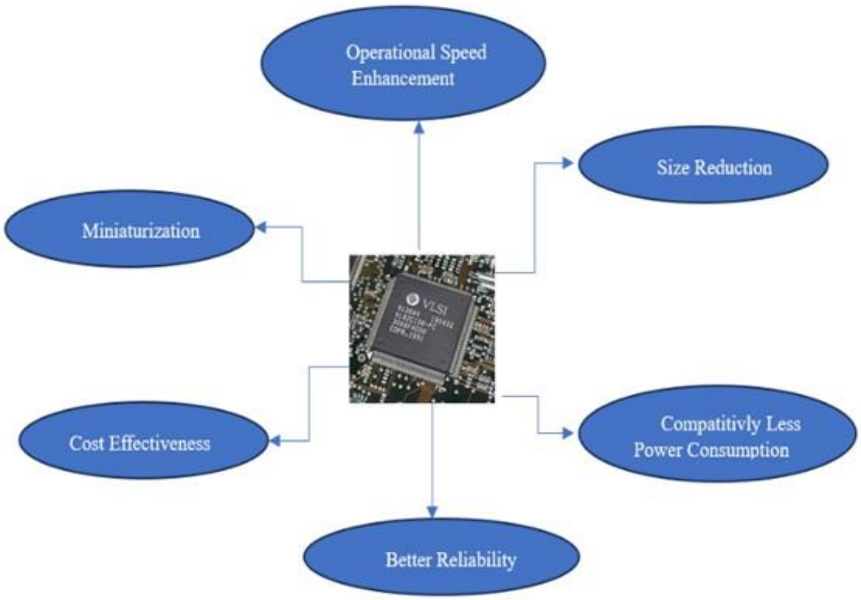

Figure 1. Merits of VLSI design

Full adder circuits are vital components of digital systems because they carried out the crucial addition arithmetic function. They are an important area of study for low-power design techniques because of their efficiency and performance, which have a direct impact on the total energy consumption and computational speed of digital circuits. The energy-sensitive uses of conventional CMOS-based full adder designs are limited, particularly when it comes to implantable and portable medical devices, because of the considerable power dissipation caused by static and dynamic power components. By utilizing energy recovery techniques to reduce dynamic power dissipation during switching transitions, adiabatic logic circuits present a viable substitute for traditional CMOS logic. In order to reduce power consumption and heat generation, adiabatic circuits work by transferring energy between the circuit's capacitance and inductance components. Because of this, adiabatic logic is a popular option for low-power digital circuit design suited for energy-efficient medical equipment [5].

This is how the paper is structured: low power principles are followed by different levels of low power techniques and the design of low power strategies. The following section discusses various types of adiabatic logic and how they operate. It also provides a literature review and analysis. The conclusion includes a discussion of the procedure and results. Lastly, the paper's conclusion and next steps are discussed.

2. LOW POWER CONCEPTS

Power dissipation is a primary concern in many applications, particularly those based on high-performance, portable, battery-operated devices. Power dissipation is the rate at which energy is taken from the source and converted into heat (electrical energy is converted into heat energy during operation). In CMOS circuits, power dissipation occurs in two ways: dynamic and static, as shown in Figure 2. Circuit switching is the source of dynamic power dissipation. A greater working frequency causes the circuits to switch ON and OFF more frequently, which increases power dissipation. Rather than being tied to changing operations, static power dissipation is related to the logical states of the circuits. Leakage current is the sole cause of static power dissipation in CMOS logic. However, static current drawing can occur when there are sporadic departures from the rigid CMOS style logic [6].

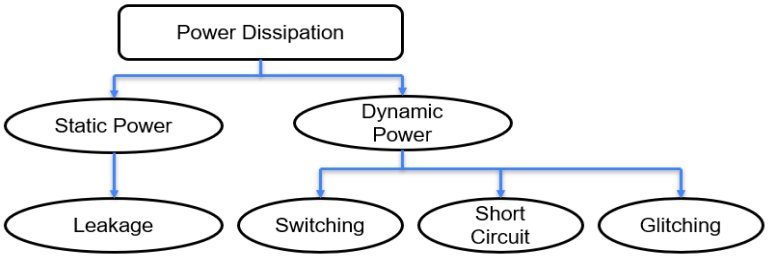

Figure 2. Types of power consumption

2.1. Static power dissipation

Static power, sometimes called quiescent mode, is used without circuit activity. Static power consumption is the amount of energy a circuit will need even if the clocks are removed, and the inputs are left unchanged when the supply voltage is there. Leakage currents that flow while the transistor is off-state are mostly to blame. The formula for static power dissipation (Pstatic) is often expressed as (1).

$$Pstatic = I_{Leak} * V_{DD} \quad (1)$$

Where
I_{Leak} is the leakage current
V_{DD} is the supply voltage

Various forms of leakage current exist in circuits; sub-threshold leakage current arises when current flows between the source and the drain. This is the main source of power that is static. The gate-to-body substrate is where the next gate leakage current occurs. The final one is junction leakage current, which flows from the body's source to its substrate. Leakage current passing via the reverse bias junction of transistors is the cause of static power dissipation, as shown in Figure 3. At room temperature, the leakage current per unit drain surface ranges typically from 10 to 100p A/μm^2.

If we reduce the static power dissipation, we have to adjust the transistor sizes and increase the threshold voltage, which can help minimize subthreshold leakage. Use strategies such as power gating, which entails shutting down portions of the circuit when it's not in use. This reduces leakage in those places by cutting the power supply to passive blocks or modules [7].

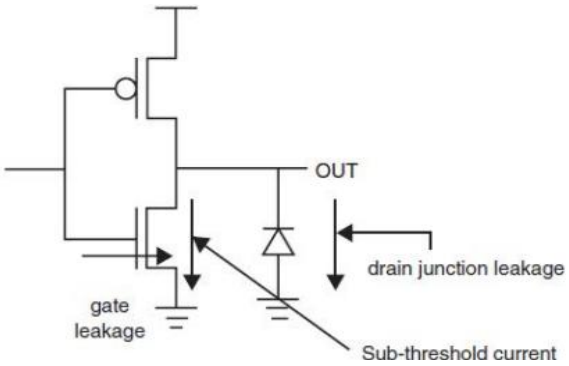

Figure 3. Leakage currents in CMOS inverter

2.2. Dynamic power dissipation

Dynamic power dissipation happens when electronic components, such as transistors in digital circuits, are actively switched. The charging and discharging of capacitive loads are connected to the device's alternating logic state. The short circuit power is present, while the NMOS and PMOS networks are only partially operational.

Whenever input signals in the circuit are changed its state with time, and it causes some power dissipation. Dynamic power is required to charging and discharging the load capacitance when transistor input switches.
When the input switches from 1 to 0 the PMOS transistor (PULL UP network) turns ON and charges the load to VDD. And that time energy stored in the capacitance is:

$$Ec = \frac{1}{2} C_L V_{DD2} \quad (2)$$

The energy delivered from the power supply is:

$$Ec = C_L V_{DD2} \quad (3)$$

Observed that only half of the energy from the power supply is stored in the capacitor. The other half is dissipated (converted to heat) in the PMOS transistor because the transistor has a voltage across it while the current flows through it. The dissipated power depends only on the load capacitance, not on the transistor or the speed at which the gate switches. When the input switches from 0 to 1, the PMOS transistor turns off, and the NMOS transistor is turned ON, discharging the capacitor. The energy stored in the capacitor is dissipated in the NMOS transistor, as shown in Figure 4. No energy is drawn from the power supply in this case. The dynamic power dissipation can be calculated as follows:

$$\text{PDynamic} = \propto * C_L * V_{DD}^2 * f_{clk} \quad (4)$$

Where:
$\propto$ = Switching activity
C_L = Loading capacitance
V_{DD} = Power supply
f_{clk} = Clock frequency

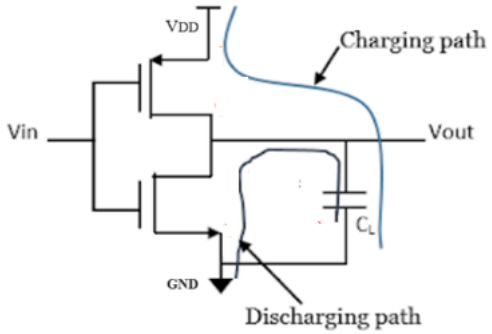

Figure 4. Dynamic power dissipation in CMOS inverter

If the dynamic power dissipation is reduced by using clock gating techniques and transistor sleep mode. lower supply voltage until the circuit functions as intended. power-down mode in order to minimize frequency as much as possible without significantly compromising performance.

Short circuit power is one component of dynamic power. When a gate switches at the input, it happens in CMOS. When a direct path exists between VDD and GND and both PMOS and NMOS are operational for a brief period of time. Temporary spikes in the current will occur during this scenario, as depicted in the Figure 5. The goal of short-circuit power minimization is to increase the circuit's overall dependability and efficiency. Integrated circuits are designed to reduce the effects of short-circuit power through the use of strategies such transistor size, logic restructuring, and dynamic power management.

The finite delay of the gates results in the generation of glitching power, which is the third form of dynamic power dissipation. Glitching is worth mentioning here since it can be a major source of signal activity and is directly proportional to the number of output transitions of a logic gate. When routes in the circuit converge at the same point but have different propagation delays, glitches frequently happen. Glitches happen when the input signals to a certain logic block arrive at different times, leading to a series of

intermediate transitions occurring before the logic block's output stabilizes. Power dissipation from these extra transitions is referred to as the glitching power.

All power losses in traditional CMOS circuits are associated with dynamic (Pdyn) short circuit (Psc) and leakage power (Pleak) as shown in (5).

$$P\,total = P\,Dynamic + P\,short\,circuit + P\,Static \quad (5)$$

$$= CL * Vdd * Fclk + Isc * Vdd + Ileak * Vdd \quad (6)$$

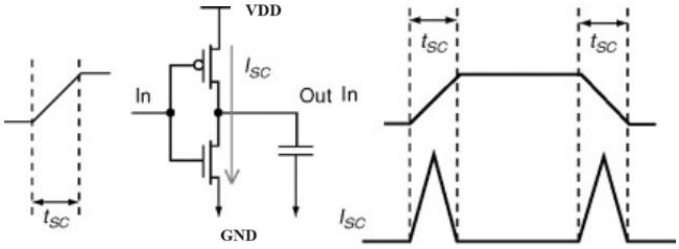

Figure 5. Short circuit power dissipation

2.3. Significance of low power medical devices

Low-power design in medical devices is of significant importance and relevance due to several critical factors in the healthcare industry. Here are some reasons why low-power design is crucial for medical devices:

Many medical devices, especially those designed for implantable and wearable applications, rely on batteries for power. Low-power design extends the battery life of these devices, reducing the frequency of battery replacements and enhancing the longevity of the device's operation. Prolonged battery life is essential for implantable medical devices such as pacemakers, neurostimulators, and insulin pumps, minimizing the need for invasive procedures to replace the power source. Low-power design enables the development of implantable and wearable devices that can continuously monitor health parameters without causing discomfort or adverse effects [8]. Low-power design is crucial for medical imaging devices that incorporate wireless communication technologies, such as Wi-Fi or Bluetooth. Reduced power consumption in communication modules ensures efficient data transfer without draining the device's power source [9].

3. LOW POWER DESIGN STRATEGIES

Low-power approaches reduce power consumption in electrical systems and circuits without compromising functionality. In many domains, low power is achieved using a variety of tactics and approaches [10]. The following are some typical low-power strategy types is shown in Figure 6.

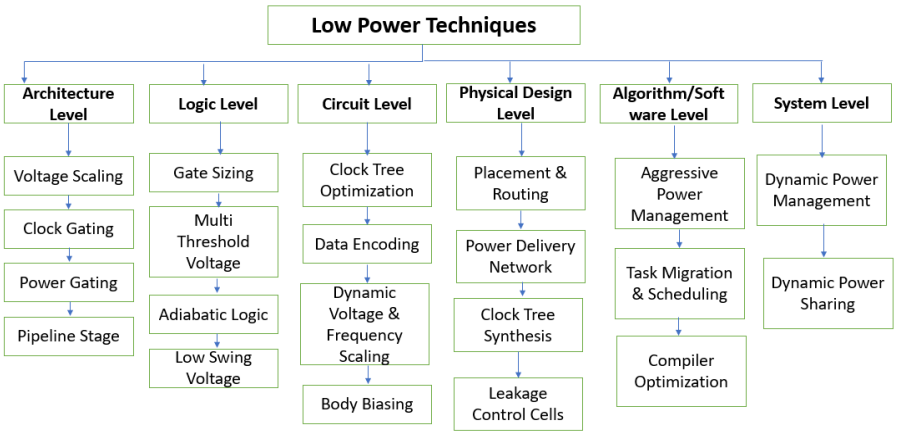

Figure 6. Low power techniques

3.1. Decrease in power at the level of architecture

The architecture level of low-power VLSI design involves considerations and techniques at the system or chip architecture level to achieve energy efficiency and minimize power consumption. Power management strategies that shut down unused blocks. Low-power systems using pipelining, parallelism, Clock and power gating.

a) Clock gating: clock gating is the process of selectively cutting off the clock signal to particular circuit segments when there is little to no activity. Actually, it prevents needless clock toggling in the circuit's idle sections, which lowers dynamic power usage as shown in Figure 7. Well, it focuses primarily on dynamic power, while adiabatic logic seeks to maximize energy efficiency overall, taking into account both static and dynamic power.

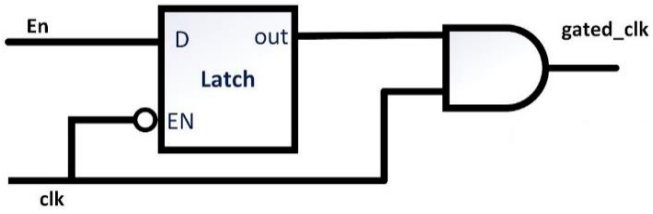

Figure 7. Clock gating for power reduction

b) Power gating: power gating involves completely turning off power to certain circuit blocks when they are not actively processing data. This technique helps minimize static power consumption as shown in Figure 8. If sleep=0, the PMOS and NMOS both sleep transistors are ON. So, the normal inverter operation is done. When sleep = 1, the sleep transistors are OFF. So, there is no direct path from power rails to ground, and hence no leakage of power is dissipated due to the pull-up and pull-down networks. Although adiabatic logic and standard power gating have similar goals, adiabatic logic focuses on recovering energy during transitions [11].

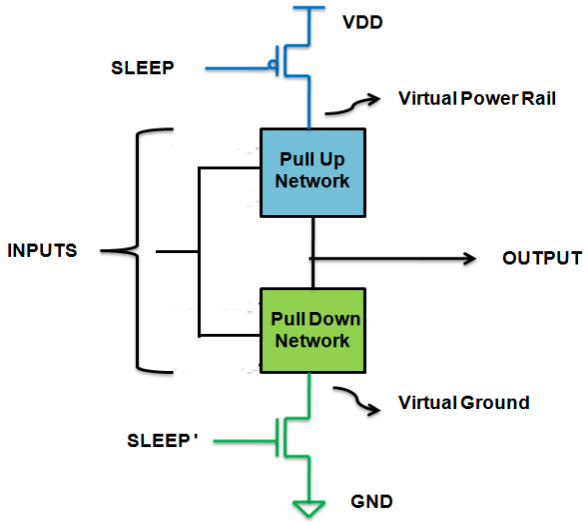

Figure 8. Power gating

c) Voltage scaling: dynamic voltage and frequency scaling (DVFS) involves adjusting the operating voltage and frequency based on the workload. Lowering the voltage during periods of lower activity helps reduce power consumption [12]. While adiabatic logic is more focused on energy recovery during transition, dynamic optimization shares the same objective but functions at a different level (voltage and frequency scaling).

3.2. Decrease in power at the level of logic/circuit

Power consumption is reduced in low-power VLSI designs at both the logic and circuit levels. Using logic optimization lessens the switching activity. Clever circuitry that minimizes internal swing and the number of devices. Adiabatic circuits are considered a logic-level technique because they operate at the digital logic level, influencing the way logic gates and circuits perform their fundamental operations.

a) Multi voltage design: it uses multiple voltage domains in a system, allowing different blocks or components to operate at different voltage levels. Enables finer control over power consumption, allowing low-power operation in specific circuit sections as shown in Figure 9. It complements adiabatic logic by providing finer control over power consumption in different areas, especially when combined with dynamic voltage scaling [13].

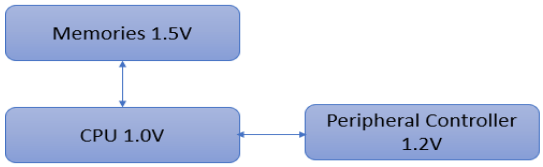

Figure 9. Multiple voltage design techniques

b) Transistor sizing: transistor sizing is a crucial aspect of digital circuit design, and it involves determining the physical dimensions of transistors within the circuit. The size of transistors significantly influences the performance and characteristics of the circuit, including speed, power consumption, and area. In digital CMOS technology, which is widely used for integrated circuits, transistor sizing is particularly important. The adiabatic logic is more concentrate on power dissipation [14].

3.3. Decrease in power at the physical design level

Optimizing component arrangement and connectivity to reduce power consumption while satisfying performance and space requirements is known as physical design power reduction.

a) Placement and routing: placement and routing determine the physical arrangement and connections of components on a chip. It involves determining the optimal location for each block to meet design goals such as performance, area, and power consumption. It is optimized for signal timing, and balance power and thermal considerations.

b) Power delivery network (PDN): the PDN is a crucial aspect of chip design responsible for supplying power to all the functional blocks on the chip. It consists of power grids and distribution networks. Minimize voltage drop, control noise, and ensure stable and reliable power delivery to all components [15].

c) Clock tree synthesis: clock tree synthesis is a process in digital circuit design that involves the generation of a clock distribution network. The goal is to efficiently deliver clock signals to all sequential elements (flip-flops, registers) on the chip. Minimize clock skew (variation in arrival times of clock signals), balance loads on different branches, and ensure stable and reliable clock signals.

In conclusion, adiabatic logic differs from conventional low-power approaches in that it strongly emphasizes energy recovery during transitions. Depending on the unique needs and features of the intended application, a technique or combination of methods may be chosen.

4. ADIABATIC LOGIC OPERATION

An approach to digital logic circuit design called adiabatic logic lowers energy loss during the ON and OFF switching of logic gates. It originates from the thermodynamic concept of adiabatic processes, which are energy transfers without the need for heat exchange. Adiabatic logic achieves its low-power characteristics by precisely controlling energy fluxes within digital circuitry.

Adiabatic logic is a digital logic design process that uses specialized techniques to recover and recycle energy that is generally wasted as heat during switching events, lowering energy consumption during the operation of digital circuits. The adiabatic operation principle has undergone significant design revisions. Each phase of the power clock determines two basic design principles for adiabatic circuits.

– Transistors should never be turned ON when voltage is applied from the source to the drain.
– Transistors should never be turned off while current is flowing through the circuit.

Now let's look at the simplified resistive-switch network shown in Figure 10. Ecurr = IR CV represents the energy dissipation throughout the charging process because the constant supply voltage level, V, has been replaced by a constant current source, I. The voltage drop across the switch is IR. I, the charging current, is determined by dividing CV by T, the charging time required to charge C from 0 to V [16].

$$\text{The Voltage across the switch} = \text{IR} \tag{7}$$

$$\text{P(t)} = I^2 \text{ R} \tag{8}$$

$$\text{Energy during charge (E)} = (I^2 \text{ R}) \text{ T} \tag{9}$$

$$\text{Also Q} = \text{CV, So Q} = C_L \text{ VDD, I} = \frac{\text{CV}}{\text{T}} \tag{10}$$

$$\text{T} = \frac{\text{CV}}{\text{I}} \tag{11}$$

$$\text{E} = (I^2 \text{ R})\text{T, } = \frac{C^2 V^2 \text{R}}{\text{T}} \tag{12}$$

Where
E = energy lost while the device was charging.
Q = transmission of charge to the load.
C= the capacitance's value.
R= resistance when the MOS switch is activated.
V= ultimate voltage at the load value.
T= the amount of time needed to charge.

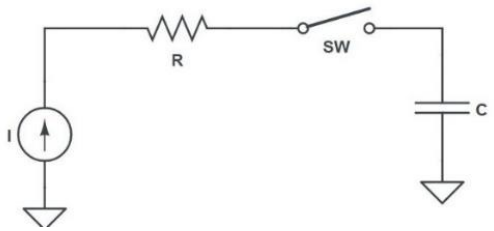

Figure 10. Adiabatic switching circuits

If the charging period T exceeds 2RC, less energy is dissipated than in the traditional scenario. In other words, by lengthening the charging period, the expended energy can be arbitrarily reduced. Furthermore, in contrast to the traditional scenario where the dissipation is dependent on the capacitance and the voltage swing, the dissipated energy is proportional to R. As a result, decreasing the PMOS network's on-resistance will lower its energy dissipation. Adiabatic logic uses a power clock to control the charging and discharging of the circuit's capacitive nodes, allowing for adiabatic switching. These stages, as seen in Figure 11, reflect different depths at which specific tasks are performed [17].

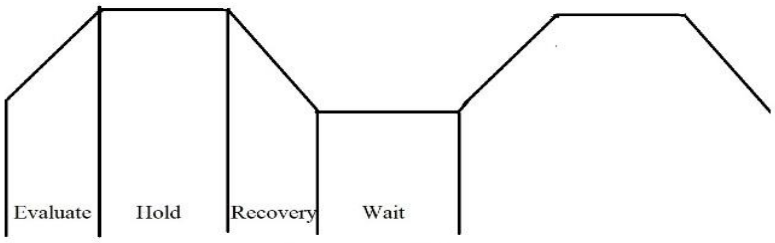

Figure 11. Adiabatic trapezoidal waveform

- Evaluate: the power supply increases gradually from low to high, the inputs stay constant, and the output follows the power supply to become valid based on the outcome of the pre-evaluation.
- Hold: the power supply remains high to keep the output valid and providing the constant input for the next stage in the adiabatic pipeline. Inputs also come back to zero.
- Recover: the power source shuts off again. Cross-coupled P-MOSFETs enable charge stored in the node capacitance to flow back to the power source when the zero input closes the channel to the ground.
- Wait: power supply initially remains at zero, inputs become legitimate, evaluation logic produces a pre-evaluated result, and low voltage output is produced.

4.1. Adiabatic logic structures

There are two types of adiabatic logic structures.

a) Partly/quasi adiabatic logic

Circuits that are almost adiabatic: some charge is moved to the earth and some heat is released. Therefore, only a portion of the energy may be recovered; nonetheless, compared to fully adiabatic logic circuits, these circuits are simpler to implement. The following are examples of popular partly adiabatic families.

- Efficient charge recovery logic (ECRL)
- 2N-2N2P adiabatic logic
- Positive feedback adiabatic logic (PFAL)
- NMOS energy recovery logic (NERL)
- Clocked adiabatic logic (CAL)
- True single-phase adiabatic logic (TSEL)
- Source-coupled adiabatic logic (SCAL)

b) Fully adiabatic logic

The load capacitance recovers all of its charges and provides feedback to the power source in fully adiabatic circuits. This makes fully adiabatic circuits more complex and slower than partial adiabatic circuits.

- Pass transistor adiabatic logic
- Split rail charge recovery logic (SCRL)

4.2. Efficient charge recovery logic

ECRL is a form of adiabatic logic, where the term "adiabatic" refers to a reversible thermodynamic process. Adiabatic logic aims to minimize energy dissipation by ensuring that the charging and discharging of capacitive nodes are as energy-efficient as possible. The primary goal of ECRL is to recover and efficiently reuse the charges stored in the load capacitance, minimizing energy losses and improving the overall energy efficiency of the logic circuits shown in Figure 12 [18].

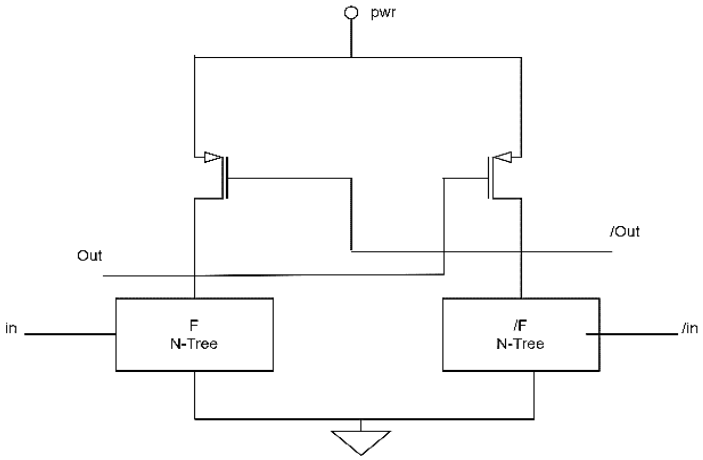

Figure 12. Schematic diagram of ECRL

The three phases of a charging cycle are: adiabatic charging (managed charging of the load capacitance with low energy dissipation), hold (maintaining the voltage across the load capacitance without

significant power dissipation), discharging (efficiently transferring charges from the load capacitance to the output), and recovery (storing recovered charges for use in the subsequent charging cycle). Energy-harvesting and low-power systems are two examples of applications where energy efficiency is critical and ECRL is frequently taken into consideration. It can be utilized in a variety of digital circuits, such as those found in portable electronics, internet of things (IoT) devices, and biomedical equipment.

4.3. Positive feedback adiabatic logic

PFAL is a specific type of adiabatic logic design that employs positive feedback to enhance the efficiency of energy transfer during both the charging and discharging phases of a digital circuit. The positive feedback mechanism is crucial for amplifying the voltage swing across the load capacitance, leading to improved energy recovery.

The load capacitance can be charged under control by turning on the adiabatic charging phase. Beyond what would be possible with straightforward charging, the voltage on the load capacitance is amplified by additional transistors or components creating a positive feedback loop. When the system reaches the adiabatic hold phase, no appreciable power dissipation occurs and the voltage across the load capacitance is maintained. Enabled the discharge phase to effectively move charges from the output capacitance to the load capacitance. In the recovery phase, any leftover charges are extracted and saved for later use during the charging cycle shown in Figure 13.

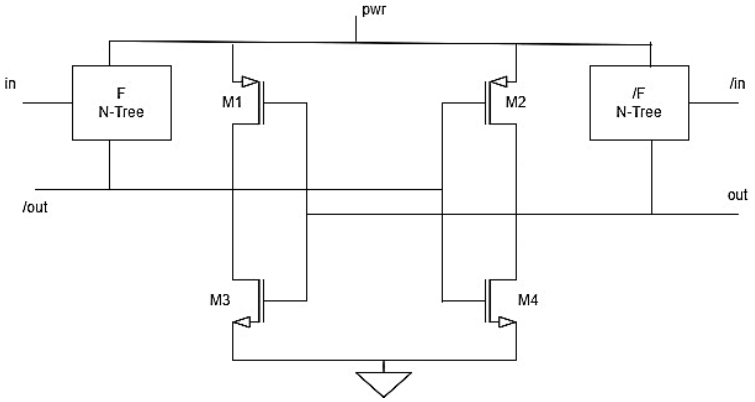

Figure 13. Schematic diagram of PFAL

4.4. Clocked adiabatic logic

The working principle of clocked adiabatic logic (CAL) involves synchronous operation with the assistance of a clock signal (CX) to control and coordinate the charging, discharging, and recovery phases of the digital circuit. CAL aims to minimize energy dissipation during these phases, making it suitable for low-power applications shown in Figure 14.

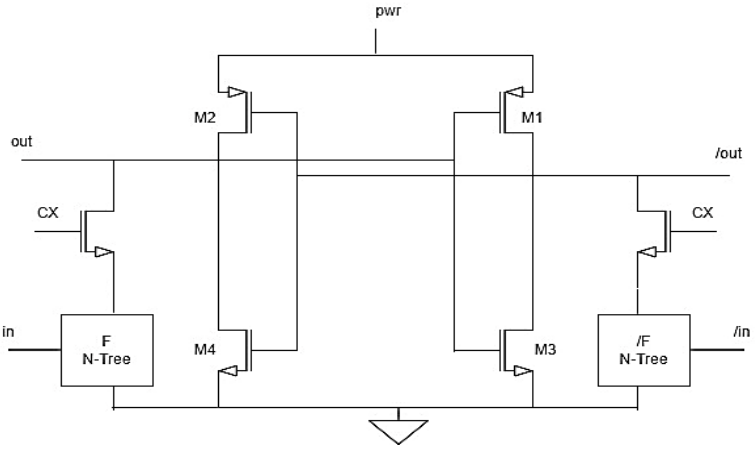

Figure 14. Schematic diagram of CAL

The clock signal controls the CAL charging phase, which charges the load capacitance. The charging procedure is timed to coincide with the clock signal's rising edge. The length of the charging phase is set by the clock signal. enters the CAL hold phase, which maintains the voltage across the load capacitance. The circuit maintains its state until the subsequent clock cycle, and the clock signal guarantees synchronous operation. turned on to effectively transfer charges from the Cload to the output during the adiabatic discharging phase. The discharging procedure is timed to coincide with the clock signal's falling edge. Additionally, any leftover charges are retrieved and saved for later use during another charging cycle. Exact control over every stage is possible with synchronous operation. reduces the amount of energy lost throughout the charging and discharging processes. It can be applied to Internet of Things applications, energy-constrained systems, and portable gadgets.

4.5. 2N-2N2P adiabatic logic

The 2N-2N2P adiabatic logic is a design that employs two N-type transistors and two P-type transistors in a specific configuration shown in Figure 15. During the adiabatic charging phase, P2 is turned on to charge the load capacitance (Cload) through the path provided by N2. Energy is stored in Cload during this phase. The system enters the adiabatic hold phase where the voltage across Cload is maintained without significant power dissipation. No transistors are actively charging or discharging during this phase. During the adiabatic discharging phase, N1 is turned on to discharge Cload through the path provided by P1. Energy stored in Cload is efficiently transferred to the output. Any remaining charges in Cload are recovered and stored for reuse in the next charging cycle.2N-2N2P adiabatic logic can be applied in low-power digital circuits where energy efficiency is crucial. It may find use in applications such as portable devices, energy-constrained systems, and IoT devices [19]. The each Cload is associated with the output node of the adiabatic logic circuit, and its voltage variations reflect the operation of the circuit. The input signals control the transitions between different phases (charging, discharging, recovery) to achieve energy-efficient operation.

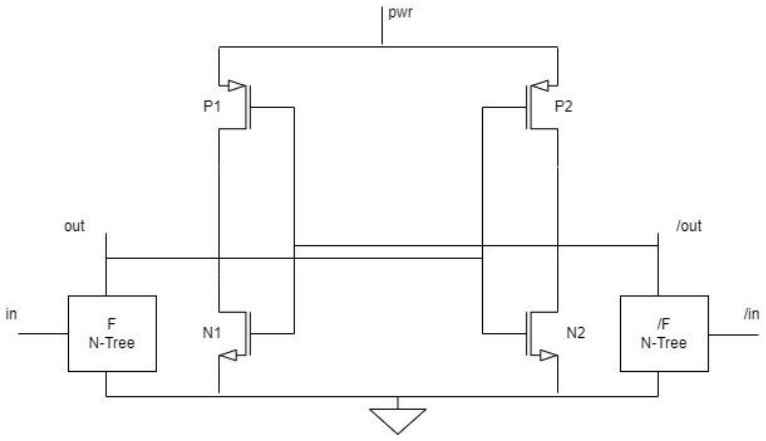

Figure 15. Schematic diagram of 2N-2N2P

5. LITERATURE SURVEY

Muthu *et al.* [20] suggested adiabatic CMOS-based electrostatic MEMS actuation circuit is discussed in the paper along with its lower power consumption as compared to earlier designs. The results indicate that by significantly reducing the clock frequency and optimizing power consumption in the circuit, a minimum power difference of 0.0186 mW is achieved between adiabatic and non-adiabatic designs. In comparison to earlier designs, the suggested adiabatic CMOS-based electrostatic MEMS actuation circuit in this study shows a significant decrease in power usage. The notable power savings are a result of optimization of the design parameters, capacitance, and clock frequency. Kumar and Tripathi [21] We saw a significant improvement in results when we compared the performance of PFAL and ECRL basic gates with CMOS gates. ECRL and PFAL logic gates are the most appropriate and practical in any circuitry due to industrial demands for low-power, fast-operating devices. Building an adder, complete adder, multiplexer, or flip-flop can all be done using these fundamental gates. Using the PFAL and ECRL gates, we have created a 2:1 mux by using NAND and NOR that operates extremely quickly and uses very little power. It is emphasized that the 2:1 MUX operates quickly and uses less power than conventional CMOS-based solutions it is shown in Table 1. Tanner tool simulation results are achieved with TSMC180nm technology.

Table 1. Comparison of CMOS, PFAL, ECRL

Parameter	CMOS		PFAL		ECRL	
	NOR	NAND	NOR	NAND	NOR	NAND
Power(nw)	170	162	105	70.7	50.9	26.2
Delay(ps)	19.5	26.4	12.7	2.90	82.7	49.4
PDP (aj)	3.34	4.72	1.34	0.25	4.21	1.29
Energy (fj)	27.3	28.3	16.8	11.3	8.1	4.19

Vaishiba and Durai [22] purpose of the energy efficient secure positive feedback adiabatic logic (EE-SPFAL) circuits that are presented in this paper is to improve security against DPA attacks by preventing information leakage and reducing non-uniform power consumption. The scientists want to reduce power dissipation and stop any weaknesses that could be used for power analysis by using adiabatic logic approaches. The suggested EE-SPFAL creates logical circuits such as buffers, OR-XNOR, and AND-NAND gates. The CMOS 180 nm cadence technology was used to analyze the different adiabatic logic circuits. Prior research has explored various approaches to designing energy-efficient and secure logic circuits. For instance. Monteiro *et al.* [23] based on the adiabatic switching idea, we have put forth a novel secure logic style. A thorough comparison of this logic's potential as a backup strategy to stop a power analysis attack at the cell level was conducted using a SPICE simulation. We conclude that our suggested CSSAL is a good option for secure hardware in low-power and low-frequency applications, like radio frequency identification (RFID) tags, wireless sensors, and contactless smart cards (13.56 MHz), based on these typical results. Kumar *et al.* [24] suggested approach makes use of an energy-efficient full adder to create a low power multiplier. In the entire adder design, a novel technique known as double pass transistor with asynchronous adiabatic logic (DPTAAL) has been used. For the different frequency ranges, the energy performance of the DPTAAL full adder is compared with that of the traditional CMOS full adder, and notable energy reductions of up to 84% are realized. The multiplier design makes use of this energy-efficient full adder cell. Maurya and Kumar [25] proposed inverter and 1-bit full adder have yielded simulation results that have been widely accepted and validated in the low power VLSI domain at low frequency. When the suggested circuit is compared to other conventional approaches, it becomes evident that the suggested logic has considerably lower power consumption than CMOS, PFAL, and 2PASCL based methods. For example, when the input frequency changes between 10 and 150 MHz, the proposed 1-bit full adder circuit and inverter circuit consume very little power—only 11% and 12% of the total power of a static CMOS-based logic circuit, respectively. Consequently, there is no doubt that the suggested adiabatic logic is a very promising and power-efficient technology, particularly in the low-power VLSI regime.

Prashanti *et al.* [2] reduce power dissipation in CMOS devices, they investigate the application of adiabatic approaches. This research examines how typical CMOS logic for inverter NAND and NOR circuits is compared to two adiabatic logic families: ECRL and PFAL. Adiabatic techniques can be a useful option for low-power applications within a specific frequency range, according to research that demonstrates this through simulations and analysis. PFAL outperforms ECRL in terms of power efficiency when compared to CMOS logic, particularly when it comes to high frequencies and load capacitances. Based on a broad variety of parameter modifications, the article shows that adiabatic logic families have potential uses in low-power.

Managoli and Ramesh [26] with a focus on low power consumption and energy efficiency, this work gives a thorough analysis on the design and implementation of a 4-bit arithmetic logic unit (ALU). These days, ALUs are getting smaller and more complex to accommodate the development of increasingly powerful but smaller computer systems. The 4-bit ALU architecture can perform three arithmetic and four logical operations. The three arithmetic operations are division, subtraction, and addition. Logical operations are AND, OR, XOR, and NOT. Circuits for power-gated adiabatic inverters that use ECRL methods have also been designed to verify the suggested methodology. The power is reduced from 54.028 mW to 23.93 mW compared to the current ALU.

Anitha *et al.* [27] in order to provide power-efficient gates for low-power electronic systems, this research investigates the usage of adiabatic logic. Adiabatic logic is emphasized as a potentially effective method to lower energy dissipation in contemporary mobile and high-speed digital gadgets. In terms of energy dissipation, propagation delay, and transistor count, the research examines several logic designs, such as CMOS logic, ECRL, PFAL, and 2N2N2P logic. Using the Cadence Virtuoso instrument and 90 nm technology, these gates were simulated. The study uses different adiabatic logic styles and CMOS logic to offer simulation findings for NOT, NAND, and NOR gates. According to the results, adiabatic logic has less energy dissipation than conventional CMOS logic shown in Table 2. The study comes to the conclusion that low-energy systems can be developed by combinational and sequential circuits using adiabatic logic.

Table 2. Comparison of power, no. of transistor used for NAND, NOR, NOT

Logic/Parameter	NOT		NOR		NAND	
	Transistor	Power(w)	Transistor	Power(w)	Transistor	Power(w)
CMOS	2	608	4	106	4	66.2
ECRL	4	62.7	6	40.4	6	39.8
PFAL	6	62.3	8	95.3	8	65
2N2N2P	6	80	8	82	8	43.8

Rao and Satyanarayana [28] in this work, the PFAL circuit is especially discussed as a low power combinational circuit design employing adiabatic logic. In terms of power dissipation and space, the PFAL circuit is compared to conventional CMOS circuits and ECRL. With its better power dissipation capabilities, the PFAL circuit is a viable choice for low-power design. Adiabatic logic reduces heat dissipation by recycling circuit energy through the use of AC voltage supply (power-clocks). Along with presenting simulation results at a TSPICE 250 nm technology node, the paper also investigates parameter modifications affecting power usage. Overall, low-power application potential and energy efficiency are demonstrated by the PFAL combinational circuit architecture.

Chugh *et al.* [29] use of adiabatic logic circuits in energy-efficient logic circuit design is covered in this work. It examines the power dissipation properties of many adiabatic logic families, including ECRL, 2N-2N2P, and PFAL. HSPICE at 65 nm technology was used for the simulations, which had a supply voltage of 1V and a frequency of 100 MHz. The research underscores the significance of taking into account both static and dynamic power when designing low-power VLSI circuits and emphasizes the advantages of adiabatic logic in terms of power conservation. Using a variety of logic gates to test the viability of various adiabatic logic families over traditional CMOS circuits; initially, the adiabatic concept of various adiabatic logic families, as shown in Figure 16, is used.

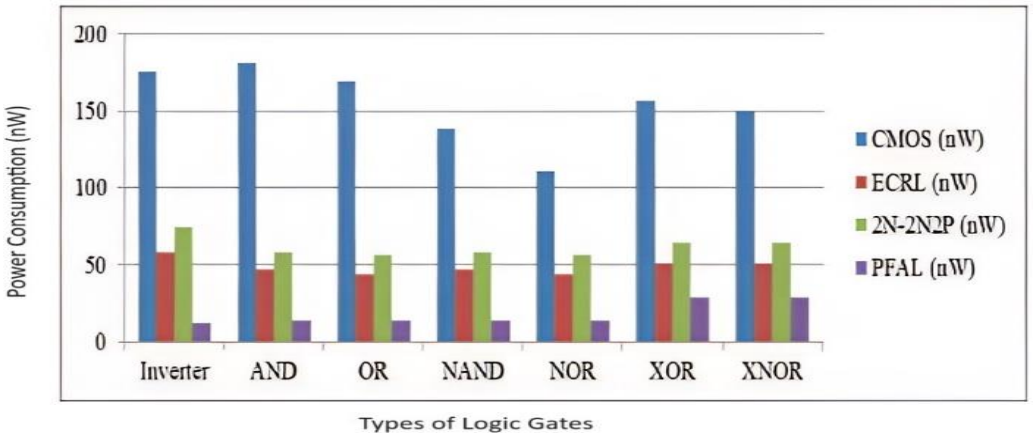

Figure 16. Comparison of all adiabatic circuit design

Li *et al.* [30] the energy efficiency of CCAL is compared in the power analysis of the paper to that of standard static CMOS and quasi-static energy recovery logic (QSERL). According to simulation data, at 200 MHz, CCAL saves almost 40% of the energy used by static CMOS. Furthermore, below 100 MHz, CCAL always dissipates less than QSERL. Compared with CMOS eight-inverter chain, the dissipation with the frequency increases the energy saved becomes less is shown in Figure 17. The CCAL eight-inverter chain saves about 40% energy at 200 MHz and 15% energy at 500 MHz compared to the CMOS implementation. The study shows that CCAL has greater energy efficiency under a range of operational conditions.

These findings demonstrate that because ECRL-based designs offer significant power savings over CMOS logic, they can be employed in low power applications such as wireless sensor networks and medical devices [31]. The Wallace Dadda and Vedic Dadda multiplier were implemented using ECRL adiabatic design, which produced a 77% lower power consumption than conventional CMOS technology, as shown in Table 3.

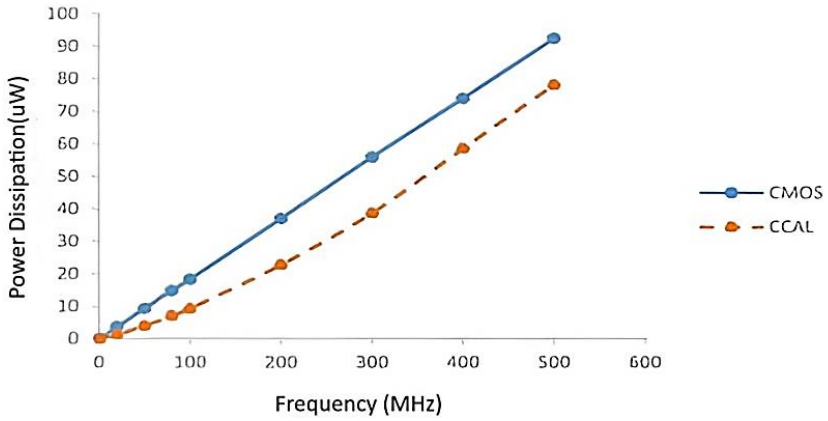

Figure 17. Comparison of power dissipation with CCAL vs CMOS

Table 3. Power dissipation of CMOS and ECRL design

Parameters	Wallace-Dadda	Vedic-Dadda	Vedic
CMOS	174.36 µW	169.35 µW	140.70 µW
ECRL	39.606 µW	37.417 µW	34.208 µW

6. RESULTS AND DISCUSSION

After reading the papers, we created a comparison table by utilizing a number of different standards. Commonly utilized for arithmetic operations, adder circuits can be found in a variety of medical devices that need to do mathematical calculations. Adder circuits are used in the digital signal processing step of medical imaging systems including computed tomography (CT) and magnetic resonance imaging (MRI) scanners. It can be applied to problems including picture enhancement, filtering, and reconstruction. The dependability, accuracy, and power efficiency of the adder circuit are critical to guaranteeing the medical equipment overall efficacy. A comparison of various adder circuits with adiabatic logic is presented in Table 4. Here, we are comparing several low power methods that are applied to full adder circuits. The full adder in [32] uses the transistor reduction technique, consuming 6.889 uW of power at 1 volt. Next, [33] uses pass transistor logic, which uses 4.47 uW of power at 1.2 volts. The transmission gate in [34] uses 6.972 uW of power at 1.2 volts. In the end, [35] uses the adiabatic logic technique; in contrast to earlier, this power is 0.421 nw. Therefore, the adiabatic logic uses less power than earlier methods.

Table 4. Comparison of different low power techniques

Ref	Techniques	Methodology	Transistor count	Delay	power consumption (µw)	Voltage supply
[32]	Cadence Virtuoso 90 nm Technology	Transistor reduction	13	20 ns	6.889	1 V
[33]	65 nm CMOS Technology Cadence Virtuoso	Pass transistor logic	10	50.8 ns	4.47	1.2 V
[34]	0.18 um TSMC CMOS Technology	PTL, TG	14	242.62 ps	6.972	1.2 V
[35]	90 nm CMOS Technology Microwind	Adiabatic logic	18	0.421 ns	0.282	1.2 V

The research demonstrates the feasibility of implementing adiabatic logic circuits in medical applications, showcasing the potential for significant reductions in power consumption. Various digital components, including signal processing units, control logic, and communication modules, benefit from the adoption of adiabatic techniques. Experimental results and simulations illustrate the energy efficiency gains achieved in comparison to traditional static CMOS logic. Medical imaging technology, wearable health monitoring systems, and implantable medical devices are among the realistic uses for the suggested low-power adiabatic logic circuits. Improved overall sustainability in healthcare technology, longer battery life, and a decreased need for external power sources are all benefits of the increased energy efficiency.

7. CONCLUSION AND FUTURE SCOPE

In conclusion, applying low-power adiabatic in the medical field offers promising energy-efficient and reliable electronic system advancements. The unique characteristics of adiabatic logic, which focuses on minimizing energy dissipation during logic transitions, align well with medical devices' stringent power constraints and operational requirements. By carefully managing energy flows and incorporating adiabatic charging and discharging mechanisms, this logic design is particularly suitable for implantable medical devices, portable diagnostic tools, and other healthcare applications where power efficiency, extended battery life, and reduced heat dissipation are critical factors. The ability of low-power adiabatic logic to strike a balance between energy efficiency and performance makes it an attractive choice for medical electronics, where reliability and low-power operation are paramount. As advancements in semiconductor technology continue, further research and development in low-power adiabatic logic have the potential to contribute significantly to the evolution of medical devices, enabling innovative solutions with enhanced efficiency and reduced environmental impact. In order to improve patient care and advance the field of medical technology, researchers and developers can keep pushing the limits of what is feasible using adiabatic logic in medical applications by investigating these potential scopes.

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CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

Data availability is not applicable to this paper as no new data were created or analyzed in this study.

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BIOGRAPHIES OF AUTHORS

Prabhu R. received Bachelor of engineering in electronics and communication engineering from Anna University, Chennai. He also received Master of engineering in VLSI Design from Anna University, Chennai. He is completed professional development course in VLSI Design and Verification in Bangalore. He is currently pursuing Doctor of philosophy in Vellore Institute of Technology, Vellore. His research interest in digital design, VLSI design, FPGA based system design, low power CMOS design, and digital image processing. He can be contacted at email: prabhu.r2020@vitstudent.ac.in.

Sivakumar Rajagopal received the BE in electronics and communication engineering from Bharathiar University, and the ME and Ph.D. degree in information and communication engineering from the College of Engineering Guindy, Anna University, Chennai, India. His research interests include bio signal processing, medical image processing, wireless body sensor networks, and VLSI. He has published over 50 journal and 50 conference papers over the last several years. He has taught a wide variety of electronics courses including digital image processing, multimedia compression techniques, VLSI design, medical electronics, and electronic circuits. He is a life member of the Indian Society of Technical Education and a senior member of IEEE. He has been invited to deliver a Keynote Speech and Chair at various international conferences. He can be contacted at email: rsivakumar@vit.ac.in.