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Assessment of detection methods for back-end process defects in equipment and devices in semiconductor manufacturing

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ABSTRACT

Defect detection plays a pivotal part in the manufacturing process of semiconductors. Defects can be rooted in the product on its own, as well as the tools used to process and make the product, particularly the equipment and machinery used. Defect detection is crucial in semiconductor manufacturing, where even minor flaws can compromise product performance. Defect detection in the backend process of semiconductor manufacturing, specifically in die attach and die bonding, is critical for ensuring product quality and reliability. Die attach involves securing semiconductor chips onto substrates, while die bonding involves connecting wires to the chip. Detecting defects during these processes is vital to prevent issues such as misalignment, inadequate bonding, or contamination, which can lead to malfunctioning chips or devices. Various techniques such as visual inspection, automated optical inspection (AOI), and X-ray imaging are utilized to identify defects like cracks, voids, or irregularities in bond formation. By employing rigorous defect detection measures, manufacturers can uphold stringent quality standards and produce reliable semiconductor devices for various applications.

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1. INTRODUCTION

Semiconductor manufacturing involves the intricate process of fabricating electronic components such as integrated circuits on semiconductor materials, employing precise techniques to etch, deposit, and pattern materials at the nanoscale level. However, despite the many advantages of integrated circuits, defects can occur during the manufacturing process, and these defects can have various impacts on the performance and reliability of the semiconductor packages. Process variations can result in performance variations, affecting factors such as speed, power consumption, and reliability, leading to inconsistencies in transistor sizes, dopant concentrations, and other parameters [1], [2]. Particle contamination meanwhile, may cause short circuits, increased leakage current, or other electrical anomalies, potentially leading to the package failure. Another known issue is defective interconnections, particularly in the metal interconnect layers, such as open circuits or shorts, can disrupt the flow of signals between components causing reduced functionality

or complete failure of the integrated circuit. Stress-induced defects on the other hand may lead to the development of cracks, voids, or other structural issues, impacting the overall reliability and lifespan of the IC [3]. Techniques such as design for manufacturing (DFM), thorough testing at various stages, and implementing redundancy in critical components are employed to improve yield and ensure the reliability of integrated circuits.

When it comes to testing and examining integrated circuits (ICs), both destructive and non-destructive inspection methods are employed. The choice between these methods depends on factors such as the stage of production, the desired level of detail, and the impact on the integrity of the IC. This survey focuses on the non-destructive testing (NDT) method that is used to examine the reliability as well as to analyze any failure mechanisms within the device [4]. Similarly, examining equipment defects is a crucial aspect of ensuring the reliability, safety, and performance of machinery and devices [5]. Die attachment and die bonding are critical steps in manufacturing the ICs as they define the connection to the package and provide electrical interconnection for power and signal transmission quality, alongside thermal management via efficient heat dissipation from proper bonding applications [6]–[8]. The objective of this paper is to provide a survey and/or review of research papers that have addressed the faults and defects of the die attachment and die bonding detection methods used, for both devices and equipment.

2. OVERVIEW OF SEMICONDUCTOR MANUFACTURING PROCESS

2.1. Wafer fabrication steps in the front-end manufacturing process

Semiconductor wafers developed from silicon are typically comprise front-end and back-end manufacturing processes. The front-end process begins with the production of silicon wafers. Wafer fabrication involves a sequence of steps: starting with a polished wafer, layers are deposited using techniques like chemical or physical vapor deposition (CVD/PVD), followed by photolithography to pattern the layers, etching to remove unwanted material, ion implantation to alter conductivity, diffusion to homogenize doping, chemical mechanical polishing to planarize surfaces, and finally testing to ensure functionality [9], [10]. These processes are repeated iteratively to build complex integrated circuits on silicon wafers. Figure 1 depicts wafer fabrication steps in the front-end manufacturing process.

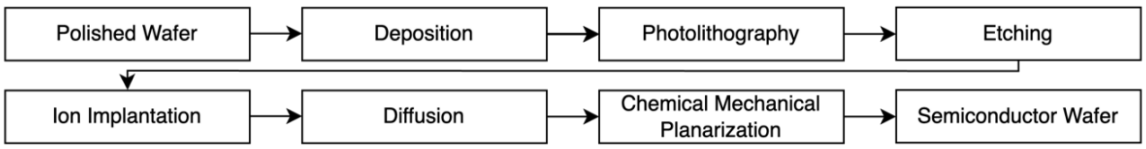

Figure 1. Wafer fabrication steps in front-end manufacturing process

2.2. Back-end manufacturing process for semiconductor production

In the back-end semiconductor manufacturing process, fabricated wafers undergo various critical steps. Initially, electrical testing identifies faulty dies, which are then marked to prevent wasted packaging. The wafer is mounted for mechanical support, then precisely diced into individual die units. Good dies are bonded to substrates, and microscopic wires connect them to electrical terminals. Plastic molding encases the components in epoxy resin for protection, followed by electrochemical plating for enhanced durability. Trim and form steps shape the leads, and final testing ensures functionality. Laser marking adds identification codes, and units are packed according to specifications for shipment. This comprehensive process ensures the production of reliable semiconductor devices for integration into electronic products [11]. Figure 2 illustrates the back-end manufacturing process for semiconductor production. Die bonding is a crucial step in establishing a reliable electrical connection between the semiconductor die and substrate. It begins with die preparation, where the die is tested, sorted, and equipped with bond pads, before the substrate is prepared, and adhesive may be dispensed onto it. The die pickup process utilizes specialized tools like Vespel collets to handle the semiconductor die, ensuring damage-free manipulation. Precision alignment systems align the die's bond pads with the substrate's contact points before placement, before the die is gently lowered onto the substrate. Once adhesive bonding is employed, curing processes via heat or UV light may follow to solidify the adhesive. Overall, die bonding ensures both electrical and mechanical integrity in semiconductor devices [12], [13]. The accuracy of this process are essential for the reliable and consistent performance of electronic devices.

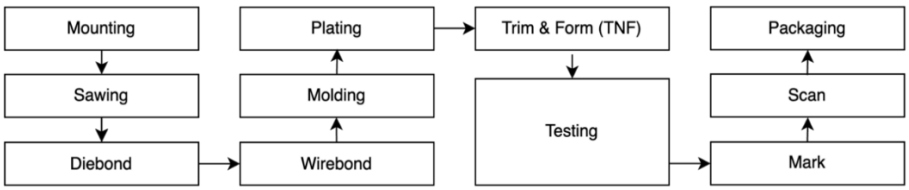

Figure 2. Back-end manufacturing process for semiconductor production

3. OVERVIEW OF DETECTION MODALITIES IN SEMICONDUCTOR MANUFACTURING PROCESS

In semiconductor manufacturing, various methods or techniques are used for sensing and monitoring different aspects of the manufacturing process, which plays a crucial role in quality control, process optimization, and ensuring the reliability of semiconductor devices. These steps in return introduces production efficiency as well as production costs. Sensor modalities for metrology in semiconductor manufacturing is highly interdependent.

Optical sensing in semiconductor manufacturing encompasses manual optical inspection and automated optical inspection (AOI). While manual inspection relies on human visual assessment using basic microscopes, AOI employs high-resolution imaging systems, advanced image processing software, and precision mechanical platforms for rapid, accurate defect detection. Manual inspection is limited by low optical resolution, slow speeds, subjective biases, and human fatigue, making it less effective than AOI [14]. AOI systems integrate specialized optics and lighting techniques to capture microscopic details and utilize data analytics for process improvement, thus minimizing yield loss and optimizing manufacturing efficiency.

X-ray metrology delivers critical dimensional, structural and compositional information during both front-end lithography and back-end assembly stages that remains inaccessible through conventional surface-limited optical and electron microscopy for process monitoring, defect detection, quality control, specifically probing tiny transistor gate geometries, measuring metal fill densities, inspecting die attachments, characterizing diffusion depths, verifying IC interconnects, auditing flip chip bonds, and examining packaged chips [15], [16]. Acoustical techniques are integral to semiconductor fabrication, offering non-invasive subsurface inspection critical for quality control and defect reduction. Scanning acoustic microscopy (SAM) employs ultrasonic waves to map buried interfaces, voids, and defects with micron-level resolution, rivaling electron microscopy allowing precise imaging of material structures and defects in chips/packages, film thickness measurement, delamination sensing, and transistor element imaging [17]. Surface acoustic wave (SAW) systems use high-frequency Rayleigh waves to monitor device surfaces, providing in-situ metrology for process and reliability monitoring [18]. Both techniques complement traditional optical and electron microscopy, offering valuable insights into semiconductor manufacturing processes.

Infrared thermography is widely used in semiconductor fabrication facilities for visualizing and quantifying thermal phenomena to optimize energy usage, prevent chip damage, and enhance processing efficiency with real-time thermal imaging and analysis. This enables precise temperature measurement across wafers, detection of hot spots, characterization of heating and cooling processes, and identification of defects such as voids or delamination, ensuring thermal conduction and device reliability.

4. DETECTION METHODS FOR DIE BONDING & DIE ATTACH ON PACKAGES AND EQUIPMENT

Die bonding and die attach processes within semiconductor manufacturing are pivotal stages requiring meticulous quality control to uphold the reliability and performance of electronic devices. These processes are susceptible to various defects that can manifest in both the semiconductor packages/products and the equipment utilized in the manufacturing pipeline. This section delves into the common defects associated with semiconductor packages/products and equipment, shedding light on advanced detection methodologies.

4.1. Die attachment and die bonding package defects

Among the common defects are incomplete solder joints and solder bridging. Detection methods for solder joint defects leverage high-resolution imaging coupled with image processing techniques, enabling the identification of incomplete joints. Deep learning methods, such as convolutional neural networks (CNNs), prove instrumental in classifying diverse solder defects. Detection involves the use of machine vision systems equipped with alignment algorithms and pattern recognition to detect and quantify skew and offset errors.

The presence of chips or cracks in the die represents another prevalent defect. Detection methods encompass imaging paired with CNNs or support vector machines (SVMs) for the classification of distinct chip and crack patterns [19]–[22]. Defects like air pockets or incomplete epoxy filling, inaccurate placement of the die on the substrate, variation in the thickness of the bond line and die fly-off or die detachment during the bonding process constitutes common defects. Optical inspection, image analysis, or spectroscopy are used to identify contaminants for foreign particles or dusts within the packages. Finally, overall package defects affecting reliability can be mitigated via accelerated testing, thermal cycling, and various NDT methods.

4.2. Die attachment and die bonding equipment component defects

Die bonding tools are critical components in semiconductor manufacturing, but they can also be sources of defects if not properly maintained. Common issues include improperly calibrated bond heads, worn-out force sensors, contaminated microscopes, tilted workholders, clogged dispensers, and misaligned bond arm motions, amage or misalignment in pick-up tools, wear and chipping in bond tools/heads, misalignment and wear in workholders, and mechanical issues in bond arms. Calibration issues and lens damage in scopes and sensors are also prevalent defects. These problems can trigger equipment alarms and contribute to higher unscheduled downtime (UDT) and mean time between assists (MTBA). Environmental factors like temperature, humidity, and vibration, coupled with preventive maintenance lapses, can also lead to equipment issues over time, such as stage backlash and inconsistent vision and heating.

Detection of defects in die bonding tools involves various methods, including machine vision, alignment algorithms, image processing, and wear monitoring using sensors. Detection methods range from regular calibration checks and visual inspections to advanced techniques like SVM, CNN, artificial neural networks (ANN), robust principal component analysis (RPCA), residual networks (ResNet), radial basis function (RBF), fuzzy c-means (FCM), generalized regression neural network (GRNN), self-organizing maps (SOM), linear discriminant analysis (LDA), learning vector quantization (LVQ), and you only look once (YOLO). Each method offers specific advantages, catering to the complexity and requirements of the detection task, ensuring the precision necessary for a robust semiconductor manufacturing process and mitigating bonded product defects, ensuring quality, yield, and long-term reliability.

4.3. Assessment of papers based on backend processes

Table 1 (in appendix) presents an extensive overview of various detection methods utilized in the back-end manufacturing processes along with their performance metrics as reported in different articles. Delving into each entry, AOI has been utilized widely throughout several processes to continuously monitor and minimize package defects throughout the backend process [23]–[28]. Several research conducted recently focuses on map detection in Pre-assembly process and testing, reporting accuracy and precision for MLP and DNN, alongside broad learning system, achieving high DSPR comparison. The wafer mapping defects performance metrics are also compared against various models and feature extraction techniques. Haddad *et al*. [28] proposed method achieved high precision and recall values in AOI.

In [29]–[31], acoustic sensing inspection are utilized, particularly in SAM, with 1D-CNN utilized for SAM image inspection, providing insights into porosity variation during bonding processes. SAM has also proven to effectively precise in defects detection, achieving an accuracy of 97.14% [23]. Comparatively, SAM is also proven to be effective compared to another radiology inspection in X-Ray and SEM for thermal joint detection [31], with a study of X/gamma-ray spectroscopy carried out by [32] for electrical characterization measurement, reporting detailed performance metrics for the spectrometer. Thermal-based inspection has also been carried out by [31], [33], whereby compared to [31], a study emphasis on the on-line thermal resistance during die-attach, highlighting the accuracy of SiC-TEG for evaluating thermal characteristics. CNN have also been used to predict the electro-thermal conductivity (ETC) of sintered Ag. Their model achieved high accuracy with an R2 value of 0.987 and a relative mean absolute error (RMAE) of 3.12% [1]. Solder joint defect detection has been extensively studied in recent years in [21], [25], [26], [34]–[38]. Various methods and modellings have been tested, with one focuses on chip scale packages (CSP) reliability, achieving validation metrics including RMSECV, MAECV, and R2 for ball/substrate and ball/test board solder joints. Solder joint defect detection has also been tested via Sequential NN, recurrent neural network (RNN), and long short-term memory (LSTM) for solder joint detection, reporting low error norms for different data pairs. ANN and RNN demonstrated stable optimization for the solder joint defect detection, with YOLOv4 for detecting solder defects in SMT circuit elements with high accuracy and speed. Alternatively, ConvNeXt-YOLOX for solder joint inspection, achieving the highest mAP among compared methods. Tai *et al* [38]. employed YOLOv2 & ResNet-50 for solder joint defect recognition, reporting high accuracy for different defect types. That said, YOLO are also utilized for solder defect detection in AOI, achieving fast processing time per PCB image. ViBe and +Elasticnet have also been used for solder joint inspection, highlighting significant improvements in error rates and accuracy. Solder joint inspection for AOI using various methods and reported different performance metrics for each method.

Wire bonding process can be further improved in manufacturing, by reducing its ball bonding and wire bonding defects. SVM, logistic regression (LR), and CNN models are proven by [22] to be effective for ball bonding inspection, achieving an 85% automated detection rate. DenseNet121, VGG19, ResNet50, MobileNetv2, EfficientNetB0 V1 & V2 employed for wire bond defect detection, achieving high accuracy across different models. A utilitarian method by [2] showcases CNN combined with computer-aided manufacturing (CAM), YOLOv3, and YOLOv3-dense for inspecting various processes like die attach, wire bond, molding, curing, punching, sorting, taping, and packing. The performance varied for different defect types, with mAP ranging from 61.59% to 95.28%. Wafer level package (WLP) reliability and solder ball reliability have also been tested via finite element method (FEM) and ANN.

Die defects detection has been analyzed in several works [2], [3], [5], [9], [39]. Generative adversarial network (GAN), YOLOv3, and other models are employed for die defect detection, achieving significant improvements in accuracy with model combinations. Die defect detection using auto ML, meanwhile has achieved a recall rate of 42.6% with 90% accuracy. ResNet 101 & DLADC SEM, CNN and GAN for defect detection has proven to results in accuracy for different subsets and training data sizes. reporting high accuracy for both methods. Meanwhile, die defect classification the accuracy between handcrafted features and proposed RCNN model have also been carried out with comparative studies being made. By comparing the RNET, VoxNET, and PointNet for scanning and inspecting die attach glue bonding, reporting RNET outperforming others with a classification accuracy of 91.82%. Die attach glue volume regression and dispensing defect identification via R^2esNet, have also showcases desirable performance metrics for various models based on scanning time and inference time study [30]. Surface treatment and final test processes meanwhile uses several methods in optimizing the process defects, with surface treatment process employing various CNN methods for performance metrics comparative approach [40], [41]. CNN and DLADC methods for surface treatment reporting high accuracy. Gaussian mixture models, one hot encoder, label encoder, F1-macro test are all explored by [42] yield classification for final test, employing various models and preprocessing techniques, reporting F1-macro scores.

5. CONCLUSION

Defect detection is indispensable in semiconductor manufacturing to ensure product quality and reliability. From the review, it's evident that defects can arise from various sources, including the product itself and the equipment used in manufacturing processes. Detecting defects during backend processes like die attach and die bonding is critical to prevent issues which can lead to malfunctioning chips or devices. Various techniques such as visual inspection, AOI, and X-ray imaging are employed to identify defects, with advancements in methods like CNNs proving to be highly effective as highlighted via plethora of studies focusing on different aspects of defect detection, ranging from solder joint defects to wafer mapping defects, and from wire bonding to die defects. Overall, the research showcased in the review emphasizes the importance of rigorous defect detection measures in semiconductor manufacturing. By employing these measures, manufacturers can uphold stringent quality standards and produce reliable semiconductor devices for a wide range of applications. Moreover, the continual advancement of detection methods and technologies underscores the industry's commitment to enhancing product quality and reliability in the ever-evolving semiconductor landscape. With most studies carried out focuses on defect detection on device or package, future work will involve further into developing a defect detection system on the semiconductor equipment, particularly for the die bond process.

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors state no conflict of interest.

DATA AVAILABILITY

Data availability does not apply to this paper as no new data were created or analyzed in this study.

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APPENDIX

Table 1. The detection methods used and performance in the back-end manufacturing processes

Article #	Authors	Type of inspection	Detection methods used	Performance
[19]	Du *et al.*	CNN performed to predict the ETC of sintered Ag.	CNN	The RMAE and R^2 were 3.12% and 0.987, re- spectively, and the RPE was within 10% for nearly 91% of model predicted results with relative error: 5%
[20]	Chen and Tsai	Image capturing for die attach, wire bond, molding, curing, punching, sorting, taping and packing	CNN + CAM, YOLOv3, YOLOv3-dense	Model class: CNN+CAM / YOLOv3 / YOLOv3-dense Defect-free: 100.00% / 90.91% / 100.00% Missing component: 3.45% / 100.00% / 100.00% Incorrect placement: 66.09% / 100.00% / 90.91% Inverse polarity: 100.00% / 72.73% / 100.00% Missing wire: 100.00% / 81.82% / 100.00% Defective surface: 0.00% / 36.36% / 80.82% mAP: 61.59% / 80.30% / 95.28%
[21]	Hamdani *et al.*	CSP reliability for solder joint, crack on package (die attach/DA)	MCS	The metamodel validation for a Kriging metamodels built based on 180 samples are $RMSE_{CV}$ = 3.3, MAE_{CV} = 2.42 and R^2 = 0.9 for ball/substrate solder joint, and $RMSE_{CV}$ = 1.79, MAE_{CV} = 1.30 and R^2 = 0.89 for ball/test board solder joint.
[22]	Chan *et al.*	Ball bonding inspection	SVM, LR, CNN-FCN-4000, CNN-Hough-4000	Experimental results showed that 15 samples among all the 100 test samples were below the predefined threshold. Hence 85% of detections are automatically conducted by the proposed framework due to 15 uncertain samples.
[30]	Dimitriou *et al.*	Scanning and inspection of DA glue bonding	RNET, VoxNET, PointNet	RNet outperforms VoxNet and PointNet with an average classification accuracy of 91.82% compared to 86.42% and 58.33%, respectively.
[29]	Brand *et al.*	SAM image inspection for bonding porosity.	1D-CNN	Porosity variation was obtained through adjusting the sinter pressure between 5 MPa and 30 MPa. Porosity variation obtained through adjusting the sinter time between 5 s and 180 s. Noticeable contrast patterns appear between the acoustic micrograph and the porosity map.
[23]	Watanabe *et al.*	SAM for defects (fused, damaged, lift, no change) at AOI	CNN	Accuracy: 97.14%
[34]	Yuan and Lee	Solder joint detection / reliability	Sequen-tial NN, RNN, LSTM	Avg error norms (27 data pairs) RNN: $1.432x10^{-4}$ LSTM: $1.357x10^{-4}$ Avg error norms (54 data pairs) RNN: $1.213x10^{-4}$ LSTM: $1.190x10^{-4}$
[35]	Yuan *et al.*	Solder joint reliability	ANN, RNN	All the AI model learning results satisfy the accuracy requirement of 0.18% when the PCA gene is applied as the initial parameter.
[43]	Chou *et al.*	WLP reliability, solder ball reliability.	FEM, ANN	-
[24]	Dai *et al.*	Solder defect detection in AOI	YOLO	PCB layout porting of <0.34 s per PCB image (110 solder joints)
[25]	Caliskan and Gurkan	Solder joint defect detection in AOI	YOLOv4	Detection of solder defects of SMT circuit elements in approximately 5K (4056x3040) images resolution can be achieved with 97% accuracy in around 4 seconds.
[36]	Chen *et al.*	Solder joint inspection	ViBe, +Elasticnet	Methods / Training Samples / Error Rate (%) / Omission Rate (%) / Accuracy (%) ViBe-Based: 400(Q) / 1.66 / 69.93% / 93.33 Elastic net: 400(Q)+40(U) / 0.00 / 1.50% / 99.91
[37]	Liao *et al.*	Solder joint inspection	ConvNeXt-YOLOX	ConvNeXt-YOLOX had the highest mAP of 97.21%, which was 0.82% and 3.02% higher than that of YOLOX and YOLOX-s
[38]	Tai *et al.*	Solder joint defect recognition	YOLOv2 & ResNet-50	Defect / Accuracy (%) Good solder: 88.56 Bridge solder: 90.47 Missing solder: 87.86

Table 1. The detection methods used and performance in the back-end manufacturing processes (Continued)

Article #	Authors	Type of inspection	Detection methods used	Performance
[44]	Evangelidis *et al.*	Die attach glue volume regression/dispensing defect identification	R^2esNet	Model: Scanning time / Inference time / Total time ec-R^2esNet10: 55.42 / 55.59 ec-R^2esNet18: 63.72 / 63.89 ec-R^2esNet34: 80.84 / 81.11 ec-DenseNet: 60.07 / 60.24
[32]	Bodie *et al.*	Electrical characterization measurement	Radio-logy (X/γ-ray spectroscopy)	The detector and preamplifier were operated uncooled at temperatures between 20 ◦C and 100 ◦C. The energy resolution (full width at half maximum, FWHM) of the spectrometer was found to be 1.66 keV ± 0.15 keV at 5.9 keV and 22.16 keV, and 1.83 keV ± 0.15 keV at 59.5 keV when operated at 20 ◦C. At a temperature of 100 ◦C, the FWHM were 2.69 ± 0.25 keV, 2.65 keV± 0.25 keV, and 3.30 keV ± 0.30 keV, at the same energies.
[27]	Chen *et al.*	Die defect for AOI equipment	GAN, YOLOv3, Faster RCNN, shot multibox detector (SSD)	Model: Testing AP (%) / Testing coordinate prediction error YOLOv3: 81.39 / 1.6456×10^{-3} GAN + YOLOv3 (1.5 fold increase): 88.12 / 2.9662×10^{-4} GAN + YOLOv3 (2 fold increase): 88.72 / $X1.5851 \times 10^{-4}$ CycleGAN + YOLOv3 (1.5 fold increase): 33.14 / 6.488×10^{-1}
[45]	Fazil *et al.*	Die defect detection	Auto ML, control group	Recall rate of maximum 42.6% means 42.6% of bad die able to be predicted correctly with 90% accuracy.
[31]	Rosman *et al.*	Thermal joint detection	SAM	SAM achieved 25.8% positive-classification (better) than X-Ray. SAM achieved 90.3% is success rate in comparison to scanning-electron-microscopy (SEM).
[46]	Phua and Theng	Defect detection for surface treatment / plating process	ResNet 101 & DLADC SEM, CNN	Model / Dataset / Top-1 Accuracy (%) / Top-3 Accuracy (%) ResNet101 / Validation: 90.7 / 99.0 ResNet101 / testing: 91.5 / 98.5 DLADC / Validation: 89.7 / 96.1 DLADC / testing: 91.1 / 96.2
[47]	Ayuni *et al.*	Wire bond defect. detection	DenseNet121, VGG19, ResNet50, MobileNetv2, EfficientNetB0 v1 & v2	Model: Accuracy (%) DenseNet121: 98.0 VGG19: 97.0 ResNet50: 98.0 MobileNet v2: 96.0 EfficientNetB0 V1: 96.0 EfficientNetB0 V2: 98.0
[28]	Haddad *et al.*	Defect detection for AOI	RCNN, background subtraction	Haddad *et al*.proposed method was able to achieve a 98.2% precision and a 99.44% recall values.
[42]	Jiang *et al.*	Yield classification for final test	Gaussian mixture models, one hot encoder, label encoder, F1-macro test	F1-macro scores Input Pre-processing: 7-models average / Top 3 average No cat. input: 0.700 / 0.761 Label enc.: 0.710 / 0.788 One hot enc.: 0.736 / 0.788
[48]	You *et al.*	Die defect classification	Region-based CNN (RCNN)	Detection: Handcrafted features / Proposed (RCNN) Avg accuracy: 94.0 % / 88.5 %
[40]	Wen *et al.*	Defect Detection for surface treatment	CNN	Method: Wen et al. / FCN / DeepLabv3 Flops: 4.041×10^{10} / 1.419×10^{9} / 2.089×10^{9} Rate: 2.4fps / 5fps / 4fps
[41]	Do *et al.*	Multiple Wafer Bin Classification	CNN – HiSTA Network	-
[49]	Phua *et al.*	Defect Detection for surface treatment	CNN - DLADC	CNN-based Model: Accuracy (%) DLADC: 93.69 SSD with VGG16: 94.17 SSD with ResNet50: 91.52
[39]	Nam *et al.*	Die Defect Detection	Generative Adversarial Network (GAN)	Subset # / SEM/CAD # / Training Data / Accuracy [%] (random) / Accuracy [%] (cluster) 1 / 1344 / 7 / 85.83 / 97.58 2 / 5910 / 14 / 89.06 / 96.54

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