TELKOMNIKA Indonesian Journal of Electrical Engineering
Vol. 12, No. 9, September 2014, pp. 6667 ~ 6672
DOI: 10.11591/telkomnika.v12i9.4727

Design of a Current Starved Ring Oscillator Based VCO for Phase-Locked Loop

Khairun Nisa' Minhad, Zainab Kazemi, Mamun Bin IbneReaz, Jubayer Jalil*, Noorfazila Kamal
Department of Electrical, Electronic and Systems Engineering, Universiti Kebangsaan Malaysia, 43600 UKM Bangi, Selangor, Malaysia
*Corresponding author, email: jubayer.jalil@gmail.com

Abstract

A design of the proposed VCO was developed for PLL in radio frequency identification (RFID) application. By using current starved ring oscillator, the designed circuit is simulated using 0.18-µm CMOS process in Mentor Graphics environment. The results show that the voltage drawn is around 5V supplied at VDD, and the product of this current and voltage has approximate 105.3mW power consumption while the VCO generates 212MHz at 1.4V.

***Keywords**: low power, current starved VCO*

1. Introduction

In modern world, modules are being utilized in smart home systems, advanced image processing implementations, and numerous networks [1-8]. Due to advent, of CMOS technology, semiconductor devices pervade in every discipline of engineering, and to activate these devices, oscillators become core components [9-15]. A voltage controlled oscillator is a module in which the oscillation frequency is controlled by voltage input. Voltage controlled oscillator (VCO) forms a key element in the design of high frequency component using phased locked loops (PLLs). In very large scale integration (VLSI) technology, VCOs developed in CMOS process are utilized in a number of applications as the sources of signal generation and as data or clock recovery systems as well as RFID applications [16-21]. In this place, we recommend that a wide tuning range is comprehended by digital and incessant (analog) tuning circuits to reduce the VCO gain. The digital tuning scheme distributes a wideband tuning range into slighter bands. The continuous tuning control is a mechanism technique for the PLL. A PLL adjustment circuit is used to apportion the accurate sub band for an assumed channel frequency so that the PLL can lock within tuning voltage range. PLL adjustment techniques are defined and a new auto-calibration circuit is offered.

Voltage controlled oscillators play an important role in modern digital systems, providing signals required for timing in digital circuits and frequency translation in radio frequency RF Circuits. Their output frequency is a function of a control input usually a voltage. An ideal voltage-controlled voltage oscillator is a circuit whose output frequency is a linear function of its control voltage. Most application required that oscillator be tunable, i.e. their output frequency be a function of a control input, usually a voltage. There are two different types of voltage controlled oscillators used in PLL, Current starved VCO and Source coupled VCO [22-24].

In recent years LC tank oscillators have shown good phase-noise performance with low power consumption. However, there are some disadvantages. First, the tuning range of an LC-oscillator approximately around 10%-20%, and this is relatively low when compared to ring oscillators which accommodates >50%. So the output frequency may fall out of the desired range in the presence of process variation. Second, the phase-noise performance of the oscillators highly depends on the quality factor of on-chip spiral inductors. For most digital CMOS processes, it is difficult to obtain a quality factor of the inductor larger than three. Therefore, some extra processing steps may be required. And finally, on-chip spiral inductors occupy a lot of chip area, typically large which is undesirable for cost and yield consideration [25].

Received November 7, 2013; Revised May 15, 2014; Accepted June 10, 2014

The VCO gain suggestively varies over the wide tuning range, this, in turn, damages the PLL performance. One elucidation is to split the tuning range into a discrete smaller band it is used as a local oscillator (LO) to up-convert and down-convert the incoming RF signals. It is the purposeful block in modern RF communication systems. Current market has advanced in such way that everything is available in compact and affordable prices. In order to realize this, fully integrated circuits are mandatory. Thus a lot of research has been done in the field of wireless communications. Designing a frequency synthesizer commissioning a VCO is a major experiment.

A PLL is fundamentally a feedback loop that locks the on-chip clock phase to that of an input clock or signal. Phase locked loop is closed loop control system that associates the output phase with the input phase. High-performance digital systems use clocks to sequence operations and synchronize between purposeful units and between ICs. Clock frequencies and data rates have been swelling with each generation of processing technology and processor architecture. Within the digital systems, well-timed clocks are generated by phase-locked loops (PLLs). The prompt upsurge of the system's clock frequency possesses challenges in generating and distributing the clock with low uncertainty.

2. Methodology and Design Consideration

It is actually significant to select the accurate technology library and process before designing a circuit [22]. The technology expresses the model parameters associated with the devices that are used in the schematic and it also provides the ground rules for laying out a circuit. In the anticipated design Mentor Graphics Design Architect IC (DA-IC) Technology CMOS process was used. The current-starved VCO is shown in Figure 1. The VCO is composed of 7 cascaded inverters. The inverter schematic is given in Figure 2.

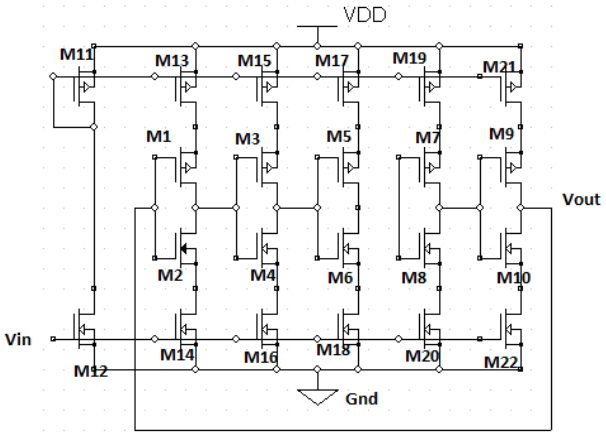

Figure 1. Current-starved VCO

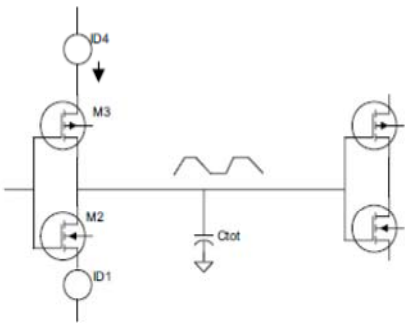

Figure 2. Inverter Schematic

2.1. Design Steps

Design steps as follow:

1) The inverter sizes M2 and M3, of Figure 1, are calculated.
2) The capacitance is calculated as:

$$C_{total} = (5/2)C_{ox}(\mathrm{WPLP} + \mathrm{WNLN}) \quad (1)$$

3) The number of stages of the oscillator is selected

The circuit of current starved VCO is same as the ring oscillator. Middle P_{MOS} M1 and N_{MOS} M2 play role as inverter while upper P_{MOS} M13 and lower N_{MOS} M14 operate as current sources. The current sources limit the current available to the inverter. In other words, the inverter is starved for current. The current in the first N_{MOS} and PMOS are mirrored in each inverter/current source stage. P_{MOS} M11 and N_{MOS} M11 drain currents are the same and are set by the input control voltage The VCO output waveforms are in shown Figure 1. It is noted that the input Voltage = 2.5V, so the circuit transfers from the undesired balance point to the desired balance point Q. On the basis of the start circuit, this work designed an enable-control circuit, through an enable terminal EN to control the circuit work or not. This design was based on TSMC 0.5-μm process, and using TT (typical typical) process corners for circuit simulation. By looking to the model library file, we can get the following parameters (TT process corner model) that may be used for manual calculation in Table 1.

Table 1. Design Parameters

Device type	Maximum channel(length)	Minimum channel(length)	Model	Gate thickness	Threshold voltage
N MOS	0.5E-10	0.2E-6	49	0.2-0.5	0.5-1.8
P MOS	0.55E-10	0.2E-6	49	0.2-0.5	0.5-1.8

According to the simulation model, M1's threshold is about 0.5 V,to ensure the M1 working in saturated zone, need about 200 mV, overdrive voltage. So the voltage between M1's gate and source is about 1V. When calculate the wide long ratio of M1, according to Figure 2,

$$\mathrm{I_1} = \mathrm{K_N}\frac{\mathrm{W_1}}{\mathrm{L_1}}(\mathrm{V_{GS1}} - \mathrm{V_r})^{\,2},\ \frac{\mathrm{W_1}}{\mathrm{L_1}} = \frac{\mathrm{I_1}}{\mathrm{K_N}(\mathrm{V_{GS1}} - \mathrm{V_r})^{\,2}} = 5$$

We select gate's length L=0.2 um, so W = 10 um. The next selection:

$$\frac{\mathrm{W_{N1}}}{\mathrm{L_{N1}}} = \frac{10}{2},\quad \frac{\mathrm{W_{P0}}}{\mathrm{L_{P0}}} = \frac{\mathrm{W_{P1}}}{\mathrm{L_{P1}}} = \frac{10}{2}$$

CEDEC 0.18μm process has been used to design and simulate the circuit diagram and the layout of the components. Finally, all components have been assembled together and tested at physical description level based on available CMOS technology. P_{MOS} and N_{MOS} sizes described as in Table 2.

Table 2. Device Sizes

Device number	Device type	Channel width	Channel length	Device number	Device type	Chanel width	Channel length
M1	N_{MOS}	10	0.5	M12	P_{MOS}	10	0.5
M2	N_{MOS}	10	0.5	M13	P_{MOS}	10	0.5
M3	N_{MOS}	10	0.5	M14	P_{MOS}	10	0.5
M4	N_{MOS}	10	0.5	M15	P_{MOS}	10	0.5
M5	N_{MOS}	10	0.5	M16	P_{MOS}	10	0.5
M6	N_{MOS}	8	0.2	M17	P_{MOS}	8	0.2
M7	N_{MOS}	8	0.2	M18	P_{MOS}	8	0.2
M8	N_{MOS}	8	0.2	M19	P_{MOS}	8	0.2
M9	N_{MOS}	8	0.2	M20	P_{MOS}	8	0.2
M10	N_{MOS}	8	0.2	M21	P_{MOS}	8	0.2
M11	N_{MOS}	8	0.2	M22	P_{MOS}	8	0.2

3. Results and Discussion

According to the pre-simulation waveform of current source designed by this paper, when the power supply voltage change from 1 to 6.5V and the power voltage bigger than 3 V, when power supply voltage fluctuates from 4V to 5.5V and the fluctuation range was 15.79%, the pre-simulation temperature coefficient of current source is 503 ppm; the enable pin can effectively control the circuit open or closed. After extract the parasitic parameters of layout take layout simulation, and do a detailed comparison between pre-simulation data and layout simulation data, the results showed that besides the temperature coefficient change a lot, the three other indicators of layout simulation are basically same with pre-simulation data, the parasitic parameters of layout influence the function of circuit is small. The circuit diagram of the V_{co} by using 11 P_{MOS} and N_{MOS} that parallel connected. A current starved ring oscillator for phase-locked loop (PLL) which has 11 P_{MOS} and 11 N_{MOS} has successfully developed and verified with DRC and LVS clean.

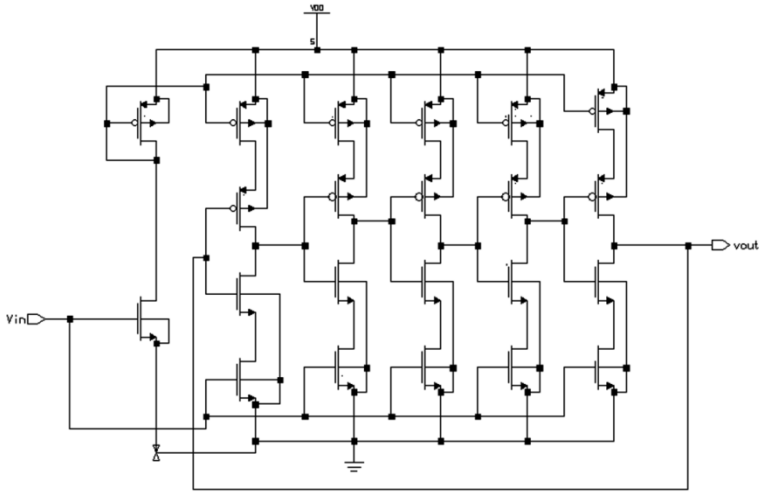

Figure 3. VCO Schematic

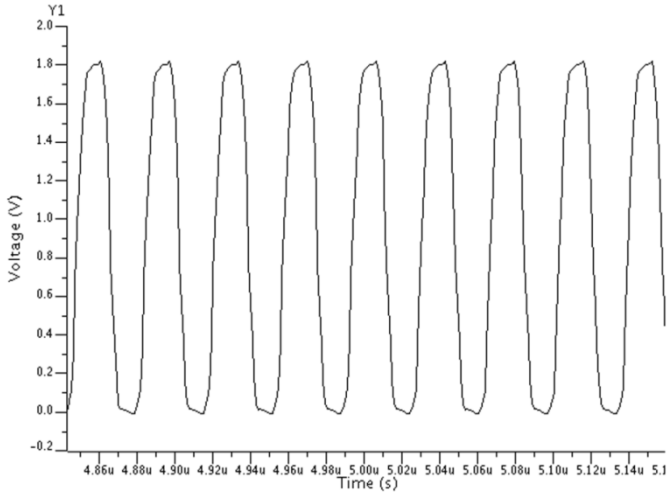

Figure 4. Current Starved VCO Output Waveform

Table 3. Control Voltage vs. Frequency of Current Starved VCO

Control voltage	Frequency(MHz)
0.5	129.3
0.6	147.05
0.7	161.29
0.8	178.57
0.9	188.67
1	192.30
1.1	203.99
1.2	208.62
1.3	212.24
1.4	212.77

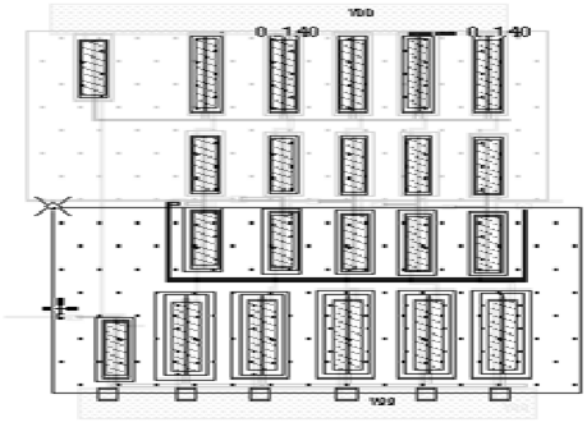

Figure 5. Current Starved VCO Layout Design

4. Conclusion

A simple VCO circuitry has been designed using the 0.18-μm CMOS technology. According to the pre-simulation waveform of current source designed by this paper, when the power supply voltage change from 1.8 to 6.5V and the power voltage bigger than 3 V when power supply voltage fluctuates from 4V to 5.5V and the fluctuation range is 15.79%, the enable pin can effectively control the circuit open or closed. After extract the parasitic parameters of layout take layout simulation, and do a detailed comparison between pre-simulation data and layout simulation data, the results showed that besides the temperature coefficient change a lot, the three other indicators of layout simulation are basically same with pre-simulation data, the parasitic parameters of layout influence the function of circuit little, and the layout this paper designed is perfect. This paper adopts the standard CMOS technology, therefore, the design of current source unit can be used as a module appeared in a complete chip design to provide static dc bias for other circuit module, and make them work in the appropriate dc operating point to ensure the whole chip can work normally.

References

[1] M Akter, MBI Reaz, F Mohd-Yasin, F Choong. A modified-set partitioning in hierarchical trees algorithm for real-time image compression. *J. Communications Technology and Electronics*. 2008; 53: 642-650.

[2] S Mogaki, M Kamada, T Yonekura, S Okamoto, Y Ohtaki, MBI Reaz. *Time-stamp service makes real-time gaming cheat-free.* Proc. Network and System Support Workshop. 2007; 135-138.

[3] F Choong, MBI Reaz, TC Chin, F Mohd-Yasin. *Design and implementation of a data compression scheme: A partial matching approach*. Proc. Computer Graphics, Imaging and Visualization. 2006; 150-155.

[4] F Choong, MBI Reaz, F Mohd-Yasin. *Power quality disturbance detection using artificial intelligence: A hardware approach.* Proc. IEEE Parallel and Distributed Processing Symp., 2005; 146a.
[5] MBI Reaz, F Mohd-Yasin, MS Sulaiman, KT Tho, KH Yeow. *Hardware prototyping of boolean function classification schemes for lossless data compression.* Proc. IEEE Computational Cybernetics Conf., 2004: 47-51.
[6] Assim, MBI Reaz, MI Ibrahimy, AF Ismail, F Choong, F Mohd-Yasin. An AI based self-moderated smart-home. *Informative*. 2006; 36: 91-94.
[7] MBI Reaz, WF Lee, NH Hamid, HH Lo, AYM Shakaff. High degree of testability using full scan chain and ATPG-An industrial perspective. *Journal of Applied Sciences*. 2009; 9: 2613-2618.
[8] MR Alam, MBI Reaz, MAM Ali. Statistical modeling of the resident's activity interval in smart homes. *J. Applied Sciences*. 2011; 11: 3058-3061.
[9] F Mohd-Yasin, MK Khaw, MBI Reaz. Radio frequency identification: Evolution of transponder circuit design. *Microwave Journal*. 2006; 49: 56-70.
[10] J Uddin, MBI Reaz, MA Hasan, AN Nordin, MI Ibrahimy, MAM Ali. UHF RFID antenna architectures and applications. *Scientific Research and Essays*. 2010; 5: 1033-1051.
[11] MJ Uddin, MI Ibrahimy, MBI Reaz, AN Nordin. Design and application of radio frequency identification systems. *European Journal of Scientific Research*. 2009; 33: 438-453.
[12] LF Rahman, MBI Reaz, MA Mohd Ali, M Kamada. *Design of an EEPROM in RFID tag: Employing mapped EPC and IPv6 address.* Proc. IEEE Asia-Pacific Conference on Circuits and Systems. APCCAS. 2010: 168-171.
[13] F Mohd-Yasin, MK Khaw, MBI Reaz. Techniques of RFID systems: Architectures and applications. *Microwave Journal*. 2006; 49: 62-74.
[14] FM Yasin, KF Tye, MBI Reaz. *Design and implementation of interface circuitry for CMOS-based SAW gas sensors.* Proc. IEEE International SOC Conference. 2005: 161-164.
[15] MK Khaw, F Mohd-Yasin, MI Reaz. *Recent advances in the integrated circuit design of RFID transponder.* Proc. IEEE International Conference on Semiconductor Electronics (ICSE 2004). 2004; 326-330.
[16] MBI Reaz, MS Sulaiman, FM Yasin, TA Leng. *IRIS recognition using neural network based on VHDL prototyping.* Proc. Information and Communication Tech. Symp., 2004: 463-464.
[17] WL Pang, MBI Reaz, MI Ibrahimy, LC Low, F Mohd-Yasin, RA Rahim. Handwritten character recognition using fuzzy wavelet: A VHDL approach. *WSEAS Trans. Systems*. 2006; 5: 1641-1647.
[18] MBI Reaz, PW Leong, F Mohd-Yasin, TC Chin. *Modeling of data compression using partial matching: A VHDL approach*. Proc. Wireless Congress. 2005: 411-416.
[19] YK Teh, F Mohd-Yasin, F Choong, MI Reaz, AV Kordesch. Design and analysis of UHF micropower CMOS DTMOST rectifiers. *IEEE Trans. Circuits and Systems II: Express Briefs*. 2009; 56: 122-126.
[20] F Mohd-Yasin, MT Yap, MBI Reaz. CMOS instrumentation amplifier with offset cancellation circuitry for biomedical application. *WSEAS Trans. on Circuits and Systems*. 2007; 6: 171-174.
[21] NB Romli, M Mamun, MAS Bhuiyan, H Husain. Design of a Low Power Dissipation and Low Input Voltage Range Level Shifter in Cedec 0.18-µm Cmos Process. *World Applied Sciences Journal*. 2012; 19: 1140-1148.
[22] HJ Chen. A Digital Phase-Locked Loop with Novel Frequency Estimation and Phase Error Compensation. M. Eng. Thesis, National Taiwan University of Science and Technology, Taiwan, 2012.
[23] P Andreani. A TX VCO for WCDMA/EDGE in 90 nm RF CMOS. *IEEE J. Solid-State Circuits*. 2011; 46(7): 1618-1626.
[24] RK Patil, VG Nasre. Current Starved Voltage Controlled Oscillator for PLL using 0.18µm CMOS Process. *Proc. Int. J. Eng. and Innovative Tech*., 2012; 1(2): 48-52.
[25] G Jovanovic´, M Stojc˘ev, Z Stamenkovic. *A CMOS Voltage Controlled Ring Oscillator with Improved Frequency Stability.* Scientific Publications of the State University Of Novi Pazar Ser. A: Appl. Math. Inform. And Mech. 2010; 2(1).