Indonesian Journal of Electrical Engineering and Computer Science
Vol. 38, No. 3, June 2025, pp. 1553~1563
ISSN: 2502-4752, DOI: 10.11591/ijeecs.v38.i3.pp1553-1563

Optimization of single electron transistor based digital logic design

Shobhika Pankaj Gopnarayan[1], Shriram D. Markande[2], Vaishali P Raut[1]
[1]Department of Electronics and Telecommunication Engineering, G.H. Raisoni College of Engineering and Management, Pune, India
[2]Department of Electronics and Telecommunication Engineering, Sinhgad Institute of Technology and Science, Narhe, Pune, India

Article Info

Article history:

Received Mar 24, 2024
Revised Dec 18, 2024
Accepted Feb 27, 2025

Keywords:

CMOS
Coulomb blockade
Coulomb oscillation
Delay
Power consumption
Single electron transistor

ABSTRACT

This paper addresses the challenge of high-power consumption and delay in conventional complementary metal-oxide-semiconductor (CMOS) circuits, particularly in the design of digital logic gates. The objective is to develop a hybrid CMOS-single-electron transistor (SET) model that reduces power consumption while maintaining acceptable performance in terms of delay. The proposed model leverages coulomb oscillation in SETs to create a changeable transconductance area, which significantly reduces energy usage. Simulation results demonstrates that the hybrid CMOS-SET circuits achieve up to 30% lower power dissipation compared to traditional CMOS designs, although a slight increase in delay is observed in complex gates like the OR gate. The novelty of this work lies in its use of coulomb oscillation for dynamic transconductance control, providing an innovative approach to balancing power efficiency and speed in nano-scale digital circuits. This makes the proposed model a promising candidate for future low-power, high-performance integrated circuits.

Corresponding Author:

Shobhika Pankaj Gopnarayan
Department of Electronics and Telecommunication Engineering
G.H. Raisoni College of Engineering and Management
Pune, India
Email: shobhikaingle@gmail.com

1. INTRODUCTION

Digital logic gates are the fundamental building blocks of digital circuits, performing basic operations like AND, OR, NOT, NAND, NOR, XOR, and XNOR. These gates are essential in constructing complex computational systems, from simple logic circuits to intricate microprocessors [1]. Traditionally, these gates have been implemented using complementary metal-oxide-semiconductor (CMOS) technology, which has driven the rapid advancements in electronics over the past few decades [2]. However, as the demand for higher integration density, lower power consumption, and faster operation grows, CMOS technology faces limitations, especially as devices shrink to the nanometer scale. This has led researchers to explore alternative technologies, such as single-electron transistors (SETs), which operate on quantum mechanical principles and offer a promising path toward ultra-low-power digital circuits [3]. SETs are a type of nanoscale device that operates by controlling the flow of individual electrons through a small conductive island [4]. The operation of SETs is governed by the Coulomb blockade effect, which occurs when the charging energy of the island is significant enough to prevent electrons from tunneling onto it unless a specific voltage threshold is met [5]. This allows SETs to achieve high sensitivity and operate with minimal power consumption [6]. Due to their quantum nature, SETs can be extremely small, making them attractive for applications in nanoelectronics where space and power efficiency are critical [7].

In recent years, digital logic gates using SETs have gained significant attention due to their potential advantages over conventional CMOS-based gates [8]. SET-based logic gates can operate at very low power levels, making them ideal for applications where energy efficiency is paramount. Additionally, the small size of SETs enables higher integration densities, which is crucial as the electronics industry continues to push the boundaries of miniaturization [9]. Furthermore, SETs can operate at high speeds, offering the potential for faster processing in digital circuits [10]. However, despite these advantages, there are several challenges associated with using SETs in digital logic gates. One major issue is the high sensitivity of SETs to noise and thermal fluctuations, which can lead to unreliable operation [11]. The small size of SETs makes them particularly vulnerable to environmental perturbations, necessitating the development of robust designs that can mitigate these effects. Another significant challenge is the limited scalability of SETs due to fabrication constraints [12]. Producing SETs with consistent characteristics at a large scale is difficult, which hinders their widespread adoption. Additionally, SETs typically have low current drive capability, which can limit their performance in certain applications [13]. The high voltage requirements needed to control SETs also pose a challenge, as they may not be compatible with existing low-voltage CMOS technology.

To address these challenges, researchers are exploring several innovative approaches. Novel device architectures, such as hybrid field-effect transistor (SET-FET) devices, are being developed to combine the benefits of SETs with the strengths of traditional CMOS technology [14]. Advanced materials and fabrication techniques are being investigated to improve the scalability and reliability of SETs. For instance, quantum dot and nanowire-based SETs offer new possibilities for enhancing device performance [15]. Additionally, new logic gate designs and circuit topologies are being explored to optimize the performance of SET-based circuits [16]. Simulation and modeling tools are also playing a crucial role in this effort, enabling researchers to refine their designs and predict the behavior of SET-based circuits under various conditions [17]. Furthermore, the development of new device models and compact models for circuit simulation is helping to bridge the gap between theoretical research and practical applications. Beyond traditional digital logic, SETs are also being investigated for their potential in emerging applications such as neuromorphic computing and quantum computing. These fields require devices that can operate with ultra-low power and at high speeds, making SETs a promising candidate. By addressing the current challenges, SET-based digital logic gates aim to achieve several key goals: ultra-low power consumption, high-speed and high-frequency operation, high scalability and integration levels, improved noise immunity and robustness, and compatibility with existing CMOS technology. Hence, the contribution of the work is as:

- Developed an innovative approach by integrating CMOS technology with single-electron transistors (SETs) to enhance the performance of digital logic circuits.
- Proposed a new SET macro model that offers better accuracy in simulating SET behavior, particularly in capturing the Coulomb oscillation and staircase effects.
- Successfully designed and simulated various basic logic gates (NOT, OR, AND) using the hybrid CMOS-SET approach in Tanner tool, verifying the performance improvements in power and delay.
- Provided a comprehensive analysis and optimization of digital logic gates using SETs, highlighting their potential to replace conventional CMOS technology for ultra-low power applications.

The manuscript is organized in the following manner. In Section 2, the literature survey is discussed, Section 3 presents the existing approach and proposed CMOS with SETs.

2. LITERATURE SURVEY

The fabrication and modeling of SET enables various SET based designs in analog and digital domains. Sharifi *et al*. [18], presented an approach for implementation of logical gates having two-inputs utilizing a same singular-stage structure. They utilized different SETs for providing various input-output relation for designing gates. Findings showed that it achieved better results by achieving highest operating temperature, reduced power consumtion and enhanced the gate speeds. Patel *et al.* [19], presented a review on existing SETs and computing designs. Joshi *et al.* [20], presented a logical design based on arithmetic-logical-unit (ALU) and SETs. They incorporated both the advantages of SETs and ALUs and presented an approach which redued delay and power. Gyakushi *et al.* [21], presented a double gate SETs based on iron nanodot-array which utilized couloumb blockade ossically. Findings showed better results in comparison with other approaches. Biswas *et al*. [22], presented a comparison among SETs and thresholding-logical-gates (TLGs) where compared the performance of both the approaches using different gates. Biswas *et al.* [23], presented a modified version for SETs where the Input-Voltage characteristices were improved by controlling source and drain nodes. This work utilized different MOSFETs for experimentation. Findings showed better results for reducing energy. Sridevi *et al*. [24], modeleed a SET having single gate using Verilog A code, where the ALU-SET based approach showed power consumption of 0.52 nW and 350 pS delay. Madhuri *et al*. [25], presented a design based on logical gates and TLGs, where they controlled

threshold voltage using graphene nanoribbon. Various gates were utilized for testing. Findings showed that circuit area and delay was reduced by 64% and 41.3% respectively in comparison with existing approaches. Most of the reviewed works in the literature have successfully reduced delay and power consumption in SET-based designs, yet few have explored the use of Coulomb oscillation to create a changeable transconductance area. This gap leaves room for further optimization in energy efficiency and performance. To address this, the present work introduces a model that leverages Coulomb oscillation to produce a variable transconductance region, aiming to further reduce energy consumption while minimizing delay, offering a novel approach to enhance the effectiveness of SET-based digital circuits.

3. METHOD

3.1. Existing SET Macro model

The existing model has been taken from [21], as presented in Figure 1, where the analogous circuit's macro-model representation is summarized. In this model, R1, R2, and R3 are expressed using a cosine function to explain the Coulomb oscillation, while D2, D3, Vp, and -Vp are incorporated to describe the Coulomb staircase in the circuit. This representation provides a comprehensive approach to understanding single-electron transistor behavior by capturing both periodic oscillations and discrete charge transfer phenomena. The use of a cosine function ensures accurate modeling of resistance variations, which are crucial for predicting circuit performance. Additionally, the inclusion of voltage components and diodes helps simulate the nonlinear characteristics of electron tunneling. This macro-model serves as a foundation for further circuit optimizations and performance enhancements in nanoelectronic applications.

3.2. Proposed SET macro model

The gate should be capacitively related to the island, hence, this work presents a new proposed macromodel for SET, as presented in Figure 2. As a result, the RG component is replaced with a diode (facing each other) to block all conceivable current in the SET. When compared to the existing model, ids are higher because of the huge resistance RG component, which allows some current to flow, resulting in higher id.

4. RESULTS AND DISCUSSION

4.1. Design and simulation results of proposed macro model of SET

To design proposed macro model of SET, this work used four diodes, three resistance and two voltage source. Using Tanner tool, this work designed SET circuit and checked all the simulation result and power and delay. The proposed model in tanner tool is presented in Figure 3. Further, this work retained the Vds voltage source at 0.6 voltage and altered the Vgs voltage source from negative to positive by several voltage steps during the drain current Vs Vgs (gate to source voltage) period. The end outcome was depicted in the waveform as presented in Figure 4. Also, characteristic of the drain current Vs, Vds voltage time were kept at the Vgs voltage source 0.6 voltage constant and changed Vds voltage source from negative to positive by some voltage steps. the result is shown in Figure 5.

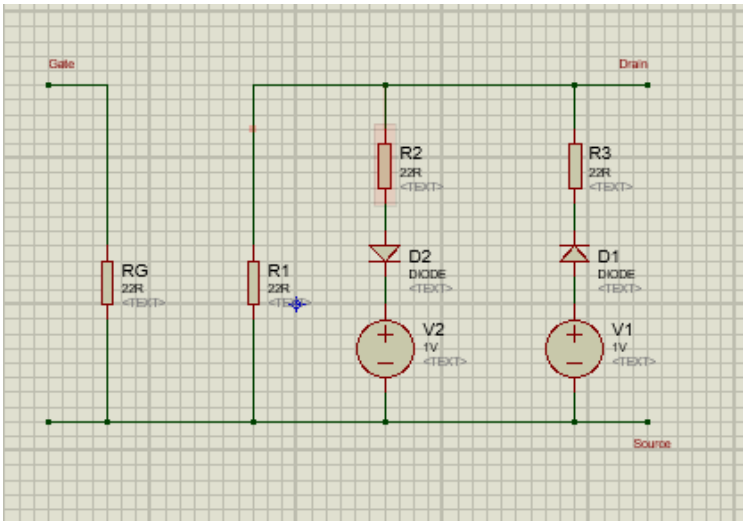

Figure 1. A SET's equivalent circuit

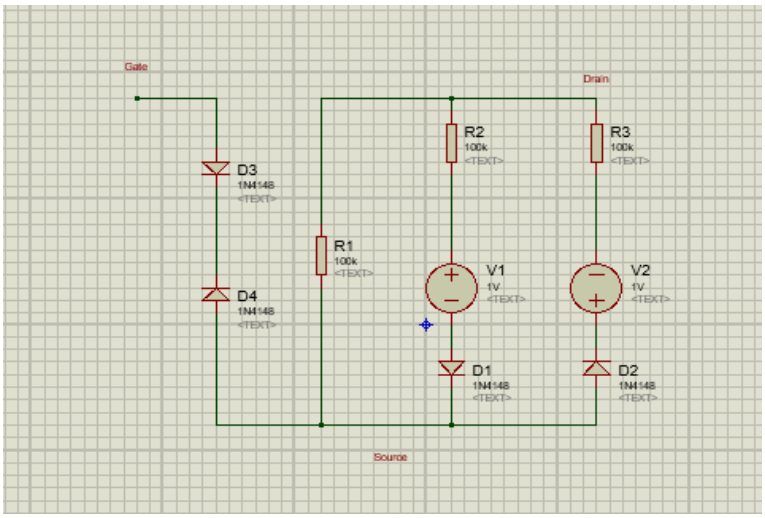

Figure 2. Proposed new macro model for SET

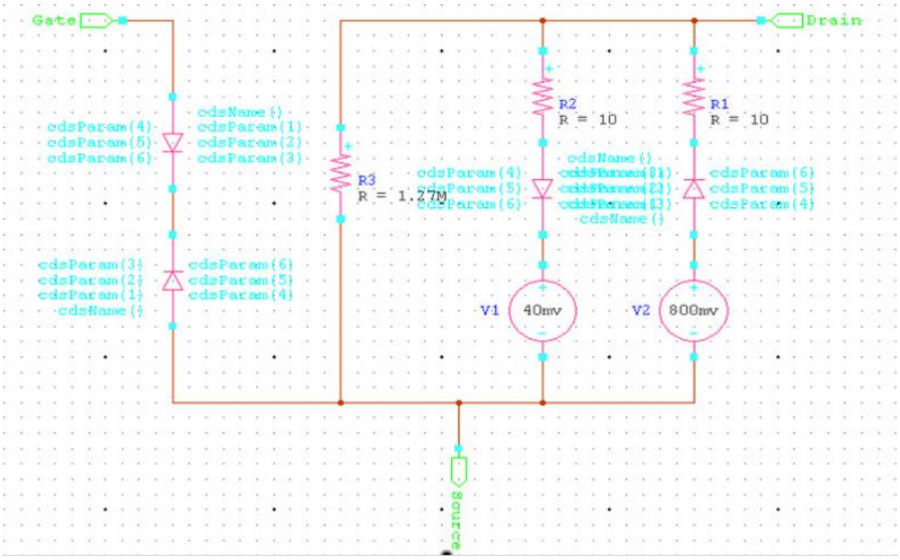

Figure 3. Proposed macro model of SET using tanner tool

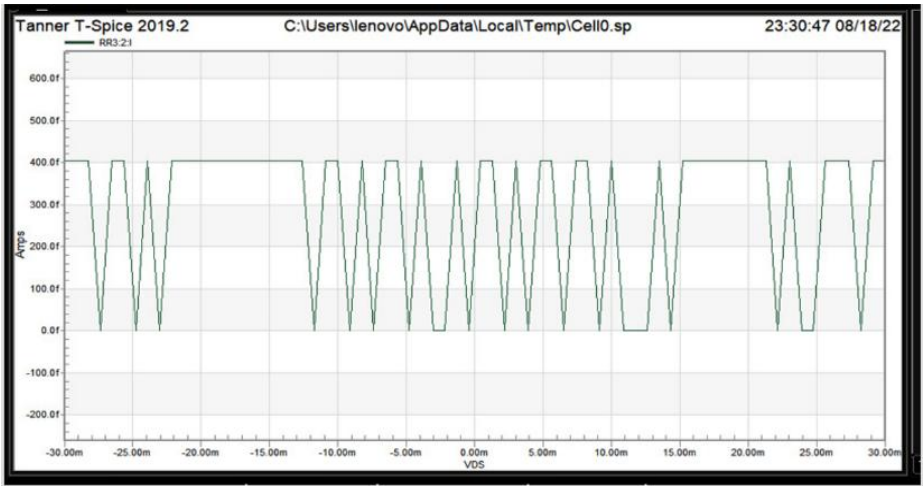

Figure 4. Drain current vs the gate voltage

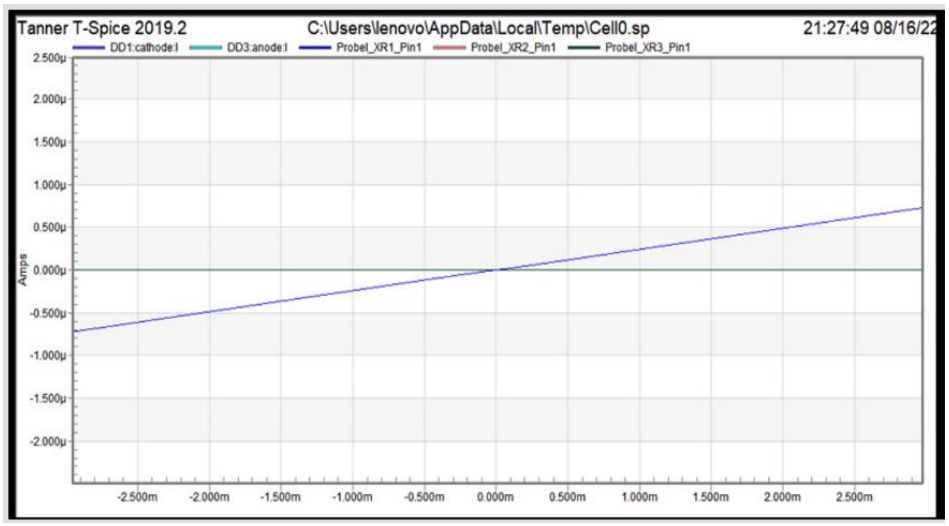

Figure 5. Drain current Vs drain voltage for the proposed model

4.2. Basic logic gate design and simulation using hybrid CMOS SET circuit

4.2.1. NOT GATE design

In this study, we designed a SET circuit to function as an N-channel metal-oxide semiconductor (NMOS) for creating a NOT gate. The SET circuit was modified to represent a single SET symbol with three terminals: gate, source, and drain, alongside a p-channel metal-oxide semiconductor (pMOS). Two voltage sources were utilized, as shown in Figure 6: one for the supply voltage (VDD) and the other for the input signal. The maximum VDD voltage was set to 300mV, and the input signal had a pulse voltage of 300mV with a pulse width of 10ms. Voltage display commands were implemented in the circuit to show both input and output voltages. Using the Tanner tool, simulations were built and supporting files loaded. As illustrated in Figure 6, when the input voltage (VI) is 0.3V (HIGH), transistor M1 (pMOS) is OFF, and the SET circuit, with both gate voltages at 0.3V (VDD), is ON, resulting in an output voltage (VOUT) of 0V (LOW). Conversely, when VI is 0V, transistor M1 is ON, and the SET circuit is OFF, producing a VOUT of 0.3V (HIGH). Thus, the circuit operates as an inverter.

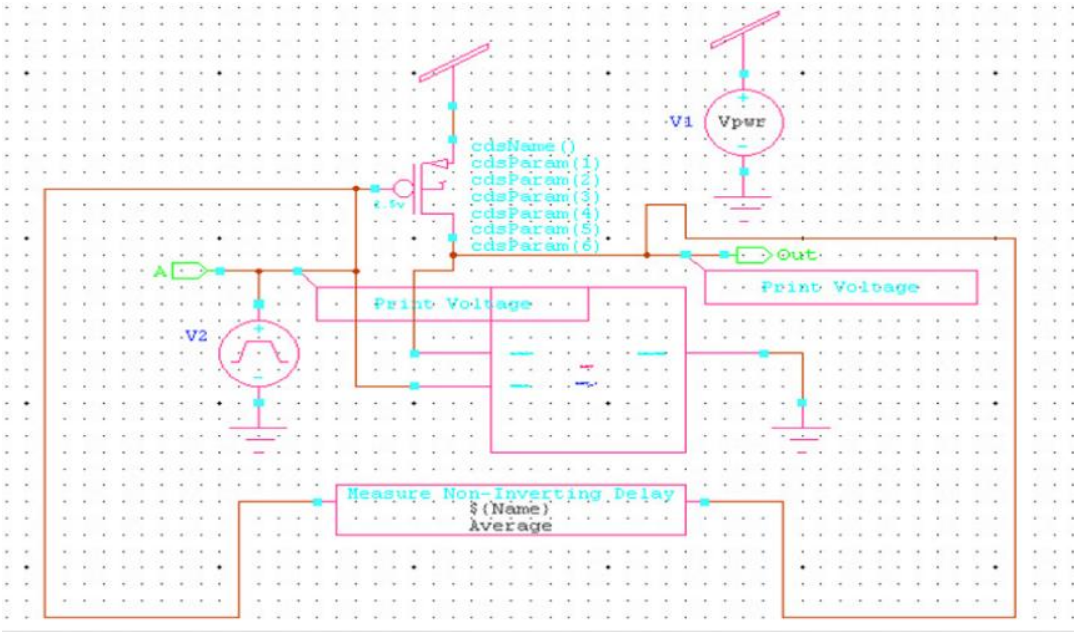

Figure 6. NOT gate design using hybrid CMOS SET

4.2.2. NOT GATE simulation result

In the waveform shown in Figure 7, the first red waveform represents the output of the NOT gate, while the green waveform indicates the input to the NOT gate, with a period of 10 milliseconds. The inversion behavior of the NOT gate is clearly observed, demonstrating a phase shift between the input and output signals. W-edit was used to generate the output waveform, ensuring accurate simulation of the circuit's response. Subsequently, T-edit was employed to analyze critical performance parameters such as power consumption and propagation delay. This analysis helps in evaluating the efficiency of the NOT gate and optimizing its design for low-power applications. The results obtained from these tools provide valuable insights into the overall functionality and performance of the circuit.

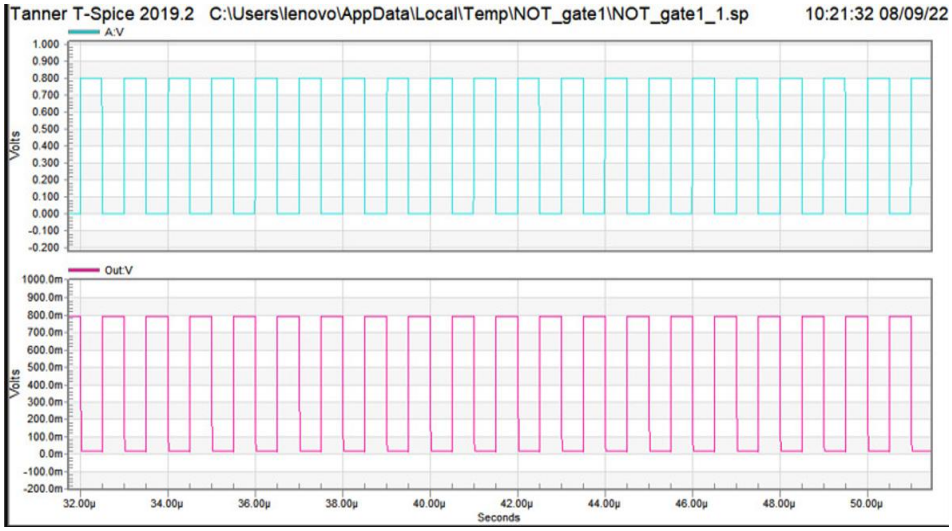

Figure 7. Not gate input and output waveform

4.2.3. OR GATE design

To create an OR gate using SET, three SET circuits were utilized in this work: one acting as an NMOS and two as PMOS, as shown in Figure 8. Additionally, three voltage sources were used—one for VDD and two for the input signals. The maximum VDD voltage was 300 mV, and the maximum input signal pulse voltage was 300 mV, with a pulse width of 5 ms for input A and 10 ms for input B. The voltage display command in the circuit was employed to show both input and output voltages. Simulations were built using the Tanner tool, and supporting files were loaded for the analysis. In the hybrid SET-CMOS NAND design presented in Figure 8, parameters were set with CG1 = CG2 = 1 aF and VDD = 3 mV. When both A and B are 0V, the VGS of M1 and M2 are both 0V. As the gate voltages are lower than the source voltages, both M1 and M2 are ON. With SET1 and SET2 at 0V, both SETs are OFF, and VOUT is connected to VDD via M1/M2, resulting in a high output. When A = 0V and B = 0.3V, the VGS of M1 remains 0V, while the VGS of M2 is 0.3V. This causes M1 to be ON and M2 to be OFF. SET1 is OFF (with a gate voltage of 0V), and SET2 is ON (with a gate voltage of 0.3V). VOUT is then connected to VDD via M1, resulting in a high output. When A = 0.3V and B = 0V, the VGS of M1 is 0.3V, and the VGS of M2 is 0V. Consequently, M1 is OFF and M2 is ON. SET1 is ON (with a gate voltage of 0.3V), and SET2 is OFF (with a gate voltage of 0V). VOUT is connected to VDD via M2, and the output remains high.

4.2.4. OR GATE simulation result

In the waveform shown in Figure 9, the red waveform represents the output of the OR gate, while the green and blue waveforms correspond to the inputs of the OR gate, with periods of 5 milliseconds and 10 milliseconds, respectively. The logical operation of the OR gate is evident, as the output remains high whenever at least one of the input waveforms is high. W-edit was used to generate the waveforms, ensuring precise visualization of the circuit's behavior. Subsequently, T-edit was employed to analyze key performance metrics, including power consumption and propagation delay. This analysis helps in assessing the efficiency of the OR gate and identifying potential optimizations for improved performance. The results provide valuable insights into the circuit's operation, which can be utilized for designing more efficient logic circuits in future applications.

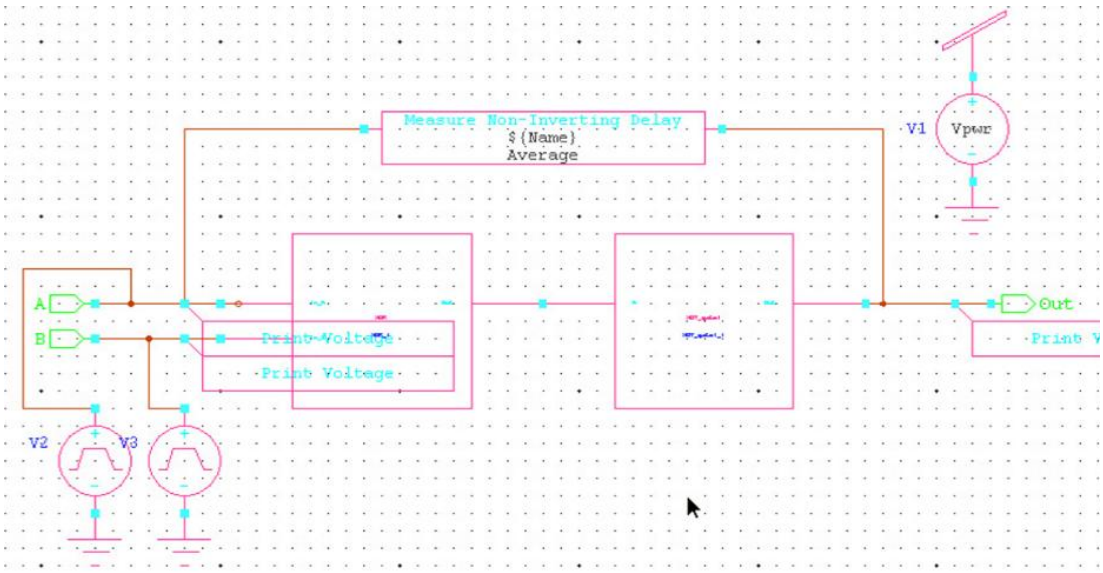

Figure 8. OR gate design using hybrid CMOS SET

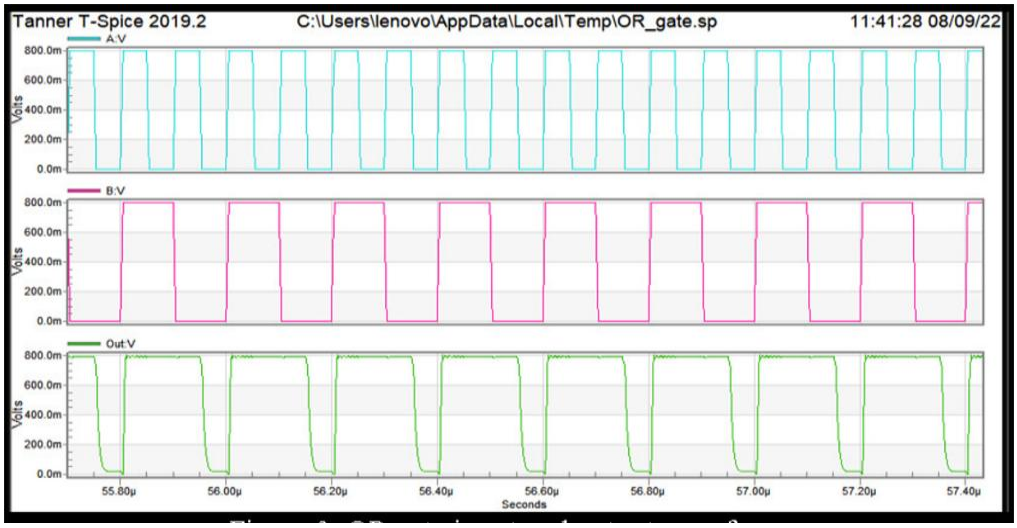

Figure 9. OR gate input and output waveform

4.2.5. AND GATE design

To design an AND gate using SET, this work employed three SET circuits, with one acting as an NMOS and the other two as PMOS, as shown in Figure 10. Three voltage sources were utilized—one for VDD and two for the input signals. The maximum VDD voltage was set to 300 mV, and the maximum input signal pulse voltage was also 300 mV, with input pulse widths of 5 ms for input A and 10 ms for input B. The voltage display command was used in the circuit to monitor the input and output voltages. Simulations and supporting files were built using the Tanner tool. In Figure 10, a hybrid SET-CMOS NAND gate was designed with parameters CG1 = CG2 = 1 aF and VDD = 3 mV. When both A and B are at 0V, the VGS of M1 and M2 are both 0V, causing both transistors to turn ON. Since the gate voltages of SET1 and SET2 are both 0V, both SETs remain OFF. With both SETs OFF, VOUT is connected to VDD via M1 and M2, resulting in a high output. When A = 0V and B = 0.3V, the VGS of M1 is 0V and the VGS of M2 is 0.3V, so M1 remains ON and M2 is OFF. In this case, SET1 remains OFF, and SET2 turns ON. VOUT is connected to VDD through M1, resulting in a high output. When A = 0.3V and B = 0V, the VGS of M1 is 0.3V and the VGS of M2 is 0V, causing M1 to turn OFF and M2 to turn ON. Here, SET1 is ON, and SET2 is OFF. VOUT is connected to VDD via M2, producing a high output.

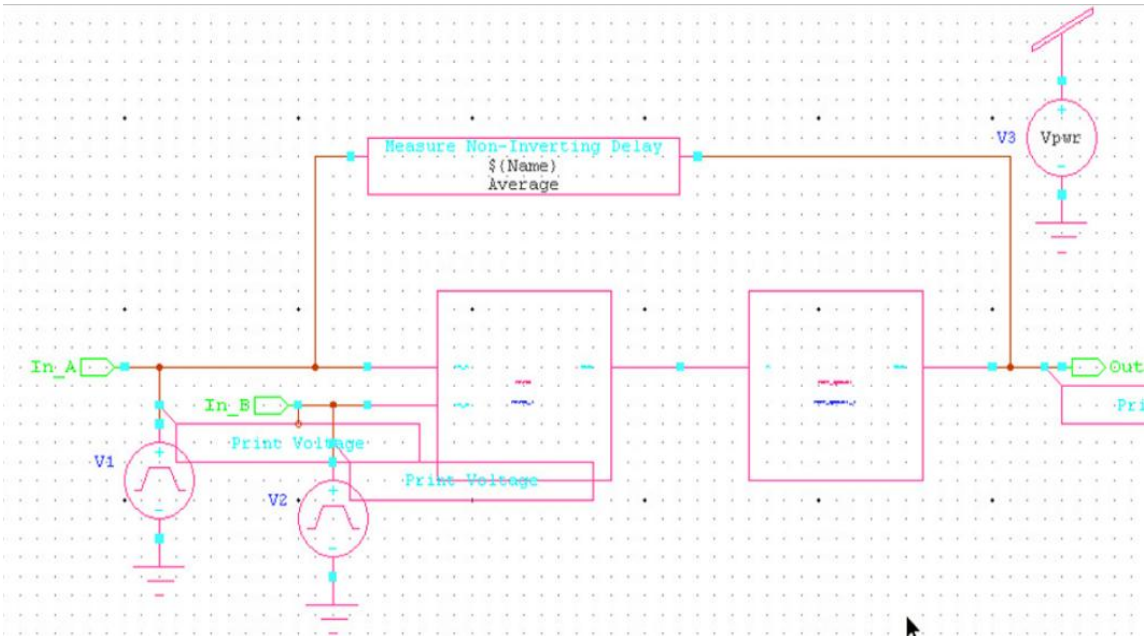

Figure 10. AND gate design using hybrid CMOS SET

4.2.6. AND GATE simulation result

The output of the AND gate is represented by the red waveform, as shown in Figure 11, while the inputs to the AND gate are indicated by the green and blue waveforms, with periods of 5 milliseconds and 10 milliseconds, respectively. The output remains high only when both input waveforms are simultaneously high, demonstrating the expected logical behavior of the AND gate. W-edit was used to generate the waveforms, ensuring accurate representation of the circuit's functionality. Following this, T-edit was utilized to analyze essential performance parameters such as power consumption and propagation delay. This evaluation helps in understanding the efficiency of the AND gate and optimizing its design for low-power and high-speed applications. The results provide valuable insights into the circuit's response, which can be instrumental in enhancing the performance of digital logic systems.

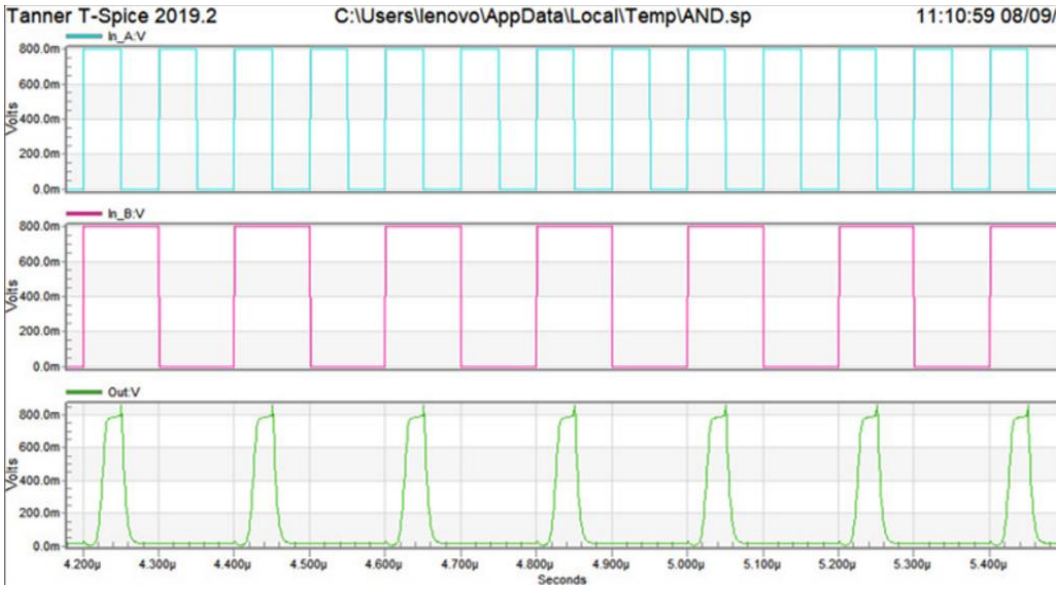

Figure 11. AND gate input and output wavefrom

4.2.7. Comparison of gate design using hybrid CMOS SET and existing gated of power and delay

The results presented in Table 1 demonstrate the power and delay metrics for the NOT, AND, and OR gates using the hybrid CMOS-SET design. The average power consumed by the NOT gate is the lowest at 4.738610×10^{-10} W, while the AND and OR gates consume 2.530024×10^{-9} W and 1.929572×10^{-9} W, respectively. The maximum power observed for these gates is relatively low, with the OR gate showing the smallest maximum power consumption at 8.2236392×10^{-8} W, indicating efficient power usage across the gates. The delay times, however, vary significantly, with the NOT gate exhibiting the shortest delay at 2.3746 ns, followed by the AND gate at 16.3991 ns, and the OR gate with the longest delay at 55.4868 ns. These results suggest that while the proposed hybrid approach is effective in reducing power consumption, there is a trade-off with delay, particularly for more complex gates like OR. Table 2 offers a comparative analysis of the proposed hybrid CMOS-SET design against existing CMOS-SET models from the literature. The hybrid NOT gate shows a significant improvement in power consumption, reducing it to 0.47 nW compared to 0.73 nW and 1.8 nW in existing designs. Additionally, the delay for the hybrid NOT gate is 2.3 ns, which is better than the 7.2 ps delay in some existing designs but falls short compared to the best delay of 1.02 ps. The AND gate in the hybrid design shows a power consumption of 1.965 nW and a delay of 16.39 ns, which is an improvement over some existing designs but not as efficient as the best-performing ones with a delay of 19 ps. The OR gate in the hybrid design consumes 2.02 nW of power and has a delay of 55.48 ns, which is lower in power compared to the existing design's 2.26 nW, but with a much longer delay.

Overall, the proposed hybrid CMOS-SET approach demonstrates significant potential in reducing power consumption, especially in simpler logic gates like NOT. However, the delay metrics indicate that while the design is competitive, particularly in terms of power, it still faces challenges in achieving the fastest possible operation, especially in more complex gates like OR. This suggests that while the hybrid approach offers advantages in energy efficiency, further optimization may be needed to minimize delays, particularly for applications where speed is critical. Additionally, the zero minimum power recorded across all gates suggests efficient power gating, which is a positive outcome for low-power applications. However, the variation in maximum power and delay times indicates that the hybrid design's performance is dependent on the specific gate architecture and the complexity of the logic function being implemented.

Table 1. Results

Metrics	NOT Gate	AND Gate	OR Gate
Average power consumed	$4.738610e^{-10}$	$2.530024e^{-09}$	$1.929572e^{-09}$
Maximum power	$3.418900e^{-07}$	$3.576484e^{-07}$	$8.2236392e^{-08}$
Minimum power	0	0	0
Delay	2.3746n	16.3991n	55.4868n

Table 2. Comparitive study

Model	Logic Gates	Power (Watt)	Delay (Sec)
Existing CMOS SET result	OR [18]	2.26n	24 p
	AND [18]	0.49n	19p
	NOT [19]	0.73	1.02p
	NOT [20]	1.8n	7.2p
	AND [20]	2.4n	23p
Using Hybrid CMOS SET	**NOT**	**0.47n**	**2.3n**
	OR	**2.02n**	**55.48n**
	AND	**1.965n**	**16.39n**

5. CONCLUSION

The study demonstrates that hybrid CMOS-SET circuits offer significant advantages in power efficiency, particularly for simple logic gates such as the NOT gate. The proposed hybrid design successfully reduces power consumption across various gates, as evidenced by the lower average and maximum power metrics when compared to existing CMOS-SET designs. However, the results also reveal that while the hybrid approach effectively lowers power usage, it does so at the cost of increased delay, especially in more complex gates like the OR gate. The findings suggest that while hybrid CMOS-SET technology holds promise for ultra-low power applications, further optimization is necessary to address the trade-offs in speed. The variations in delay indicate that the design may require additional refinement to achieve both low power consumption and high-speed operation, particularly in scenarios where fast response times are crucial. Future work could focus on enhancing the transconductance characteristics and exploring new circuit topologies to further optimize the performance of hybrid CMOS-SET circuits, potentially making them more viable for a broader range of digital applications.

FUNDING INFORMATION

This work has not been funded by any source.

AUTHOR CONTRIBUTIONS STATEMENT

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Shobhika Pankaj Gopnarayan	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Shriram D. Markande										✓		✓		
Vaishali P Raut										✓		✓	✓	

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare no conflict of interest.

DATA AVAILABILITY

The data supporting the findings of this study are publicly available. The data that support the findings of this study are openly available in Journal of Computational Electronics at http://doi.org/10.1007/s10825-020-01590-7, reference number [18], Microsystem Technologies at http://doi.org/10.1007/s00542-020-05002-5, reference number [19], IEEE International Symposium on Nanoelectronic and Information Systems (iNIS) at http://doi.org/10.1109/iNIS.2017.17, reference number [20].

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BIOGRAPHIES OF AUTHORS

Shobhika Pankaj Gopnarayan is Assistant Professor at AISSMS Polytechnic, Pune. She holds a Master degree in Electronics and Telecom Enggineering, specialization (Microwave Engg) from University of Pune and Bachelor's degree in Electronics and Telecom Enggineering from Pune University. Diploma in Electronics and Telecom Enggineering from MSBTE Mumbai, Maharashtra. Her research area includes electronics, electron devices, VLSI, microelectronics and nano technology. Currently persuing Ph.D. in VLSI (E & Tc) from, (Autonomous) Raisoni College of Engineering and Management, Wagholi Pune, under Pune University. She can be contacted at email: shobhikaingle@gmail.com.

Dr. Shriram D. Markande is a highly accomplished researcher and professional with a diverse academic background and extensive experience in the field of Electronics Engineering. He obtained his Bachelor of Engineering (BE) degree from Walchand College of Engineering, Sangli in 1985, showcasing a strong foundation in engineering principles early in his academic journey. Dr. Markande furthered his education by earning a Master of Engineering (ME) degree from the College of Engineering, Pune (COEP) in 1999, demonstrating a commitment to advancing his knowledge and expertise in the field. His academic pursuits culminated in a Ph.D. in Electronics Engineering from Bharati Vidyapeeth University, Pune in 2010, reflecting his dedication to research and scholarly contributions to the field of electronics. With a total experience spanning 38 years, Dr. Markande brings a wealth of knowledge and expertise to his research endeavors, making significant contributions to the advancement of electronics engineering and related fields. He can be contacted at email: sits@sinhgad.edu.

Dr. Vaishali P Raut is Assistant Professor at G H Raisoni College of Engineering and Management Pune SPPU, India. She Holds Ph.D. degree in Electronics Engineering with specialization I Microelectronics. Her research area includes VLSI, Microelectronics, Nano electronics. She has authored and co-authored in more than 25 publications in national and international journals and conferences with 100+ citations. She can be contacted at email: vaishraut02@gmail.com.