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Advances on Low Power Designs for SRAM Cell

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Abstract

As the development of complex metal oxide semiconductor (CMOS) technology, fast low-power static random access memory (SRAM) has become an important component of many very large scale integration (VLSI) chips. Lot of applications preferred to use the 6T SRAM because of its robustness and very high speed. However, the leakage current has increasing with the increase SRAM size. It consumes more power while in standby condition. The power dissipation has become an importance consideration due to the increase integration, operating speeds and the explosive growth of battery operated appliances. The objective of this paper is to review and discuss several methods to overcome the power dissipation problem of SRAM. Low power SRAM can be produced with improvement in term of power dissipation during the standby condition, write operation and read operation. Discharging and charging of bit lines consumes more power during write '0' and '1' compared to read operation. One of the methods to produce low power SRAM design is with make modification circuit at a standard 6T SRAM cell. This modification circuit will help to decrease power dissipation and leakage current. Several method was discussed in this paper for understand the method to produce low power design of SRAM cell. Recommendations for future research are also set out. This review gives some idea for future research to improve the design of low power SRAM cell.

Keywords: *leakage current, power dissipation, read write operation, SRAM*

1. Introduction

In modern world, integrated circuit (IC) is an advanced electric circuit by patterned diffusion of trace elements into the thin surface of a semiconductor material. All electronic equipment today is used IC and it has revolutionized the world of electronics [1-8]. Due to the introduction of complex metal oxide semiconductor (CMOS) technology, semiconductor devices spread through every discipline of engineering and CMOS memories become core component [9-15]. As CMOS technology development, the memory becomes the main power in the System-On-Chip (SOC) and part of the chip is the memory circuit. The memory chip is described as integrated circuit placed on a Printed Circuit Board (PCB). Random Access Memory (RAM) is the common name for the memory.RAM is fundamental system components used in the transfer and storage of data throughout computer system. In very large scale integration (VLSI) technology, memories developed in CMOS process are utilized in a number of applications as the sources of store data in RFID applications [16-23].

The first generation of RAM not chips at all, but rather ferrite rings used to store data by changing their polarity to represent a 0 or a 1 as data. RAM was not packaged as memory chips until the coming of the integrated circuit. Memory chips act as a matrix of switches that store the state of one bit as voltage. These states are a representation of the data currently being stored in RAM. These memory chips transfer to and from the different devices connected to a computer system. Memory chips provide a fast access area among the hard drives and CPU of a computer where data can be stored during processing without incurring the performance penalties of slower mechanical hard drives [24-25].

The two major of RAM are dynamic RAM (DRAM) and static RAM (SRAM). The SRAM and DRAM use different technologies to hold the data. The common type is use is DRAM. However, if the speed is importance, SRAM is faster than DRAM. SRAM does not necessary to be refreshed but DRAM must to be refreshed thousands of times per second. SRAM can give

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access times as low as 10ns, DRAM only support access times of about 60ns. SRAM is not common use like DRAM because SRAM is more expensive, despite it faster. Both type of RAM are volatile. Volatile mean when the power turned off the data content will lose.

In this study, the static RAM (SRAM) is focused. Advance in CMOS technology make it potential to design SRAM for decrease power consumption, increase speed performance and high integration density. To reach these objectives, the characteristic size device has been design to very small dimension and features. The technology scaling results in a significant increase leakage current of CMOS devices [26].

As the integration density of transistors increase, in today's SOC design and processors, leakage power has become an importance concern. Considerable attention has been paid to the design of high performance and low power SRAMs, as they are importance components in both high performance processors and handheld devices. Different design remedies can be implementing; the dynamic power consumption can reduce drastically decrease by power supply voltage. However, with an aggressive scaling in technology as predicted by the technology roadmap, substantial problems have already been encountered when the conventional 6T SRAM configuration is used at an ultra-low power supply [26]. This cell indicates weak stability at very small feature sizes.

This paper more focuses on power dissipation. The power dissipation has been a major consideration caused to the operating speeds and increased integration, as well as caused to the explosive growth of battery operating appliances. The major drives of fast low power design are supply and processes scaling still. This research studied dissipation in power, which can be used in conjunction for scaling to achieve fast low power operations. The power dissipation was happen during write, read and mode operation, so in this paper showed the several methods which use by researcher to reduce power dissipation during write, read or mode operation and finally some recommendation for future work.

2. Background

2.1. Conventional 6t SRAM Cell

The conventional 6T SRAM is quite similar to the static SR latch. It is the combination of two inverter and two transistors for control the circuit call Word Line. The standard SRAM requires six transistors per bit, two transistors (NMOS and PMOS) for each inverter and two transistors NMOS for access. The Word Line (WL) was replacing the clock to access the cell by enabled the line. It is controlled by two pass transistor M_5 and M_6, shared between the read and write operation. The SRAM can achieve high memory density by size it as small as possible. Figure 1 shows the circuit conventional 6T SRAM cell [27-28].

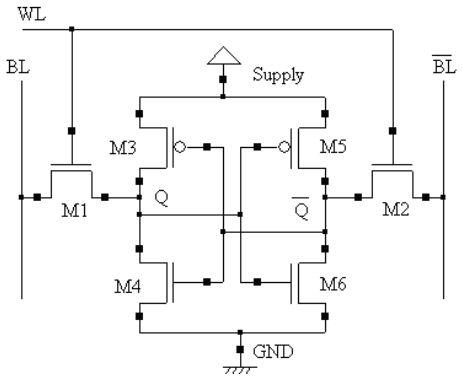

Figure 1. Conventional 6T SRAM Cell [25]

A conventional 6T SRAM cell has three condition operations. It is standby condition (circuit in idle), write operation (updating the data) and read condition (data has been requested). The "write stability" and "readability" should have during The SRAM operated in

write and read condition. Table 1 shows the ON/OFF transistor during write and read operation. The three states operation as follows:

In the standby mode, the transistors M_5 and M_6 are turn 'OFF' and disconnect the cell from the bit lines [29]. As long as the two cross-coupled inverters (M_1, M_2, M_3 and M_4) connected to the supply, it will continue to reinforce each other.

Assume value at Q node is 1 and Q bar node is'0'. The read process is begun by the bit lines are both initially floating high, then the word lines is 'HIGH', transistors M_1 and M_2 are turn 'ON'. Value '1'stored in Q note is pass to the bit lines by leaving BL at its pre-charge value and BL bar was discharge via transistors M_2 and M_6 to a ground [30]. At BL, the transistors M_1 and M_3 pull the bit line to '1'. On the other hand, when the value at Q node is '0' and Q bar node is'1', the BL pull to '1' while BL bar to '0'. Between BL bar and BL will have a minor difference of delta. After that, these lines reach a sense amplifier, which will sense amplifier which line has higher voltage. Thus will inform there was '0' or '1' stored. The faster the speed of read operation is be reach if the higher the sensitivity of sense amplifier [29].

If value '1' needs to be writing, first the value '1' should be applying to the bit lines. The transistor M_6 is turn 'ON' and discharge the charge on Q bar node via M_2 and M_6. Q bar is '0'; the transistor M3 is turn 'ON' and transistor M_4 is turn 'OFF'. In this situation, the charge was stored on the Q node.

Conversely, value '0' needs to write, the value '0' should be apply to the bit line. When Word Line (WL) is 'HIGH', transistors M_1 and M_4 is turn 'ON' and charged sore at the BL discharge to ground via transistors M_1 and M_4. The node Q is '0' so the transistor M_5 is turn 'ON' and transistor M_6 is turn 'OFF'. The charge stores at B bar lines.

Table 1. Transistor Turn On/Off during Read and Write Operation [29]

	M1	M2	M3	M4	M5	M6
Read 1	ON	ON	ON	OFF	OFF	ON
Read 0	OFF	OFF	OFF	ON	ON	ON
Write 1	OFF	ON	ON	OFF	OFF	ON
Write 0	ON	OFF	OFF	ON	ON	OFF

The cause of the power dissipation due to three factors; the dynamic and static power dissipation and subthreshold leakage channel. While the dynamic power dissipation is classified into two categories, one is short circuit power and second is power consumption during switching.

The short circuit powers is the input signal has a limited slope and can cause direct path current flowing via the gate for a short time during the switching operation.For this short time frame, there is a short circuit path between V_{DD} and ground and the circuit using a large number of powers [30-31].

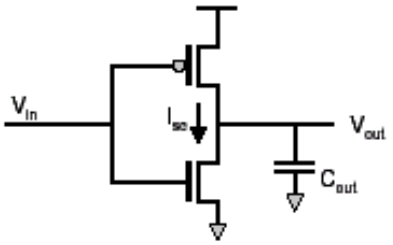

Figure 2. Short Circuit Power Dissipation [31]

The equation the energy consumption per switching can be derive from refer to the Figure 2.

$$E_{dp} = V_d * I_{peak} * t_{sc} \quad (1)$$

$$P_{shortcut} = V_{dd} * I_{peak} \quad (2)$$

Where,
V_{dd} = voltage supply,
I_{peak} = Peak current,
t_{cs} = time period power consumption

Short circuit power can be reduce with matching the fall and rise times. But in real world, the times are not matched, since optimizing for propagation delay can result in unmatched times. Therefore, in the digital circuit, the circuit power is a bigger source of power consumption [30], [32-33].

Power consumption during switching is a charge is flow from V_{DD} to the V_{OUT} of the inverter, after and current input transaction, with this $V_{OUT}$was pull to $V_{DD.}$ The lumped capacitance CL causes from gate capacitances and from parasitic wire capacitance of the gate capacitance of the logic gates driven by inverter, which is show in Figure 3.

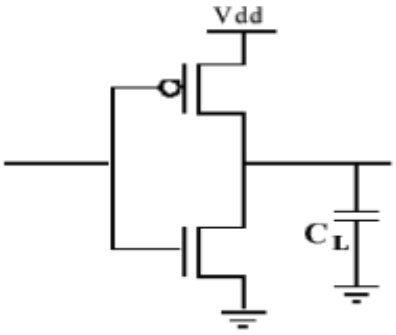

Figure 3. Dynamic Power Dissipation [31]

When the opposite switchover of the input, transistor NMOS is turn 'ON' and transistor PMOS is turn 'OFF'. The charge on CL is discharge to ground.This situation is calling the dynamic power dissipation. In CMOS circuit, it is the largest source of energy dissipation. Conclude that, one rise and following fall transition of the output consume energy is [31], [34-36]:

$$E = C_{Load} * V_{dd} * V_{dd} \quad (3)$$

Where,
C_{LOAD} = the load capacitance and
V_{DD} = the power supply.

If f is the clock frequency and the average number of 'HIGH' to 'LOW' or 'LOW' to 'HIGH' of the node is denoted by α then the power consumption due to capacitive switching is given by:

$$P_{switching} = \alpha C_{Load}(V_{dd})^2 f \quad (4)$$

Where,
α = activity factor,
V_{DD} =voltage swing of the output node,
C_{LOAD}= effective capacitance of the output load and
F = switching frequency.

The static component of power consumption has been ignored in static CMOS. But, a number of leakage mechanisms begin to gain significance. Most of these mechanisms are indirectly or directly cause to the small device geometries [31], [34-35].

(a) I_{hot} = gate current
(b) IPT = channel punch through leakage
(c) I_{sub} = the subthreshold leakage current
(d) I_{gate} = the gate oxide tunneling
(e) IGIDL = gate induced drain leakage
(f) I_{rev} = reverse bias pn junction leakage

Sub-threshold leakage via a MOS device channel called the second source of leakage current. Despite a transistor is turn 'OFF', but still have leakage current, via the channel at the microscopic level. This current is called, as the sub-thereshold leakage current due it happens during the gate voltage is below $V_{th.}$ Equation of leakage current is:

$$Isub = Ae^{\frac{Vgs-Vth}{nkT/q}}(1-e^{\frac{-Vds}{kT/q}}) \quad (5)$$

From the equation we can see directly the sub-threshold leakage current is reduce if V_{th} increase and vice versa. Therefore asymmetric configuration deals with dual threshold voltage in each SRAM cell.

Researchers have done research to overcome this problem and propose several methods of solution. This paper will uncover a number of ways to solve the problem of power consumption.

2.2. Single Bitline 6t SRAM Cell

Majumdar and Basu are using the theory with decrease bit line capacitance of the SRAM cell will lower dynamic power dissipation without degrading the performance to design their proposed SRAM cell. So these designs SRAM only using a single bit line for write and read operation. Mean that only single bit process was involved for discharge and charge during their operation.

The leakage power and active power control the power consumed during the operation phase. A leakage power is the power consumed when charges leak via transistor that is turn 'OFF'. While an active power is the power, consumed when both pull-down and pull-up network are active, creating a direct current flow from V_{DD} to ground [37].

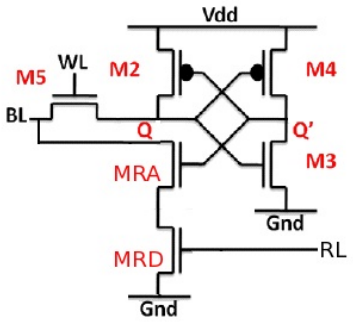

Figure 4. Low Power Single Bit Line 6T SRAM cell [37]

For every write operation of the conventional, before the precharge started, both of the bit line is placed complementary data is. Depend on the data value only one of the bit lines will charge. The circuit is assumed that the capacitor is discharge after the write is complete. So during a write operation the power dissipation is double. When read operation, both the bit lines once again are charged and then one is discharged during reading a '0', while the other is discharged after the operation is complete.

For the proposed 6T SRAM cell, only a single bit line is either charged if it is a '1' or does not get charged at all assuming that the data was already present before the precharge

circuit has been began. Assumedthe bit line is discharged after the write ‘1’ operation. In a read ‘1’ condition, the bit lines are precharged. Moreover, assumed the bit lines are discharged after the read process is over. During a read ‘0’ cycle, the bit lines capacitance is discharged and precharged via the cell [37].

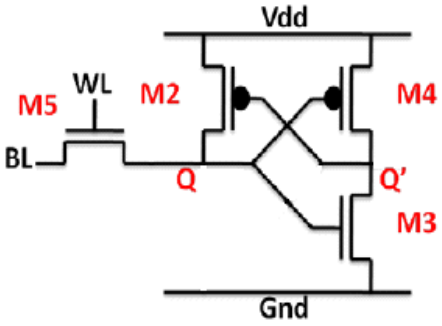

Figure 5. Four Transistor (Single Ended) SRAM Cell [37]

The circuit purposed 6T SRAM cell designed by way remove M_6 (PMOS transistor control WL for BL bar) and M_1 (NMOS transistor for connection Q node to ground) and was replacing by two NMOS transistor is calling Read Driver Transistor (MRA) and Read Driver Transistor (MRD). Both of these transistors create connection between BL lines to ground. The advantage of removing M_6 from circuit is it can be reduced by a factor of two of power consumption from charging. As only one bit line is charge during a read operation not of two and the line is charge during write operation about of time (assume equal probability of writing ‘1’ and ‘0’) instead of every time when a write operation is required. The cell areas reduce by one-bit line and one transistor. The advantage when M_1 transistor being taken away is the further reduction power consumption.

If Q content ‘1’ and Q bar ‘0’, both of memory nodes will lock each other at their respective voltage. Assume Q is‘0’ and Q bar ‘1’, Q is floating. See the Figure 4, the leakage current viatransistor M_2should be lower compare of transistor M_5 to make sure Q still stay at ‘0’.

If value ‘1’ needs to write, the word line is charge to V_{DD}, since NMOS transistor is stronger driver than PMOS transistor, no matter is incurred while writing a ‘0’ into the cell. The lack of the pull down NMOS transistor for memory Q allows writing a ‘1’ into the cell easily. Writing a ‘1’ is done by precharging bit line ‘1’ to V_{DD}. The Purposed SRAM and Conventional 6T SRAM have a same way to do operation write ‘0’.The bit line BL is discharge and then word line WL is charged to V_{DD}.

Alternately, if value at Q node is ‘0’ before read the value at Q nodes, the bit line is charge to V_{DD}. The MRD transistor was turn ‘ON’. The value at Q bar is ‘1’ so transistor MRA was turn on and will drain the charge on the bit line through transistor MRD to ground. That means the bit line has just read a ‘0’.Assume value at Q node is ‘1’ and Q bar will be ‘0’. The charge in bit line cannot pass through from MRD to ground because of transistor MRA is ‘OFF’.

These techniques can decrease of dynamic power consumption to only 40% to 60% (best case / worst case) compare of a conventional 6T SRAM cell. Table 2 shows the result of simulation done by Majumdar and Basu.

Table 2. Power Dissipation between Proposed SRAM and Conventional 6T SRAM Cell [37]

	Conventional 6T SRAM cell	Proposed SRAM cell
WRITE ‘0’	162µW	0µW
WRITE ’1’	162µW	81µW
READ ‘0’	243µW	162µW
READ ‘1’	243µW	81µW

2.3. SRAM Cell For Portable Devices

This design was focus to reduce power dissipation during write operation. Upadhyay et al. was suggest to include two more trail transistors (M_7 and M_8)between pull down network and ground level for proper discharging and charging a bit lines as shown in Figure 6 [25].

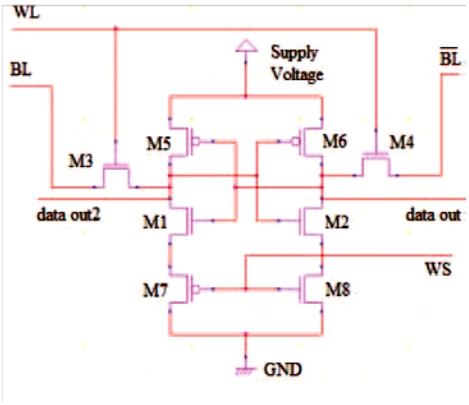

Figure 6. SRAM Cell of Upadhyay et al. [25]

The sub-threshold, which is flowing in the circuit during transistor, is in cut off region can reduced with use the two pull down transistors. Threshold voltage influence the leakage current in circuit. When sub-threshold current is increase, the threshold voltage is decreases. Because of drain induced barrier lowering (DIBL) in the MOSFET the drain voltage increases if the threshold voltage decreases. The equation can be derived as below [25, 38]:

$$Vth' = Vth - nVd \quad (6)$$

Where,
n = DIBL coefficient,
Vth= threshold voltage and
Vd= drain voltage.

The increase the threshold voltage by using two trail transistors has reduced the drain voltage with decreased sub-threshold current. Decreased sub-threshold can be reducing power dissipation. The main factor to ensure proper functioning of SRAM is the size of transistors. According to Thumb Rule, the Width ratio of transistors M_5 and M_3, M_3 and M_1, M_6 and M_4 and $M_4$and M_2, is equal to 1.5.

$$\frac{W_6}{W_4} \approx \frac{W_5}{W_3} \approx 1.5 \text{ and } \frac{W_4}{W_2} \approx \frac{W_3}{W_1} \approx 1.5 \quad (7)$$

This size configuration provides the proper driving voltage to transistors for turn 'ON' and 'OFF' condition. The M_7 and M_8transistors were function to reduce power dissipation with cut off the circuit during write '1' to '0' and '0' to '1'.

Assume want to write value '1'. Have 2 situations, from '1' to '1' or '0' to '1'. Node B must write to '0', to get node B '0', BL should setting to '0'and asserting WL. Figure 7 shows write '1' operation. Situation 1: from '1' to '1' write to cell. This is not possible because both node B and BL are at zero potential. Situation 2: from '0' to '1' write to cell. In Upadhyay et al. proposed cell, it is simple to flip the cell state from '0' to '1' by before asserting WL, turn ON transistor M_7 with set WS is '1'.

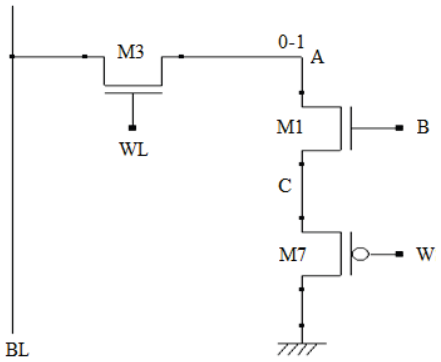

Figure 7. Path for Write “1” [25]

However, if someone wants to write value 0, then there have two situations, from ‘0’ to ‘0’ or ‘1’ to ‘0’. Node B must write to ‘1’, to get B node ‘1’ BL should set to V_{DD} and asserting WL. Figure 8 shows write ‘0’ operation. Situation 1: from ‘0’ to ‘0’ write to cell. Since node B is initially high, therefore this write pattern is not possible. Situation 2: from ‘1’ to ‘0’ write to cell. In Upadhyay et al. proposed cell, it is simple to flip the cell state from ‘1’ to ‘0 by set WS to ‘0’, so that charged cannot discharge through M_2 to ground [25]. The function of WS signal is to makes sure the right value of signal and the right operation before asserting WL, transition from 1 to 0 and 0 to 1 can be easily allowed.

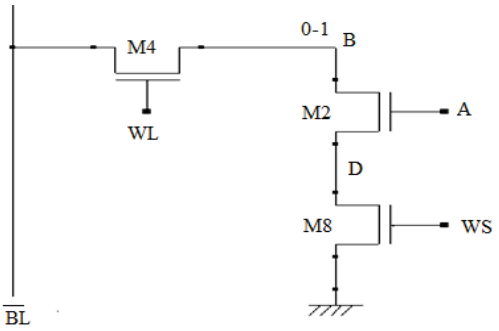

Figure 8. Path for write “0” [25]

The power dissipation during write ‘0’ and ‘1’ operation is more, causes one of the two bit lines of conventional 6T SRAM cell should be discharged to low regardless written value. In proposed SRAM, by control a signal WS, transistor M_7 or M_8 can be turn ‘OFF’. Proper control of signal WS can avoid any single bit line from being discharged during write ‘0’ or write ‘1’ mode.

The result of comparison between proposed SRAM and conventional 6T SRAM cell on different frequency during write operation are shown at Table 3. During the switching activity the proposed SRAM cell, dissipate lower dynamic power. Compare to conventional 6T SRAM cell, the power dissipation for proposed SRAM cell reduced by 12% to 38% [25].

Table 3. Power Dissipation between Conventional 6T SRAM and Proposed SRAM Cell [25]

Frequencies	Conventional 6T SRAM cell (uW)	Proposed SRAM celll (uW)	Percentage decrease (%)
500MHz	3.95	2.45	38.00
1GHz	6.01	4.97	19.8
2GHz	9.83	8.6	12.8

2.4. 7T SRAM Cell

Akashe and Jain proposed the circuit to reach improvements in performance, stability and power dissipation compared with a conventional 6T SRAM cell. The 7T SRAM cell is proposed for innovative precharging and bit line balancing scheme during write operation and maximum standby power saving in a SRAM array. Figure 9 shows proposed 7T SRAM cell [26].

The main source of standby power for a SRAM cell is leakage current which the major components is sub-threshold leakage, the gate direct tunneling leakage and the reverse biased band to band tunneling junction leakage. The subthreshold leakage, which is defined as a weak inversion conduction current of the CMOS transistor when Vgs < Vth, represents a significant leakage current component in the off-state [26];

$$Isub = Ioe^{\frac{Vgs-Vth}{nkT/q}}(1-e^{\frac{-Vds}{kT/q}})\text{e} \quad (8)$$

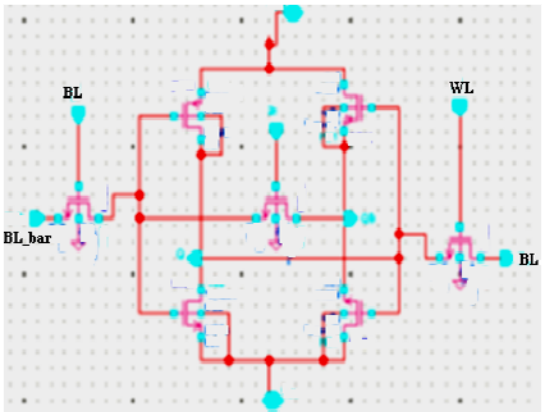

Figure 9. Proposed 7T SRAM cell of Akashe and Jain [26]

From Equation (8), the V_{ds} of the MOSFET influence the subthreshold current. When V_{ds} increase, the subthreshold current also increase. So Anie Jain and Shyam Akashe was adding M_5 (additional transistor) to reduce the sub threshold current [26].

$$Io = \mu Cox\left(\frac{W}{L}\right)\left(\frac{kT}{q}\right)^2(1-e^{1.8}) \quad (9)$$

From Equation (9), we know the sub threshold leakage current isproportional transistor size. Anie Jain and Shyam Akashe suggest with scaling down the pull down NMOS can reduce the leakage current.The BL voltage also affects the leakage current. The leakage current can be reduced by decrease the voltage.

Both bit line should be restore to V_{DD} following a write operation in the conventional 6T SRAM to make sure a successful read operation. The write amplifier circuitry of ensures that the selected bitline is back to a high value by generating a negative pulse to precharge the selected bitline high after driving the bitline 'LOW' to write '0' into a SRAM cell. Therefore, both bit lines (BL and BL bar) will be restored to high state after write operation [26, 38].

During the write operation, firstly cut off the feedback connection by turn 'OFF' transistors N_5. BL bar carries complement of the input data. Transistor N_3 is kept 'OFF' and transistor N_4 is turn 'ON'. The BL bar transfers the complement of input data to inverter 2 to develop Q, cell data, which drives inverter I and develops QB. Assume want to write '0'. BL bar is kept 'HIGH' with negligible write power consumption. Assume want to write 1. BL bar is discharged to '0' with comparable power consumption to a conventional write.

The read operation for purposed SRAM is same like conventional 6T SRAM cell and N_5 is turn 'ON'. Assume value at Q node is '0'. The read path consists of N_2 and N_4, and exactly behaves like the conventional cell. Assume value at Q node is '1'. The read path consists of N_1, N_5 and N_3 that represents a critical read path [26].

Anie Jain and Shyam akashe are using CADENCE for done the simulation and the result show at Table 4 and 5. The result show the proposed 7T SRAM a 45 % reduction in power consumption during write operation compare with a conventional 6T SRAM.

Table 4. Power Consumption between Conventional 6T and Proposed 7T SRAM cell [26]

Parameter	Power Consumption
6T	2.097mW
7T	1.147mW

Table 5. Leakage Current between Conventional 6T and Proposed 7T SRAM Cell [26]

Parameter	Leakage Current
6T	2.311mA
7T	1.148mA

2.5. Cache Design

Aly and Bayoumi proposed 7T SRAM cell for reduce power consumption during write operation. The charge and discharge of a bit line influence power consumption. The purpose SRAM only use BL bar for performs write operation and it depend on cutting off the feedback connection between the 2 inverters, inverter 1 and inverter 2, before a write operation. Figure 10 shows proposed 7T SRAM cell [39].

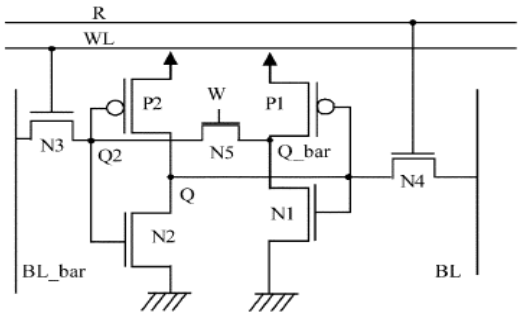

Figure 10. Aly and Bayoumi's 7T SRAM Cell

Aly and Bayoumi's proposed circuit is same as circuit proposed by Akashe and Jain's. Only have some difference at WL signal between these circuits. For circuit proposed by Aly and Bayoumi, the WL signal is isolated, which controls the transistors N_3 and N_4. However circuit proposed by Akashe and Jain's are using only single signal to control both transistors.

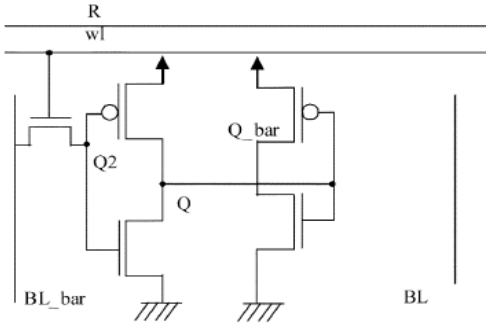

Figure 11. 7T SRAM –write operation of Aly and Bayoumi proposed

The transistor N_5 is kept 'OFF' for cut off the feedback during write operation. Transistor N_4 is turn 'OFF', transistor N_3 is turn 'ON' as show in Figure 11 and BL bar carries complement of the input data.

Now it is found that the purpose SRAM seem like two cascaded inverters, inverter2 followed by inveter1 as show in Figure 12. The data was transfer from BL_bar to Q_2 by transistor N_3 with driver inverter2 than was transfer toQ by transistor P_2 and N_2. After that data at Q was transfer to Q bar by transistor P_1 and N_1. This data is equal Q_2 if data is '0' and slightly higher than Q_2 if data is '1'. Then, transistor N_5 is turn 'ON' and WL is turn 'OFF' to reconnect the feedback link between the two inverters to stably store new data [39].

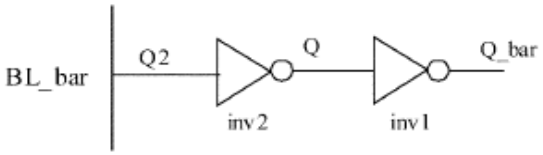

Figure 12. Equivalent Circuit [39]

Assume want to write '0'. Both BL_bar and BL are precharged high. Using the proposed write scheme, BL bar is kept high with negligible power consumption and designing properly transistor sizing is importance to ensure a stable write '0' operation as explained below.Assume want to write '1'. BL bar is discharged to '0' with comparable power consumption to the conventional 6T SRAM cell. To write a '0' in the cell, there is no need to discharge BL bar and therefore, the activity factor of discharging BL bar is less than '1' and depends on the percentage of writing '1' [39].

Transistor $N_5$is turn 'ON', both WL and R signals are turned 'ON'. Assume value at Q is '0','the read path consists of transistor N_4 and N_2, as shown in Figure 13, and behaves like a conventional 6T SRAM cell.

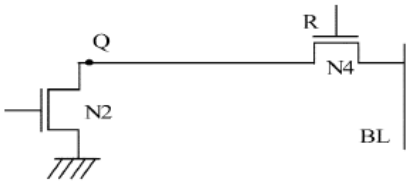

Figure 13. Read Path when Q = 0

Assume value at Q is '1' the read path consists of transistor N_3, N_1 and N_5,which represents a critical read path as shown in Figure 14. In a critical sidethis three series of transistor should be carefully sized, otherwise it will result in reduce the driving capability of the cell.

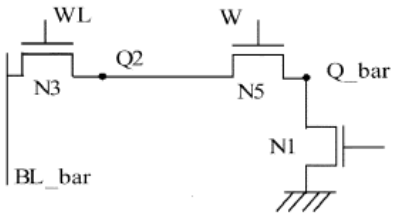

Figure 14. Read Path when Q = 1[39]

Aly and Bayoumi was done analysis in term of power consumption and result can see at Table 6. During write '0', when the original value data is '0'power can save by 99.9% because BL_bar not necessary discharge to ground. While, when the original data is '1' power can decrease by 96%.

When write '1', the additional BL_bar interconnects capacitance cause the power consumption increase by 1.5% [39].

At the worst case patterns, where the probability to write '0' equals that to write '1', using simulate with HSPICE, the proposed 7T SRAM cell achieves 49% bit line power saving while maintaining read delay and SNM. During read operation, comparison read power between proposed SRAM cell and conventional SRAM cell show that read power has increase by 2.3% due to the increase in the cell size, which leads to longer word line interconnect and using two separate wires, WL and R, to activate the cell.

Table 6. Power Consumption for Different Input Patterns [39]

Write pattern	Conventional(uW)	Proposed(uw)	Reduction (%)
0 to 0	113.5	7E-2	99.9%
0 to 1	116.7	118.4	-1.4%
1 to 0	116.5	4.7	96%
1 to 1	113.3	115	-1.5%

2.6. Symmetric and Balanced 11-T SRAM Cell

Singh et al. proposed a new design, which can decrease the power consumption during read and write operations. the power consumption during write '1' and '0' operation can be decreased by insert two tail transistors in the pull down path of the respective inverter. While to reduce power consumption during read operation, another transistors had included. During read operation, the circuit acts as a conventional 6T SRAM cell.

The proposed circuit includes another transistor to reduce the power consumption in read operation and allow the circuit to act as a conventional 6T SRAM cell during read operation. The bit and bit bar line are controlled by switching behaviour of the tail transistors. Write operation using two-bit line and read operation only use one bit line.

The propose circuit is shown at Figure 15. The circuit have 11 transistors include six transistors same as conventional 6T SRAM cell. The proposed cell includes two transistors NMOS N_6 and $N_8$are used for read operation and another two tail transistors N_7 and N_9 (which are controlled by bit line and bit bar line respectively). The write operation is controlled by write word line (WWL) using transistor N_3 and N_4. The read operation is performed through access transistor N_5 that is driven by read word line RWL. Read operation uses single bit-line RBL [40].

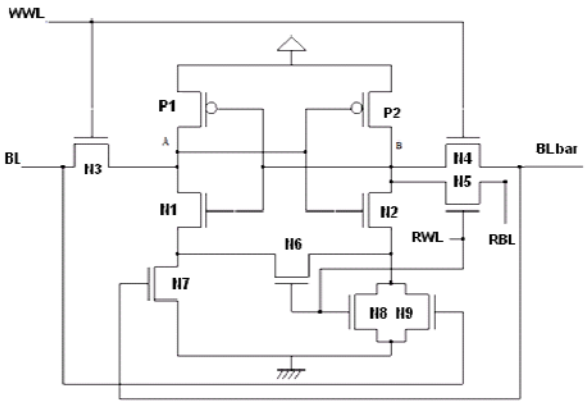

Figure 15. 11T- proposed SRAM Cell by Singh et al. [40]

During write operation, WWL is set to '1' and RWL is set to '0'. Write '1' and write '0' operations are performed by selecting proper values on bit line as well as bit bar line. The critical paths for these two write operations are shown in Fig 16. Assume want to write value 0. The BL = '0', N_9 turn 'OFF', Node B shift to '1' mean node A = '0'.Assume want to write value '1'. The BL = '1', N_7 turn 'OFF', A pushes to '1' which result '0' at not B, in these two operations, BL or BLbar is neither charging or discharging as in 6T cell, therefore, during write '0' and '1' operation a lot of power can save [17].

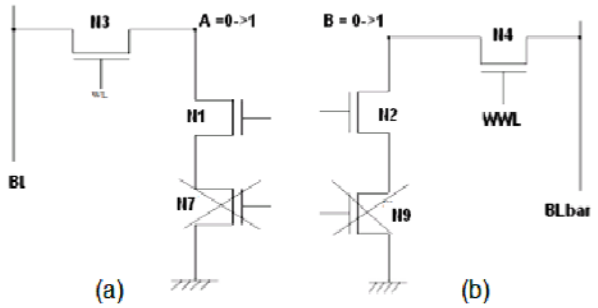

Figure 16. During Writing Operation a) 0 ->1, b) 1 -> 0

During read operation WWL = '0' and RWL = '1'. Transistor N_8 and N_6 is turn 'ON' depending upon the stored data at B, either read '0' or '1' operation can be performed. The critical path during read '1' operation is shown in Figure 17. Transistors N_9 and N_8 are in parallel and if both transistors have same size, it can decrease by half of the effective Rds-on. The circuit is call balanced 11T SRAM cell where both transistor N_8 and N_9 have same width size. In 11T SRAM cell, '0' to '1' or '1' to '0' transitions during read '0' operation are not allowed which means a lot of power is saved as no bit line is to discharge.

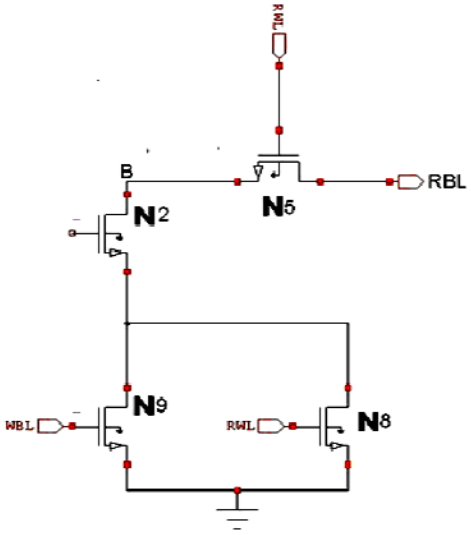

Figure 17. Critical Path during Read 1 Operation [40]

Singh et al. simulated the proposed 11T SRAM cell with tanner EDA tool and result is shown in Figure 18. The result is the comparison between proposed cell, ZA cell and conventional 6T cell. The result shows the proposed cell is decreased average power by 40% compare to conventional 6T cell.

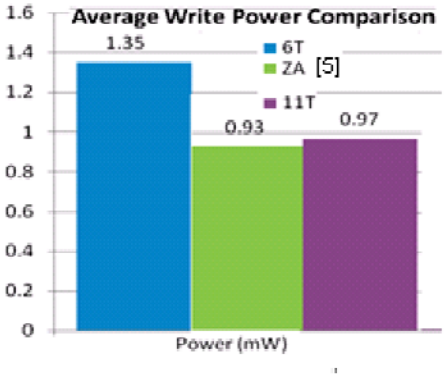

Figure 18. Power consumption

2.7. Optimized SRAM Cell Design

Kumar et al. proposed 9T SRAM cell to decrease the power consumption during the write operation. The schematic of proposed 9T SRAM cell is shown at Figure 19 [41].

This purposed SRAM have added one transistor N_7 between the pull down network of one the inverter and ground. The BL line has connected to the gate of transistor N_7. Another NMOS transistor N_6 has adder in the proposed SRAM cell between two inverters and the gate of transistor N_6 connected to read word line (RWL). The transistor N_6 can decrease effective resistance of the pull down network of inverter. The read operation of proposed SRAM cells it like conventional SRAM cell. Read operation is performed via access transistor RBL bar and N_5 [41].

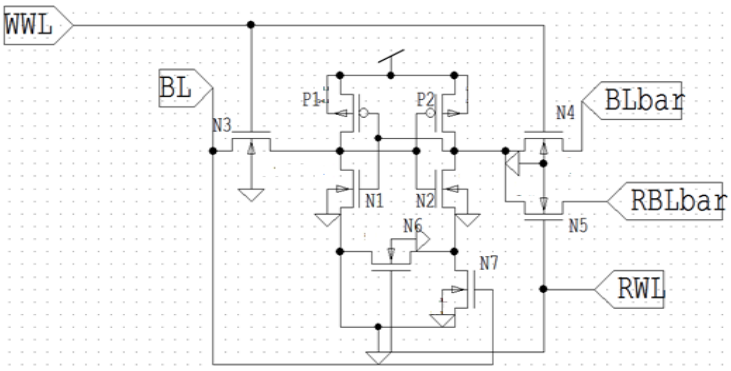

Figure 19. 9T SRAM Cell of Kumar et al.

Kumar et al. not explain detail how the circuit function during write and read operation. The result of simulation using Tanner tools-schematic editor(s-edit), t-spice and waveform editor (w-edit) is presented. The result of simulation is shown at Table 7 and Table 8. The power consumption during read '1'and write '1' operation is decrease around 89% and 67%. While, during read '0'and write '0' the power consumption increase by around 93% and 64% [41].

Table 7. Variation in Power Consumption during read 1 and read 0 [18]

(W/L)N 7	POWER(Mw) Read '0'	POWER(Mw) Read '1'
1	0.0412	0.1020
2	0.0409	0.0983
3	0.0408	0.0973
4	0.0407	0.0968

Table 8. Variation in Power Consumption during Write 1 and 0 Operation [41]

(W/L)N7	POWER (Mw) Write '0'	POWER (Mw) Write '1'
1	0.160	0.444
2	0.40	0.449
3	0.404	0.453
4	0.406	0.457

2.8. Controllable Voltage Level Circuit

Akashe et al. produced two new designs. First design has included load circuit is call 7T gated-ground SRAM. This design was put the transistor between pull down network circuit and ground. The function this transistor is during standby mode this transistor will cut of the circuit from ground to remove the leakage paths via the inverter NMOS source. The designs shows even in the absence of a ground path, the cell maintain its value during standby mode. The gate of transistor was connected to the WL [42-44].Second design is newly developed leakage current decreasing circuit is known a self-controllable Voltage Level (SVL). During the standby mode, this circuit can decrease leakage power [42].

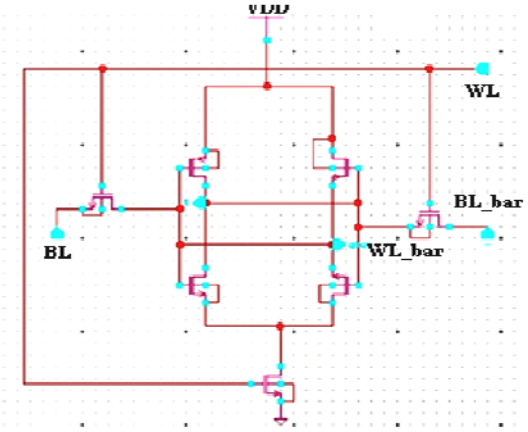

Figure 20. Schematic of 7T SRAM Cell by Akashe et al.

Assume want to write value '1' (storage node Q should '1' and QB '0'), first BL and BL_bar are charged and discharged. Transistors P_1 and P_2 turn on with set WL to low. WL will still at low voltage to keep transistor N_5turn 'OFF'. Transistor P_1 was charge up to 'HIGH' level node Q. Transistor P_2 was discharge 'LOW' level by BL_bar. WL set to 'HIGH' and transistors P_1 and $P_2$is turn 'OFF' when Q is charged sufficiently. Assume want to write value '0' (storage node Q should '0' and Q bar '1') first BL and BL_bar are discharged and charged. Even if write and read cycle come alternately, no additional power consumption was creating. It because there is no mismatch between the voltage level of bit lines in read cycle and that in write cycle [42].

Assume value at Q is '1' .Transistors P_1 and P_2 is turn 'OFF' with WL set to 'High'. WL will still at 'High' voltage to keep transistor N_5 on. BL is discharge through transistors N_3 and N_5. BL_bar is charge through transistor N_4.The storage nodes Q and Q bar complete decouple the datum from BL during a read operation. Assume value at Q is '0'. Transistors P_1, P_2 turn 'OFF' and transistor N_5 turn 'ON'. The BL bar is discharge via transistors N_4 and N_5.The read operation for the propose SRAM have different operation compare conventional 6T SRAM. Read and write path is separate in this proposed SRAM cell. The storage nodes should not be disturbed by reading datum. Besides, the voltage of the storage node, which store '0', is closely maintained at the ground level during a read operation, therefore, the 7T SRAM cell has higher endurance against external noise [42].

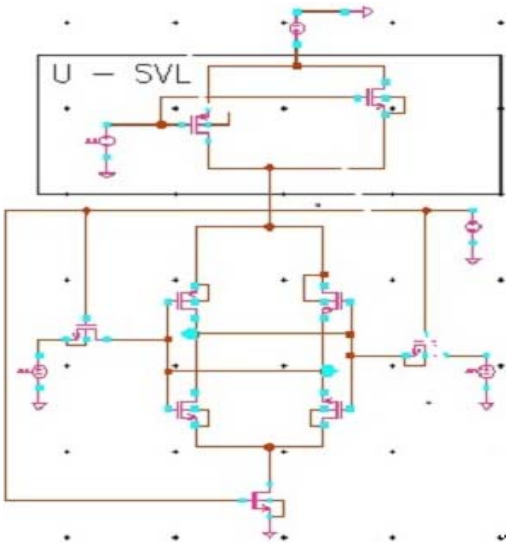

Figure 21. Schematic Diagram of USVL Based 7T SRAM Cell [19]

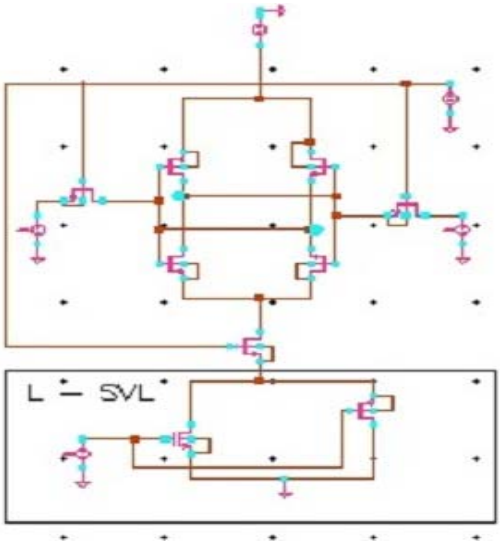

Figure 22. Schematic Diagram of LSVL Based 7T SRAM Cell [42]

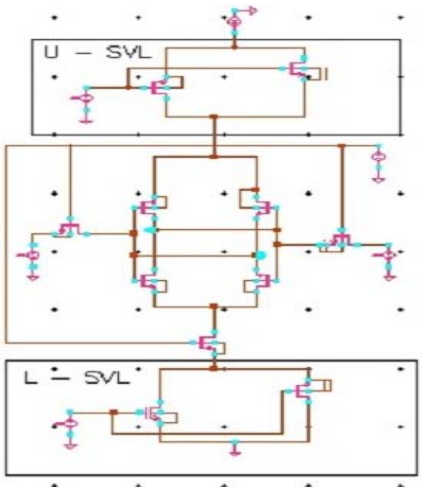

Figure 23. Schematic Diagram of SVL based 7T SRAM cell [42]

A self-controllable-voltage-level (SVL) circuit- which can supply a maximum DC voltage to an active-load circuit on request or can decrease the DC voltage supplied to a load circuit in standby mode was develop. This SVL circuit can minimal overheads in term of chip area and speed for reduce standby leakage power of CMOS logic circuit. When control signal goes to a high level, drain voltage increase to V_{DD} (0.7V), while source voltage decrease to ground (0V), so the SRAM becomes active. Three types of self-controllable voltage level (SVL) circuit area develop. Type 1 has an upper SVL circuit; this circuit has a single transistor PMOS and NMOS connected in series. Transistor PMOS is turn ON was connecting to V_{DD} and the load circuit in the active mode on request, and transistor NMOS is turn ON connect V_{DD} and the load circuit in standby mode. Type 2 has a lower SVL circuit. This circuit has PMOS and NMOS with connected between ground and the load circuit. This circuit supply VSS to the active load circuit through the NMOS on and VSS to the standby load circuit with the PMOS ON. Type 3 combines the upper and lower SVL circuits, which is shown in Table 9.

Table 9. Show the Operation Mode for SVL [42]

Mode	Upper SVL circuit	Lower SVL circuit
Active	PMOS switch is turned on VDD is supplied	NMOS switch is turned on Vss is supplied
Standby Mode	NMOS is turned on VD(<VDD) is supplied	PMOS is turned on Vs(>Vss) is supplied

Akashe et al. have simulated the proposed SRAM cell using cadence virtuoso tool. The parameters and result of proposed SRAM cell is shown in Table 10 and Table 11.

Table 10. Parameters of 7t SRAM Cell [42]

Process technology	45nm
Power supply voltage	0.7V
Pre-charge voltage	1V

Table 11. Simulation Result of SLV Based 7t SRAM [42]

Circuit (7T SRAM)	Leakage current(uA)
Write	1.347
Read	1.25
with USVL	1.155
with USVL	1.077
with SVL	0.04

3. Results and Discussion

The Power dissipation occurs during write, read and standby mode of operation. Various ways can be done to reduce power dissipation. Several factors need to be considered for the SRAM. Especially in terms of size and speed SRAM.

Table 12. Performance Comparison of Different SRAM Cells

	Conventional 6t SRAM Cell [36]	Single Bitline 6t SRAM Cell [25]	SRAM Cell For Portable Devices [26]	7T SRAM Cell [39]	Cache Design [40]	Symmetric and Balanced 11-T SRAM Cell [41]	Optimized SRAM Cell Design [42]
CMOS technology	0.18 um	0.9um	0.45um	0.18um	0.25um	0.18um	0.45um
Total number of transistor	6	8	7	7	11	9	7,9,11
Tool / software	not mentioned	Microwind 3.1 software	Cadence	HSPICE	Tanner	Tanner	cadence
Total reduction	Write 0 100% Total around 40% to 60 % Write 1 50% Read 0 33% Read 1 66%	500MHZ 38% Total around 12% to 38 % 1GHZ 19.83% 2GHZ 12.76%	45%	From 0 to 0 99.9% From 0 to 1 -1.4% From 1 to 0 96% From 1 to 1 -1.5%	Write 28% Read 33%	Write 65%	No comparison
Operation	Read and write	write	Read and write	write	Read and write	write	Read and write

Researchers to produce a good SRAM, including process fabrication, the addition of circuits and circuit modifications, have done various methods. Most researchers used a modification of the circuit to reduce power dissipation by adding a transistor to generate new SRAM. Therefore, the area of SRAM will be increasing.

Table 12 shows the number of categories of comparison between the new design SRAM cells. Use various tool scan to carry out the study. Symmetric and Balanced 11-T SRAM cell and optimized SRAM cell design has been using Tanner tool to simulate their proposed SRAM cell, while SRAM cell For portable devices and controllable voltage level circuit have used software Cadence. Each Single Bitline 6t SRAM Celland 7T SRAM Cell using Microwind 3 and HSPICE for simulate proposed SRAM cell.

The number of transistors is an important feature in determining width area of the SRAM cell. The less number of transistors used higher the probability to reduce the generality of SRAM cell. From Table 12 we can be concluding conventional 6t SRAM cell is a best-proposed SRAM in term of area category. It because proposed in conventional 6t SRAM cell only use six transistors it like conventional SRAM. SRAM cell for portable devices and 7T SRAM cell also can be considered a better SRAM because only have one extra transistor if compare with conventional 6T SRAM. Researchers have been using different CMOS technology in designing transistor while conducting the research. The software used during simulation may influence this difference.

The power consumption happen during at all condition, standby mode, read and write condition. This paper had studied four proposed SRAM cell will help reduce power consumption during write and read operation and three proposed SRAM, which only reduce power consumption during, write operation. Because researchers use different simulation tool and CMOS technology, so it is difficult to do conclusion, which the proposed SRAM cell has, better in reducing power dissipation. In case study 1 total reduction of power consumption is around 40% to 60 % during write and read condition [36]. While single bitline 6t SRAM cellonly help decrease power consumption during write operation by 12% to 38% [25]. The power can be save about 45% during read and write condition by use proposed SRAM in SRAM cell for portable devices. In 7T SRAM cell has to situation good and poor. Good situation happen during write pattern from ‘0’ to ‘0’ and ‘1’ to ‘0’. For this operation the power consumption reduce about 99.9% for pattern from ‘0’ to ‘0’ and by 96% for pattern ‘1’ to ‘0’. Poor situation has happen during pattern from ‘0’ to ‘1’ and ‘1’ to ‘0’. In this operation power consumption has increase about 1.4% and 1.5 % [39]. Power reduces by 28% during write operation and by 33% during read operation in Symmetric and Balanced 11-T SRAM Cell. About 65% of power consumption can be reduced by using RAM as proposed in the Optimized SRAM Cell.

Good modifications are modifications that affect a decrease of power dissipation in both operations (read and write). One of the best proposed SRAM is created by Majumdar and Basu in conventional 6t SRAM cell. The proposed SRAM is using only a single bit for charge and discharge during write and read operation and involve the same number of transistors with conventional SRAM. Therefore, in terms of size is not much different from the conventional SRAM, while the power dissipation can be reduced for write and read operation. This proposed SRAM also decrease a power consumption around 40% to 60% [35].

In addition, SRAM produced by Singh et al. in Symmetric and Balanced 11-T SRAM cell also better, although using many transistors and involve increased area but it can reduce power dissipation during write and read operation. Overall, forms this study, it can be concluded that in circuit modification to reduce power dissipation or consumption must be balanced with the area and speed operation.

4. Conclusion

In this paper, the advance of low power design SRAM has been studied in detail. This paper focused more about power dissipation. Future studies can be made in term of delay and speed operation in advance of low power design SRAM cell. Now in the world the system of memory becomes very important and integral part of all processors and programmable devices. The demand to create a new design to make sure power dissipation decrease is very required.

References

[1] Akter M, Reaz MBI, Mohd-Yasin F, Choong F. A modified-set partitioning in hierarchical trees algorithm for real-time image compression. *Journal of Communications Technology and Electronics.* 2008; 53(6): 642-650.

[2] Mogaki S, Kamada M, Yonekura T, Okamoto S, Ohtaki Y, Reaz MBI. *Time-stamp service makes real-time gaming cheat-free.* 6th ACM SIGCOMM workshop on Network and system support for games, ACM, Sep. 2007: 135-138.

[3] Mohd-Yasin F, Khaw MK, Reaz MBI. Radio frequency identification: Evolution of transponder circuit design. *Microwave journal.* 2006; 49(6): 56-70.

[4] Uddin J, Reaz MBI, Hasan MA, Nordin AN, Ibrahimy MI, Ali MAM. UHF RFID antenna architectures and applications. *Scientific Research and Essays.* 2010; 5(10):1033-1051.

[5] Uddin MJ, Ibrahimy MI, Reaz MBI, Nordin AN. Design and application of radio frequency identification systems. *European Journal of Scientific Research*. 2009; 33(3): 438-453.

[6] Choong F, Reaz MBL, Chin TC, Mohd-Yasin F. *Design and implementation of a data compression scheme: A partial matching approach.* Conference on Computer Graphics, Imaging and Visualisation: Techniques and Applications, Sydney, Australia. 2006: 150-155.

[7] Choong F, Reaz MBI, Mohd-Yasin F. *Power quality disturbance detection using artificial intelligence: A hardware approach.* 19th IEEE International Parallel and Distributed Processing Symposium (IPDPS 05). 2005: 146a.

[8] Reaz MBI, Mohd-Yasin F, Sulairnan MS, Tho KT, Yeow KH. *Hardware prototyping of boolean function classification schemes for lossless data compression.* 2nd IEEE International Conference on Computational Cybernetics, Vienna, Austria. 2004: 47-51.

[9] Reaz MBI, Sulaiman MS, Yasin FM, Leng TA. *IRIS recognition using neural network based on VHDL prototyping.* International Conference on Information and Communication Technologies: From Theory to Applications. 2004: 463-464.

[10] Pang WL, Reaz MBI, Ibrahimy MI, Low LC, Mohd-Yasin F, Rahim RA. Handwritten character recognition using fuzzy wavelet: A VHDL approach, *WSEAS Transactions on Systems.* 2006; 5: 1641-1647.

[11] Assim A, Reaz MBI, Ibrahimy MI, Ismail AF, Choong F, Mohd-Yasin F. An AI based self-moderated smart-home. *Informacije MIDEM.* 2006; 36: 91-94.

[12] Reaz MBI, Leong PW, Mohd-Yasin F, Chin TC. *Modeling of data compression using partial matching: A VHDL approach.* 6th World Wireless Congress, (WWC 2005), San Francisco Bay Area, USA, 2005: 411-416.

[13] Mamun IR, Lee WF, Hamid NH, Lo HH, Yeon A, Mohd S. High degree of testability using full scan chain and ATPG-An industrial perspective. *Journal of Applied Sciences.* 2009; 9(14): 2613-2618.

[14] Teh YK, Mohd-Yasin F, Choong F, Reaz MI, Kordesch AV. Design and analysis of UHF micropower CMOS DTMOST rectifiers. *IEEE Transactions on Circuits and Systems II: Express Briefs.* 2009; 56(2): 122-126.

[15] Mohd-Yasin F, Yap MT, Reaz MBI. CMOS instrumentation amplifier with offset cancellation circuitry for biomedical application. *WSEAS Transactions on Circuits and Systems.* 2007; 6(1): 171-174.

[16] Alam MR, Reaz MBI, Ali MAM. Statistical modeling of the resident's activity interval in smart homes. *Journal of Applied Sciences.* 2011; 11: 3058-3061.

[17] Rahman LF, Reaz MBI, Ali MAM, Marufuzzaman M, Alam MR. *Beyond the WiFi: Introducing RFID system using IPv6.* Proceedings of the ITU-T Kaleidoscope Conference, Pune, India. 2010: 1-4.

[18] Mohd-Yasin F, Khaw MK, Reaz MBI. Techniques of RFID systems: Architectures and applications. *Microwave Journal.* 2006; 49(7): 62-74.

[19] Yasin FM, Tye KF, Reaz MBI. *Design and implementation of interface circuitry for CMOS-based SAW gas sensors.* IEEE International SOC Conference, Herndon, VA. 2005: 161-164.

[20] Khaw MK, Mohd-Yasin F, Reaz ML. Recent advances in the integrated circuit design of RFID transponder. *IEEE International Conference on Semiconductor Electronics*. 2004: 326-330.

[21] Rahman LF, Reaz MBI, Mohd Ali MA, Kamada M. *Design of an EEPROM in RFID tag: Employing mapped EPC and IPv6 address.* IEEE Asia-Pacific Conference on Circuits and Systems, (APCCAS 2010), Kuala Lumpur, Malaysia. 2010: 168-171.

[22] Rahman LF, Reaz MBI, Ali MAM, Marufuzzaman M. Implementation of Sense Amplifier in 0.18 μm CMOS Process. *Electronics and Electrical Engineering.* 2012; 4(120): 113-116.

[23] Itoh BSK. Adaptive Circuit for the 0.5-V Nanoscale CMOS Era. *IEICE Transactions on Electronics.* 2010; E93-C(2): 216-233.

[24] Akashe S, Bhushan SI, Sharma S. *High Density and Low Leakage Current Based 5T SRAM Cell Using 45 nm Technology*. IEEE International Conference on Nanoscience, Engineering and Technology (ICONSET), Chennai. 2011: 346-350.

[25] Upadhyay P, Mehra MR, Thakur N. *Low Power Design of an SRAM Cell for Portable Devices.* International Conference on Computer & Communication Technology (ICCCT'10). 2009: 255-259.

[26] Jain A, Akashe S. *Optimization of Low Power 7T SRAM Cell in 45nm Technology*. 2ndInternational Conference on Advanced Computing & Communication Technologies. 2012: 324-327.

[27] Weste HEN, Harris. CMOS VLSI Design- A Circuits and Systems Perspective. *Addison Wesley*. 2004: 715-718.
[28] Rabaey JM, Chandrakasan A, Nikolic B. Digital Intergrated Circuits- A Design Perspective. *Pearson Education*, 2003:657-659.
[29] Yagain D, Parakh A, Kedia A, Gupta GK. *Design and implementation of High speed, Low area Multiported loadless 4T Memory cell*. Proceedings4thInternational Conference on Emerging Trends in Engineering & Technology. 2011: 268-273.
[30] Siwach A, Rishi R. Asymmetric SRAM – Power Dissipation and Delay. *IJCEM International Journal of Computational Engineering & Management*. 2011; 11: 28-31.
[31] Barnes. A 500MHz 64b RISC CPU with 1.5Mb On-Chip Cache. *IEEE International Solid State Circuits Conference, Digest of Technical Papers*. 1999: 86-87.
[32] Moshovos A, Falsafi B, Najm FN, Azizi N. A Case for Asymmetric-Cell Cache Memories. *IEEE Transaction on very large scale integration (VLSI) systems*. 2005; 13(7): 155-162.
[33] Heo S, Barr K, Hampton M, Asanovic K. *Dynamic fine-grain leakage reduction using leakage-biased bitline.* Proceedings 29th Annual International Symposium on Computer Architecture. 2002: 137–147.
[34] Rabaey JM, Chandrakasan A, Nikolic B. Digital Integrated Circuits: A Design Perspective, Prentice Hall series in electronics and VLSI, Prentice Hall, Second edition. 2003.
[35] Kang, Lebelebici. CMOS Digital Integrated Circuits: Analysis and Design. 2007.
[36] Majumdar B, Basu S. *Low Power Single Bitline 6T SRAM Cell with High Read Stability.* Proceedings International Conference on Recent Trends in Information Systems. 2009: 169-174.
[37] Weste NHE, Harris D, Banerjee A. CMOS VLSI Design, Pearson Education, Third Edition. 2006: 55-57.
[38] Chandrakasan A, Bowhill WJ, Fox F. Design of High-Performance Microprocessor Circuits. IEEE Press. 2000.
[39] Aly RE, Bayoumi MA. Low-Power Cache Design Using 7T SRAM Cell. *IEEE Transactions on Circuits and Systems Ii: Express Briefs.* 2007; 54(4): 318-322.
[40] Singh AK, Prabhu CMR, Pin SW, Hou TC. *A Proposed Symmetric and Balanced 11-T SRAM Cell for lower power consumption.* TENCON. 2009: 1-4.
[41] Imran AK, Khan A. *Optimized Sram Cell Design for High Speed and Low Power Applications.* Proceedings World Congress on Information and Communication Technologies. 2011: 1357-1362.
[42] Akashe S, Mishra M, Sharma S. *Self- controllable Voltage Level Circuit for Low Power, High Speed 7T SRAM cell at 45 nm Technology.* Proceedings 2012 Students Conference on Engineering and Systems (SCES), Allahabad, Uttar Pradesh. 2012:1 – 5.
[43] Marufuzzaman M, Abidin S, Reaz MBI, Rahman LF. Design of 3-Bit ADC in 0.18 µm CMOS Process. *TELKOMNIKA Indonesian Journal of Electrical Engineering.* 2014; 12(7): 5197-5203.
[44] Al A, Reaz M, Jalil J, Ali MAM. An Improved A Low Power CMOS TIQ Comparator Flash ADC. *TELKOMNIKA Indonesian Journal of Electrical Engineering.* 2014; 12(7): 5204-5210.