

Three-stage Amplifier Adopting Dual-miller with Nulling-resistor and Dual-feedforward Techniques

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Abstract

A high-gain wide-bandwidth three-stage amplifier, which employs dual-miller compensation with nulling-resistor and dual-feedforward compensation (DMCNR-DFC), is designed and analyzed in this paper. By adopting the technique of DMCNR-DFC, the designed three-stage amplifier achieves well performance including gain-bandwidth product (GBW) and slew rate (SR). The improved DMCNR-DFC three-stage amplifier is designed and simulated in 0.35 μ m BCD process. Simulation results show that DMCNR-DFC three-stage amplifier achieves a dc gain of about 121.1dB and GBW of about 6.1MHz with 52° phase margin using a 5-V power supply voltage.

Keywords: dual-miller compensation with nulling-resistor, dual-feedforward compensation, three-stage amplifier

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1. Introduction

The operational amplifier is a fundamental building block in the analog integrated systems and mixed-signal systems [1-4]. With the development of modern CMOS technology, the channel lengths and supply voltages of MOSFET transistors are scaling down, and conventional single-stage cascode amplifiers are not suitable for obtaining high dc gain and large output-swing simultaneously. In fact, the topology of three-stage amplifier is a good trade off between dc gain, bandwidth and power consumptions. However, three-stage amplifiers suffer from the close-loop stability problem because they have multiple-poles and zeros. Therefore, the frequency compensation technique should be analyzed and discussed to improve the stability of three-stage amplifier system.

In the recent past many years, many frequency compensation techniques of three-stage amplifiers have been reported [5-16]. For the architecture of three-stage amplifier, the nested Miller compensation (NMC), which can provide a well stability, is a well-known compensation technique [9]. However, the NMC three-stage amplifier suffers from enormous power consumption and gain-bandwidth limitation when the number of gain stages increases, and which has a right half plane (RHP) zero. Moreover, the gain-bandwidth production of NMC three-stage amplifier is only one quarter of that of a single-stage amplifier [10]. Based on NMC, many compensation topologies have been reported to improve the bandwidth and the stability of three-stage amplifier, such as nested Gm-C compensation (NGCC) [11], active feedback frequency compensation (AFFC) [12], dual active-capacitor active-feedback compensation (DACFC) [13], impedance adapting compensation (IAC) [14], cross feedforward cascade compensation (CFCC) [7], current buffer Miller compensation (CBMC) [6], AC boosting compensation (ACBC) [15], reverse nested Miller compensation (RNMC) [16], and single-Miller capacitor feedforward frequency compensation (SMFFC) [8], and so on. In general, these compensation techniques based on NMC achieve well performance. However, the frequency compensation technique must still be discussed and analyzed to further improve the performance of three-stage amplifier.

In this paper, a three-stage amplifier, which adopts dual-miller compensation with nulling-resistor and dual-feedforward compensation (DMCNR-DFC), is designed and analyzed.

Section 2 will discuss the conventional NMC three-stage amplifier. The improved DMCNR-DFC three-stage amplifier will be analyzed and designed in Section 3. Section 4 will give the simulation results of three-stage amplifier. Finally, conclusions are given in Section 5.

2. Analysis of Conventional NMC Three-stage Amplifier

Figure 1 shows the topology of NMC three-stage amplifier [10]. A_{v1} , A_{v2} and A_{v3} form the basic three-stage amplifier, and their transconductances are expressed by g_{m1} , g_{m2} and g_{m3} respectively. C_{m1} and C_{m2} are the compensation capacitor, and R_L and C_L are, respectively, load-resistor and load-capacitor. $r_{o(1,2)}$ and $C_{o(1,2)}$ are the equivalent output resistance and the lumped capacitance respectively. Figure 2 is the transistor-level circuit of NMC three-stage amplifier. The first-stage, second-stage and last-stage of NMC three-stage amplifier are made up of transistors $M_1\sim M_9$, $M_{10}\sim M_{13}$ and $M_{14}\sim M_{15}$ respectively.

As reported in [10], it is assumed that $g_{mi}r_{oi}\gg 1$, $C_{mi}\gg C_{oi}$, $C_L\gg C_{mi}$ and $g_{m3}R_L\gg 1$, here $i=1, 2$. Besides, with an additional condition that $g_{m3}\gg g_{m(1,2)}$, the open-loop small-signal transfer function of NMC three-stage amplifier, which is reported in reference [10], can be expressed as:

$$A_{vNMC}(s) = \frac{g_{m1}g_{m2}g_{m3}r_{o1}r_{o2}R_L \left(1 - \frac{C_{m2}}{g_{m3}}s - \frac{C_{m1}C_{m2}}{g_{m2}g_{m3}}s^2 \right)}{\left(1 + g_{m2}g_{m3}r_{o1}r_{o2}R_L C_{m1}s \right) \left[1 + s \frac{C_{m2}(g_{m3} - g_{m2})}{g_{m2}g_{m3}} + \frac{C_L C_{m2}}{g_{m2}g_{m3}}s^2 \right]} \quad (1)$$

As analyzed in reference [10], it is assumed that $C_{m1}=4(g_{m1}/g_{m3})C_L$ and $C_{m2}=2(g_{m2}/g_{m3})C_L$, and the gain-bandwidth product (GBW) of NMC three-stage amplifier can be given by:

$$GBW = \frac{1}{4} \left(\frac{g_{m3}}{C_L} \right) \quad (2)$$

Equation (1) and Equation (2) indicate that NMC three-stage amplifier has one-fourth GBW of single-stage amplifier and has a RHP zero. The RHP zero degrades the stability significantly. To further improve GBW and stability of three-stage amplifier, an improved topology of three-stage amplifier, which adopts dual-miller compensation with nulling-resistor and dual-feedforward compensation (DMCNR-DFC), is analyzed and designed in section 3.

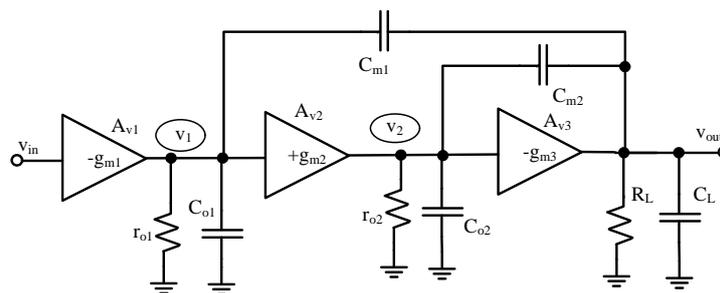


Figure 1. Topology of NMC Three-stage Amplifier

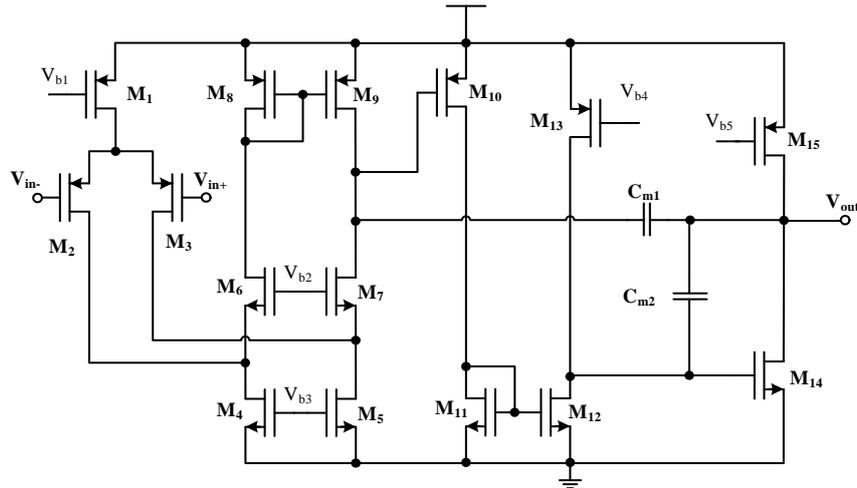


Figure 2. Transistor-level Circuit of NMC Three-stage Amplifier

3. Analysis and Design of Improved DMCNR-DFC Three-stage Amplifier

The topology of improved DMCNR-DFC three-stage amplifier, which adopts dual-miller compensation with nulling-resistor and dual-feedforward compensation, is shown in Figure 3. The dc gain of DMCNR-DFC three-stage amplifier is realized by cascading gain stages A_{v1} , A_{v2} and A_{v3} . A_{v1} is a high gain stage, A_{v2} is high-gain and wide-output-swing second-stage, and A_{v3} is the last stage with wide-output-swing. A_{va} and A_{vf} form, respectively, a feedforward stage. R_{m1} - C_{m1} and R_{m2} - C_{m2} form, respectively, miller compensation with nulling-resistor. A_{va} - A_{v2} and A_{vf} - A_{v3} form the push-pull second-stage and the push-pull output stage of three-stage amplifier respectively, so DMCNR-DFC three-stage amplifier has an improvement transient response.

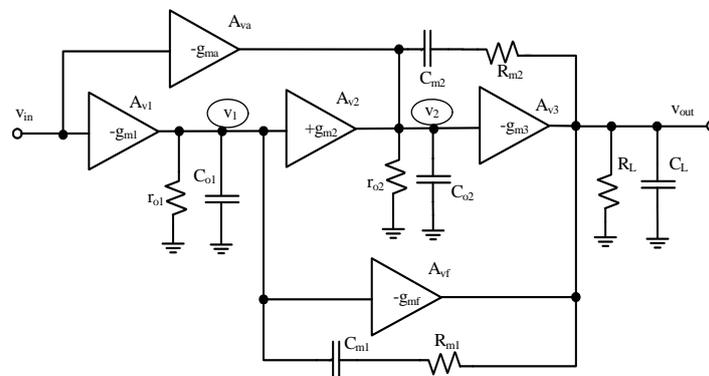


Figure 3. Topology of DMCNR-DFC Three-stage Amplifier

3.1 Transfer Function and Stability Analysis of DMCNR-DFC Three-stage Amplifier

As shown in Figure 3, g_{m1} , g_{m2} and g_{m3} are, respectively, the transconductances of the first-stage, second-stage and last-stage of DMCNR-DFC three-stage amplifier. $r_{o(1,2)}$ and $C_{o(1,2)}$ are the equivalent output resistances and lumped parasitic capacitance of gain stages respectively, and R_L and C_L are, respectively, the loading resistor and loading capacitor. g_{ma} and g_{mf} are the equivalent transconductances of feedforward stage A_{va} and A_{vf} respectively. To analyze the stability of DMCNR-DFC three-stage amplifier in this paper, the open-loop transfer function can be obtained by analyzing the equivalent small-signal topology as shown in Figure 3. At the same time, to simplify the transfer function without losing accuracy with the goal of

providing a clearer insight to the DMCNR-DFC three-stage amplifier, the following assumptions are reasonably made.

- (1) The loading capacitor C_L is much greater than the compensation capacitors $C_{m(1,2)}$, i.e. $C_L \gg C_{m(1,2)}$.
- (2) The compensation capacitors $C_{m(1,2)}$ and the loading capacitor C_L are much greater than the lumped output capacitors of each stage, i.e. $C_{m(1,2)}$ and $C_L \gg C_{o(1,2)}$.
- (3) The compensation capacitors $C_{m(1,2)}$ have equivalent capacitance, i.e. $C_{m1} = C_{m2}$.
- (4) The dc gains of all stage are much greater than 1, i.e. $g_{m1}r_{o1}$, $g_{m2}r_{o2}$ and $g_{m3}R_L \gg 1$.
- (5) The output resistance of all stage are much greater than resistors $R_{m(1,2)}$, i.e. $r_{o(1,2)}$ and $R_L \gg R_{m(1,2)}$.
- (6) To have a symmetrical push-pull output stage, the transconductances g_{m3} and g_{mf} are equal, i.e. $g_{m3} = g_{mf}$.

Based on those assumptions, the open-loop small-signal transfer function of DMCNR-DFC three-stage amplifier can be given as:

$$A_v(s) = \frac{A_{dc} \left(1 + \frac{s}{z_{LHP1}}\right) \left(1 + \frac{s}{z_{LHP2}}\right) \left(1 + \frac{s}{z_{LHP3}}\right)}{\left(1 + \frac{s}{p_{-3dB}}\right) \left(1 + \frac{s}{p_{nd1}}\right) \left(1 + \frac{s}{p_{nd2}}\right) \left(1 + \frac{s}{p_{nd3}}\right) \left(1 + \frac{s}{p_{nd4}}\right)} \quad (3)$$

$$A_{dc} = g_{m1}g_{m2}g_{m3}r_{o1}r_{o2}R_L \quad (4)$$

$$z_{LHP1} = \frac{1}{C_{m2} \left[(R_{m2} + R_{m1}) - 1/g_{m3} \right]} \quad (5)$$

$$z_{LHP2} = \frac{g_{m3} (R_{m2} + R_{m1}) - 1}{R_{m1}C_{m1} (g_{m3}R_{m2} - 1)} \quad (6)$$

$$z_{LHP3} \approx \frac{g_{m1}g_{m2} (R_{m2} - 1/g_{m3})}{R_{m2} (g_{m2}C_{o1} + g_{m1}C_{o2})} \quad (7)$$

$$p_{-3dB} = \frac{1}{g_{m2}g_{m3}r_{o2}r_{o1}R_L C_{m1}} \quad (8)$$

$$p_{nd1} = \frac{1}{R_{m2}C_{m2}} \quad (9)$$

$$p_{nd2} = \frac{g_{m2}R_{m2}}{(R_{m2}C_{o2} + R_{m1}C_{o1})} \quad (10)$$

$$p_{nd3} = \frac{g_{m3}}{C_L} \quad (11)$$

$$p_{nd4} = \frac{1}{(R_{m1}C_{o1}) // (R_{m2}C_{o2})} \quad (12)$$

$$GBW = A_{dc} \times p_{-3dB} = \frac{g_{m1}}{C_{m1}} \quad (13)$$

In this topology as shown in Figure 3, $R_{m1} \gg 1/g_{m3}$, so it is concluded that $z_{LHP1} < p_{nd1}$. The zero z_{LHP1} can cancel the pole p_{nd1} . R_{m1} and R_{m2} are in an order of magnitude, and $C_{o(1,2)}$ and $C_{m(1,2)}$ are the lumped capacitance and compensation capacitance respectively. Based on the above assumption, the relation of zero z_{LHP2} and pole p_{nd2} can be obtained as:

$$z_{LHP2} = \frac{g_{m3}(R_{m2} + R_{m1}) - 1}{R_{m1}C_{m1}(g_{m3}R_{m2} - 1)} < p_{nd2} = \frac{g_{m2}R_{m2}}{(R_{m2}C_{o2} + R_{m1}C_{o1})} \quad (14)$$

Equation (14) shows that the zero z_{LHP2} can cancel the pole p_{nd2} . At the same time, $C_{o(1,2)}$ are the lumped capacitance, so the zero z_{LHP3} and the pole p_{nd4} can be pushed to a frequency that are higher than the unity-gain frequency (UGF). So, Equation (3) can be approximated as:

$$A_v(s) \approx \frac{A_{dc}}{\left(1 + \frac{s}{p_{-3dB}}\right) \left(1 + \frac{s}{p_{nd3}}\right)} \quad (15)$$

Equation (15) indicates that DMCNR-DFC three-stage amplifier is approximated to a system with two poles. Therefore, phase margin (PM) of DMCNR-DFC three-stage amplifier can be approximately written as:

$$PM \approx 90 - \arctan \frac{GBW}{p_{nd3}} \quad (16)$$

To ensure the stability of a unity-gain feedback system, three-stage amplifier should have a phase margin of at least 45° and 60° preferable in most situations. Therefore, pole p_{nd3} should be larger than GBW, and GBW of DMCNR-DFC three-stage amplifier can be written as:

$$GBW = \frac{g_{m1}}{C_{m1}} \leq p_{nd3} = \frac{g_{m3}}{C_L} \quad (17)$$

According to the above analysis, by adopting the DMCNR-DFC technique, the designed DMCNR-DFC three-stage amplifier achieves wider GBW than the conventional NMC three-stage amplifier for a given load capacitance C_L .

3.2. Transistor-level Circuit of DMCNR-DFC Three-stage Amplifier

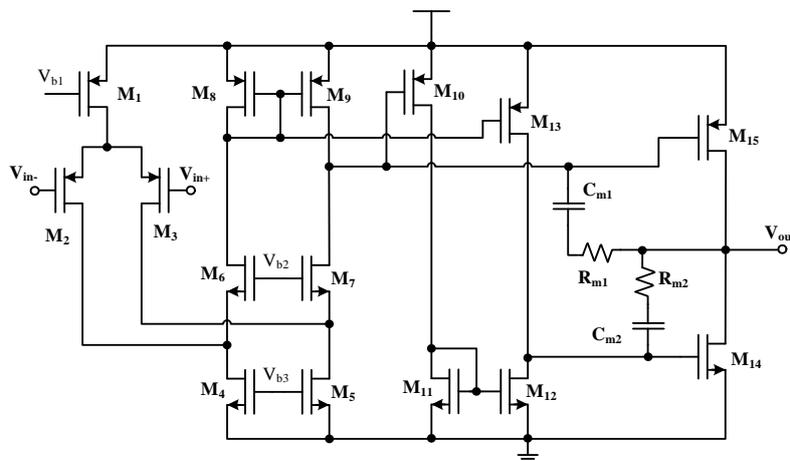


Figure 4. Transistor-level Circuit of DMCNR-DFC Three-stage Amplifier

The transistor-level circuit of DMCNR-DFC three-stage amplifier is shown in Figure 4. Transistors $M_1 \sim M_9$ form the first gain stage A_{V1} , and transistors $M_{10} \sim M_{13}$ form the second gain stage A_{V2} . A_{V3} is made up of transistor M_{14} . M_{15} forms the feedforward stage A_{Vf} , and A_{V3} and A_{Vf} form the push-pull output-stage. Feedforward stage A_{Va} is made up of transistors $M_1 \sim M_9$ and transistor M_{13} . At the same time, A_{Va} and A_{V3} form the push-pull stage at the output of the second gain stage A_{V2} . Those two push-pull output stages can effectively improve the slew-rate of DMCNR-DFC three-stage amplifier. $R_{m1} \sim C_{m1}$ and $R_{m2} \sim C_{m2}$ form the compensation network respectively.

4. Simulation Results

To verify the circuit of DMCNR-DFC three-stage amplifier shown in Figure 4, NMC and DMCNR-DFC three-stage amplifier are both designed and simulated in $0.35\mu\text{m}$ BCD technology with a 5-V power supply voltage.

The simulated open-loop frequency response of NMC three-stage amplifier and DMCNR-DFC three-stage amplifier are, respectively, shown in Figure 5 and Figure 6 under 100-pF load capacitor and 25-k Ω load resistor. The NMC three-stage amplifier achieves the dc gain of 121.2dB, phase margin of 54.4° and GBW of about 1.84MHz, but DMCNR-DFC three-stage amplifier achieves the dc gain of 121.2dB, phase margin of 52° and GBW of about 6.1MHz. Simulation results show that DMCNR-DFC three-stage amplifier achieves wider GBW than NMC three-stage amplifier.

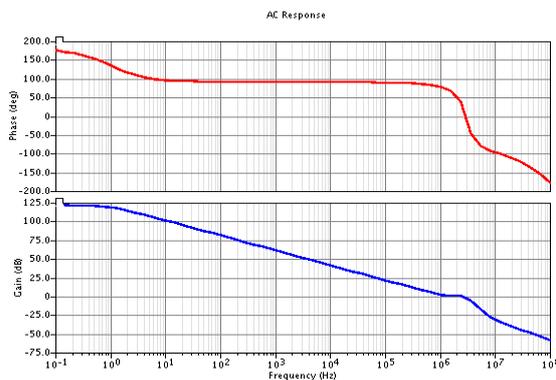


Figure 5. Open-loop Frequency Response of NMC Three-stage Amplifier

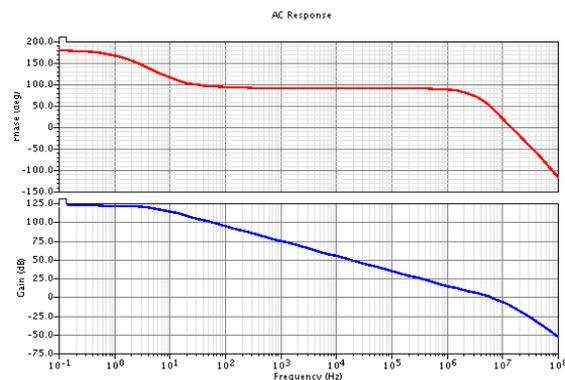


Figure 6. Open-loop Frequency Response of DMCNR-DFC Three-stage Amplifier

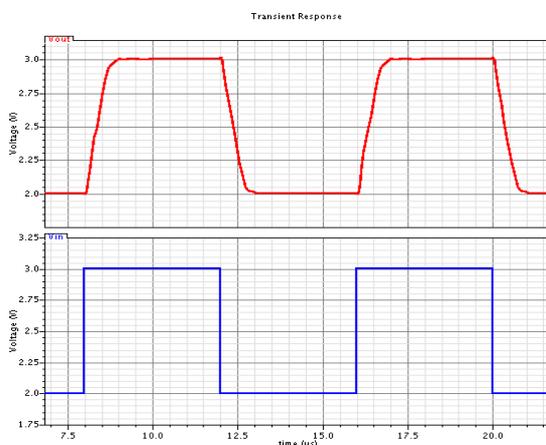


Figure 7. Transient response of NMC three-stage amplifier

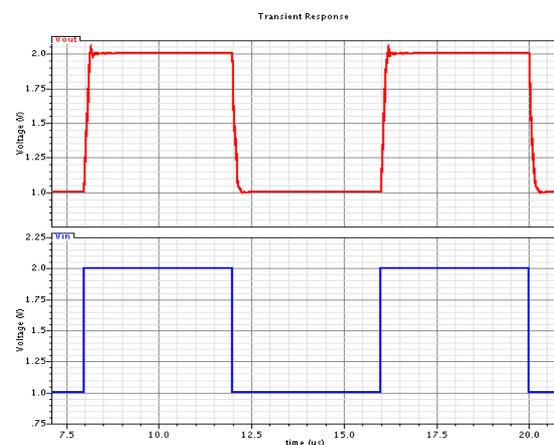


Figure 8. Transient response of DMCNR-DFC three-stage amplifier

Figure 7 and Figure 8 show, respectively, the simulated transient response of NMC three-stage amplifier and DMCNR-DFC three-stage amplifier in a unity-gain negative feedback configuration to a 125-kHz 1-V_{pp} pulsing input signal. NMC three-stage amplifier achieves positive slew rate (SR⁺) of 1.43 V/ μ s and negative slew rate (SR⁻) of 1.39 V/ μ s. And DMCNR-DFC three-stage amplifier achieves SR⁺ of 6.3V/ μ s and SR⁻ of 6.32V/ μ s. Simulation results show that DMCNR-DFC three-stage amplifier achieves well SR than NMC three-stage amplifier. Finally, performance summary of NMC three-stage amplifier and DMCNR-DFC three-stage amplifier are given in Table 1. From Table 1, the DMCNR-DFC three-stage amplifier achieves a well performance.

Table 1. Performance Summary of Three-stage Amplifier

	Ref. [8]	Ref. [14]	NMC three-stage amplifier in this paper	DMCNR-DFC three-stage amplifier in this paper
Process	0.18 μ m CMOS	0.35 μ m CMOS	0.35 μ m BCD	0.35 μ m BCD
Supply voltage (V)	1.5	1.5	5	5
Loading Capacitive (pF)	250	150	100	100
I _{dd} (mA)	0.023	0.02	0.2	0.2
A _{dc} (dB)	~100	110	121.2	121.2
GBW (MHz)	4.4	4.4	1.84	6.1
Phase margin	73°	57°	54.4°	52°
Average SR (V/ μ s)	1.8	1.8	1.41	6.31

5. Conclusion

A DMCNR-DFC three-stage amplifier, which adopts dual-miller compensation with nulling-resistor and dual-feedforward technique, has been designed and analyzed in this paper. By adopting the dual-miller compensation with nulling-resistor and dual-feedforward technique, the RHP zero can be removed, and the designed DMCNR-DFC three-stage amplifier achieves wider GBW and well SR than NMC three-stage amplifier. Simulation results show that DMCNR-DFC three-stage amplifier achieves well small-signal and large-signal performances.

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