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A Study of Three-Level Neutral Point Clamped Inverter Topology

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Abstract

The three-level Neutral Point Clamped (NPC) inverter has become matured and widely used topology in high-power medium-voltage applications due to several advantages associated with it as compared to other available multilevel topologies. This paper presents a brief review on operation of three-level NPC inverter. Different modulation strategies used in NPC inverter is also discussed. The problem of neutral point voltage balancing with its solution is presented. Finally, the simulation and experimental results for three-level NPC inverter are given which validates the proper operation of this topology.

***Keywords**: NPC, PWM, SVM, NP balance*

1. Introduction

The importance of renewable energy has increased due to reduction of available fossil fuel reserves and their negative impact on environment. Besides, because of expanding economies and population, the demand of energy has been increasing gradually. For efficient and reliable integration of renewable energy systems into distribution grid as well as to drive the required high power, new converter topologies and semiconductor technologies has emerged. For this reason, multilevel inverter have been introduced as they can achieve high power using medium-power semiconductor technology as compared to conventional inverter using high power semiconductor devices, which are still under development [1, 2].

The idea of multilevel inverter was introduced in 1975 and in 1981, A. Nabae, I. Takahashi, and H. Akagi presented the first three level inverter [3, 4]. In order to achieve high power, multilevel inverter used an array of semiconductor devices with several lower dc voltage sources for power conversion resulting in stepped voltage waveform. The dc voltage sources can be capacitors, batteries or renewable energy voltage sources. The commutation of the switches sum up these dc voltage sources to get higher output voltage. The voltage of power semiconductor switches endure only reduced voltages as the rating of power semiconductor switches is dependent on dc voltage source to which they are connected.

There are two types of inverter, the two level and multilevel. A Two level inverter generates an output voltage with two levels while the minimum numbers of voltage levels in multilevel inverter are three. The increase in number of levels of the inverter will have a good output voltage waveform with reduced harmonic distortion but with increase in control complexity. A multilevel inverter has great advantages compared to two level inverter mentioned as below:

a) The output waveforms contain very low total harmonic distortion (THD) and lower dv/dt.
b) Multilevel inverter can draw input current with very little distortion.
c) They can operate at both high switching frequency as well as low switching frequency.

With several advantages multilevel inverters do have some disadvantages. As with the increase of voltage level the number of power semiconductor switches also increased so overall system becomes more expensive and complex. Despite the advantages of multilevel converters their prevalence in industrial application is low due to technological problem such as reliability, efficiency, control complexity and modulation methods. However, the recent researches on

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these technical difficulties have resulted multilevel converter being accepted for various power system application.

A lot of inverter topologies have been proposed over the last two decades in which three are basic and most of the other topologies are hybrid circuits of two of the basic multilevel topologies with or without slight variations. The three basic topologies are diode-clamped (neutral-clamped), capacitor-clamped (flying capacitors) and cascaded H-bridge with separates dc sources [1, 2]. The NPC multilevel inverter is widely used in various industrial applications among other multilevel inverter topology. This paper presents a brief review on three-level NPC inverter topology and its modulation strategies. The major issue of this inverter topology is neutral point voltage unbalance which is addressed along with the solution. Finally the simulation and experimental are presented to validate the discussions.

2. Review of Topology

The three level neutral point clamped inverter is shown in the Figure 1. This inverter is the modified form of two-level inverter topology with the addition of two new semiconductor switches per phase. The two capacitor C1 and C2 split the dc bus voltage which make the neutral point 'P' that generate an additional voltage level hence making it three-level inverter. The clamping diode limits the voltage stress across the switches to the value of the voltage across the capacitor that is Udc/2. Table 1 shows the switching states for three-level inverter. The inverter output is Udc/2 when switch S1 and S2 are on while output –Udc/2 when switch S3 and S4 are switched on. The inverter generates switching state 0 when S2 and S3 are on.

NPC offers many advantages like the capacitance requirement in this topology is reduced as all phases share common dc bus; hence back to back topology is suitable for practical uses just like for multidrive and high voltage back to back interconnections [2, 4]. Further, capacitors can be charged prior treating them as group. However, NPC has some disadvantages too, the number of clamping diode increase with the increase in number of levels which can be unmanageable. The reverse recovery of these clamping diode presents a major design challenge when the inverter is operating under PWM in high voltage high power application [2, 5].

The NPC inverter is the widely used inverter topology for various industrial applications [1, 6]. Application of NPC includes high power medium voltage variable speed drive, static var compensator and interface between dc transmission line and ac transmission line. The back to back configuration of NPC make it suitable for regenerative application like conveyers for mining industry and interfacing of renewable energy system with the grid [7, 8].

Table 1. Three-level Inverter Switching States

Switching State	Device Switching Status (Phase A) S1	S2	S3	S4	Inverter Terminal Voltage
1	On	On	Off	Off	Udc/2
0	Off	On	On	Off	0
-1	Off	Off	On	On	- Udc/2

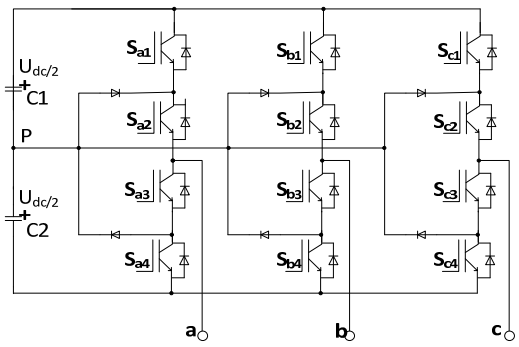

Figure 1. Three-Level NPC Inverter Topology

3. Modulation Strategies used in NPC Inverter

Several modulation techniques and control strategies have been proposed and implemented for multilevel inverters such as multilevel Multicarrier pulse width modulation (PWM), multilevel selective harmonic elimination, and space-vector modulation (SVM).

3.1. Multicarrier PWM Strategies

Sinusoidal PWM is very popular method in industrial application in which a sinusoidal reference signal is compared with two carriers Vtr1 and Vtr2 as shown in the Figure 2. In three-level NPC inverter switch S1 and S3 are complementary and switch S2 and S4 are complementary. In the figure, PWM signals are represented by PWM1 and PWM2. PWM1 signal is to drive S1 and S3 while PWM2 signal is to drive S2 and S4. When the reference wave is greater than zero, switch S1 and S3 turn on one time in every control period while switch S2 and S4 do not change their states and remain at 1 and 0 respectively. When the reference wave is less than zero, switch S2 and S4 turn on one time in every control period while switch S1 and S3 keep themselves at 0 and 1 respectively as shown in the Figure 2.

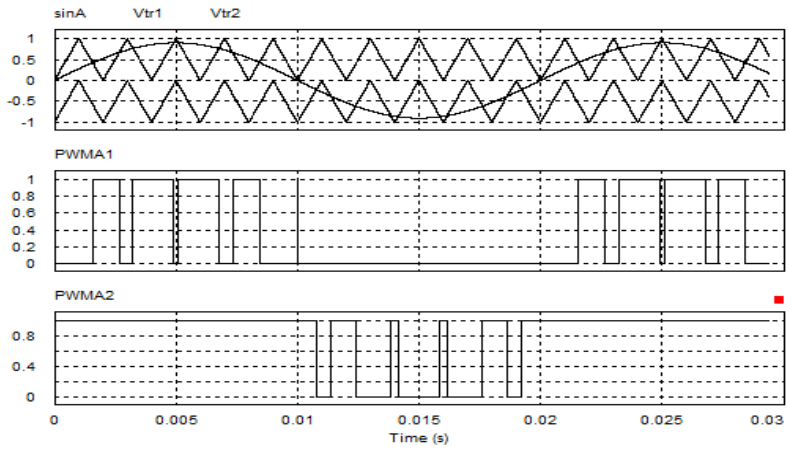

Figure 2. Multicarrier Modulation Strategy for Three-Level Inverter

3.2. Space Vector Modulation Stretegy

SVM is one of the widely used modulation strategy for voltage source inverter.SVM offers higher magnitude of fundamental component as compared to SPWM. However, for three level inverter the algorithm of SVM becomes complex because of larger number of switching states. For three-level inverter, the number of switching states is 3^3=27 as indicated in the table II. Space vector diagram is shown in Figure 3 has six sectors and each sector has four regions. From table II, it can be seen that small vectors have redundant switching states which can be used for capacitor voltage balancing.

The space vector PWM in three-level inverter can be realized into three steps. In Step 1, sector is determined as follows,

$$\begin{bmatrix} U_d \\ U_q \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} U_{an} \\ U_{bn} \\ U_{cn} \end{bmatrix} \quad (1)$$

$$\left|U_{ref}\right| = \sqrt{{U_d}^2 + {U_q}^2} \quad (2)$$

$$\theta = \tan^{-1}\left(\frac{U_q}{U_d}\right) = \omega_s t = 2\pi f_s t \quad (3)$$

Here fs is the fundamental frequency, θ will give the sector. Once sector is found out, region can be determined by doing simple mathematics as mentioned in [9].

Step 2 includes the determination of time duration for each voltage vector. The reference voltage vector in two-level PWM is approximated by choosing two adjacent vectors and zero vector but in multilevel PWM, reference voltage is usually tracked by selecting nearest three triangular vertices in order to minimize the harmonic in output line to line voltage [19]. Suppose the reference voltage is located in region 2 of sector 1, then the time duration required for each voltage vector is solved by using following calculations,

$$U_1 T_a + U_7 T_b + U_2 T_c = U_{ref} T_s \quad (4)$$
$$T_a + T_b + T_c = T_s$$

T_a, T_b and T_c is time duration for U_1, U_7 and U_2 respectively. U_{ref} is the reference voltage and T_s is the sampling or modulation period. Voltage vectors U_1, U_2 and U_7 determine the triangle region in which U_{ref} is located. In final step, the switching time for each transistor is determined. The sequence of changes in space vectors in each switching scheme is usually organized in such a way that only one leg is affected in each step [10].

Table 2. Space Vector and Switching States of Three-level Inverter

Space Vector		Switching State		Vector Classification	Vector Magnitude
V_0		[1 1 1] [0 0 0] [-1 -1 -1]		Zero Vector	0
		P-Type	N-Type		
V_1	V_{1p}	[1 0 0]			
	V_{1n}		[0 -1 -1]		
V_2	V_{2p}	[1 1 0]			
	V_{2n}		[0 0 -1]		
V_3	V_{3p}	[0 1 0]			
	V_{3n}		[-1 0 -1]	Small Vector	$1/3U_{dc}$
V_4	V_{4p}	[0 1 1]			
	V_{4n}		[-1 0 0]		
V_5	V_{5p}	[0 0 1]			
	V_{5n}		[-1 -1 0]		
V_6	V_{6p}	[1 0 1]			
	V_{6n}		[0 -1 0]		
V_7		[1 0 -1]			
V_8		[0 1 -1]			
V_9		[-1 1 0]		Medium Vector	$\sqrt{3}/3U_{dc}$
V_{10}		[-1 0 1]			
V_{11}		[0 -1 1]			
V_{12}		[1 -1 0]			
V_{13}		[1 -1 -1]			
V_{14}		[1 1 -1]			
V_{15}		[-1 1 -1]		Large Vector	$2/3U_{dc}$
V_{16}		[-1 1 1]			
V_{17}		[-1 -1 1]			
V_{18}		[1 -1 1]			

3.3. Selective Harmonic Elimination (SHE) Strategy

SHE offers appreciable reduction in the switching losses because the equipment has to be operated at low switching frequency to minimize semiconductor losses hence has been extended to multilevel inverter for high power applications. In SHE, generally, low frequency harmonics are removed by selecting proper switching angles among different level inverters while additional filter is used to eradicate higher frequency harmonic components.

The heavy computational process is the main drawback of SHE method so the design and implementation of SHE based method in inverters with higher number of levels becomes even more complex due to increase in switching angle.

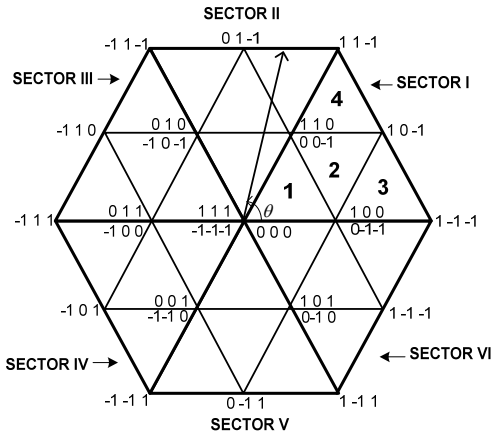

Figure 3. Space Vector Diagram of Three-Level Inverter

4. Neutral Point Voltage Balance of NPC Inverter

Though NPC Inverter provide attractive performance results for high power applications, the complex circuit structure and complicated operation brings various issues with it which has to be addressed. In the case of NPC inverter, Neutral point (NP) voltage imbalance is an important issue. Capacitor unbalance occurs in NPC due to different operating conditions based on modulation index [11], dynamic behavior and load conditions etc and results in voltage difference between the capacitors causing shift in neutral point [12]. If the neutral point voltage is not balanced, it will cause some serious damage to switching device. In addition, due to unbalance of neutral point voltage, low frequency ripple at neutral point potential appears which results in low frequency harmonics in output voltage hence increase in the THD of output current [11]. So the neutral point voltage should be properly balanced. The deviation in dc link voltage can be caused by the following reasons [13],

a) Inaccuracies occur during manufacturing process cause unbalance of dc capacitors.
b) Unbalanced three phase operation caused by change in operating grid conditions and external disturbances
c) Switching device characteristics are not consistent.
d) The disharmony brought about by action time of small voltage vectors effect neutral point potential deviation.

The voltage vectors shown in the Table 2 consists of zero, small, medium and large vector. Not all the vectors affect the neutral point potential. The zero and large vector do not affect neutral point balance because they do not connect any phase to neutral point. Medium vectors connect one of the phases to neutral point so they affect the neutral point voltage. Small vectors come in pair and affect NP voltage by connecting one or two phase to neutral point and NP voltage rise or drop depending upon the direction of NP current. Medium vectors cannot be controlled however the redundant switching states of small vector are used to balance the neutral point voltage. Table III shows the list of vectors which affect NP potential. As it is complicated to solve this issue directly, various algorithms have been introduced to balance neutral point voltage for carrier based modulation as well as for space vector modulation.
The three-level NPC inverter switching state can be expressed as:

$$V_{ss} = \left[S_a, S_b, S_c\right]^T$$

Where $S_x \in [-1, 0, 1], x \in [a, b, c]$

When one of the phases of bridge is connected with the neutral point (Sx=0), at that time, the load current will flow into or out of the neutral point through the clamp diodes. Therefore, the neutral current can be expressed as:

$$i_{neu} = (1-|S_a|)i_a + (1-|S_b|)i_b + (1-|S_c|)i_c \quad (5)$$

$$i_{neu} = -|S_a|i_a - |S_b|)i_b - |S_c|i_c \quad (6)$$

The three-phase positive-sequence modulation voltages are given by:

$$\begin{cases} e_a = M\cos(\omega t) \\ e_b = M\cos(\omega t - \frac{2\pi}{3}) \\ e_c = M\cos(\omega t + \frac{2\pi}{3}) \end{cases} \quad (7)$$

Where M is the modulation index. In neutral point voltage control based on zero sequence voltage injection method, the zero-sequence voltage U_0 is superimposed on the reference voltages. So the actual three-phase reference voltages after zero sequence voltage injection are given by:

$$\begin{cases} U_a = e_a + U_0 \\ U_b = e_b + U_0 \\ U_c = e_c + U_0 \end{cases} \quad (8)$$

Here we define the sign function as followed:

$$\mathrm{sgn}(v) = \begin{cases} 1 & v \geq 0 \\ -1 & v < 0 \end{cases} \quad (9)$$

Substituting (8) and (9) into (6), the neutral point current is given by:

$$\begin{aligned} i_{neu} &= -[\mathrm{sgn}(e_a).e_a.i_a + \mathrm{sgn}(e_b).e_b.i_b + \mathrm{sgn}(e_c).e_c.i_c] \\ &-U_0[\mathrm{sgn}(e_a).i_a + \mathrm{sgn}(e_b).i_b + \mathrm{sgn}(e_c).i_c] \end{aligned} \quad (10)$$

By adjusting the amount of neutral current the neutral point voltage can be controlled. To simplify the analysis, we can divide the positive-sequence modulation waveform into six sections, as given in Figure 4.

Table 3. Three-level Inverter Switching States

Positive Small Vectors	i_{NP}	Nagitive Small Vectors	i_{NP}	Medium Vectors	i_{NP}
[0 -1 -1]	i_a	[1 0 0]	$-i_a$	[1 0 -1]	i_b
[1 1 0]	i_c	[0 0 -1]	$-i_c$	[0 1 -1]	i_a
[-1 0 -1]	i_b	[0 1 0]	$-i_b$	[-1 1 0]	i_c
[0 1 1]	i_a	[-1 0 0]	$-i_a$	[-1 0 1]	i_b
[-1 -1 0]	i_c	[0 0 1]	$-i_c$	[0 -1 1]	i_a
[1 0 1]	i_b	[0 -1 0]	$-i_b$	[1 -1 0]	i_c

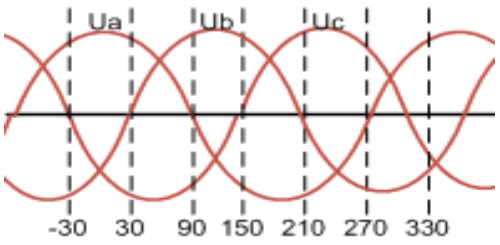

Figure 4. Six Section of Modulation Voltage

From Figure 4 it can be seen that only one phase has the maximum absolute amplitude in each interval. For example, in interval [-30°, 30°] phase A has the largest absolute amplitude while in [150°, 210°] phase C has largest amplitude. So in each interval there is specific phase current that affect neutral point potential. Besides, Table IV shows there is particular set of small vector in each interval that causes neutral point voltage balancing problem.

Based on multicarrier modulation strategy, by using current direction and two DC bus capacitor voltage difference, the appropriate zero-sequence component can be calculated. The zero-sequence voltage injected into modulating voltage can change the action time of redundant small vectors and so achieve the purpose of NP balancing control [14].

Table 4. Three-level Inverter Switching States

Interval	P type Small Vector	i_{neu}	N type Small Vector	i_{neu}
$-30^{\circ} \le \theta < 30^{\circ}$	[1 0 0]	$-i_a$	[0 -1 -1]	i_a
$30^{\circ} \le \theta < 90^{\circ}$	[1 1 0]	i_c	[0 0 -1]	$-i_c$
$90^{\circ} \le \theta < 150^{\circ}$	[0 1 0]	$-i_b$	[-1 0 -1]	$-i_b$
$150^{\circ} \le \theta < 210^{\circ}$	[0 1 1]	i_a	[-1 0 0]	$-i_a$
$210^{\circ} \le \theta < 270^{\circ}$	[0 0 1]	$-i_c$	[-1 -1 0]	i_c
$270^{\circ} \le \theta < 330^{\circ}$	[1 0 1]	i_b	[0 -1 0]	$-i_b$

Generally, the addition of zero sequence voltage change the dwell time of small vectors. The addition of positive zero sequence voltage increase the action time of P type small vector while the action time of N type small vector increases with addition of negative zero sequence voltage. For example in section $-30^{\circ} \le \theta < 30^{\circ}$, if the neutral point voltage is greater than zero and the direction of current is into the neutral point then neutral point voltage can be decreased by injecting positive zero sequence voltage. If the neutral point voltage is less than zero and direction of current is into the neutral point then it can be increased by adding negative zero sequence voltage. But the addition of zero sequence must ensure the constraint give below:

$$\left| e_a + U_0 \right| < M$$

Zero sequence voltage injection method can be can be divided into following step:

a) Conversion of three phase modulating wave e_a, e_b, e_c to $\alpha\beta$ plane.
b) Find out rotating angle θ through U_α, U_β
c) Determine sections by using θ
d) Depending upon neutral point voltage and direction of phase current add the zero sequence voltage. Also make sure addition of zero sequence voltage must follow the modulation constraint.
e) Now put three-phase modulation wave into PWM modulation module to generate PWM signal to drive IGBTs.

Several other carrier based PWM technique also have been proposed to balance neutral point voltage [15, 16].

In space vector, the redundant switching states of small vectors are used to balance NP voltage. Therefore, most of the NP voltages balancing strategy used in SVM are based on some modification of small vectors. To eliminate the error in NP the relative duration of positive and negative small vectors in a pair are changed just like in [17]. In this paper, the NP voltage balancing is achieved by adjusting dwell time of positive and negative voltage vectors by adding a time offset at the turn on of the switch. A simple method is given for the calculation of proper time offset. In order to reduce NP voltage deviation, many other advanced strategies based on SVM have been proposed [17, 18].

In carrier-based PWM, it has been seen that all the neutral point voltage balance techniques use some form of the manipulation of zero sequence voltage ,while in SVM, all the NP balancing schemes are also based on the same concept which is the manipulation of redundant switching level of small vectors. As the difference between the phase voltage of positive and negative small vector in the same pair is zero sequence voltage so conversely, the manipulation of small vector is the manipulation of zero sequence voltage. This seems to be equivalence between carrier based and SVM based PWM schemes for NP balance control. NP potential balance is not issue for three-level inverter but for higher level it is still an attractive research area for researchers.

5. Simulation and Experimental Results

The simulation is carried out in MATLAB/SIMULINK for analysis and verification of the discussion presented. The experimental platform was set up using three-level NPC inverter and the control and signal processing tasks were carried out in TMS320F2812 32 bit fixed point DSP. The experiment is carried out at low voltage level to ensure safer operating condition. Dc side voltage is U_{dc} =100V where C1=C2= 3500μf in the experimental setup. The general block diagram of experimental setup is shown in Figure 5.

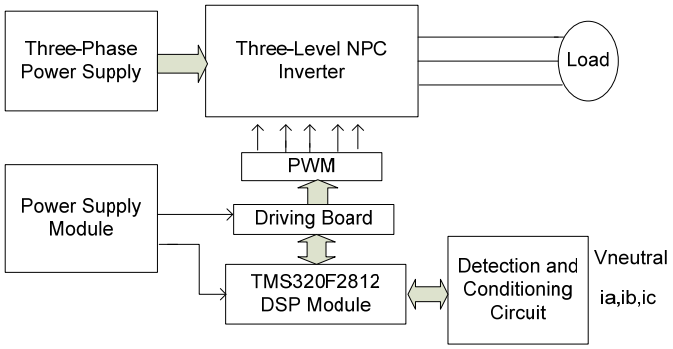

Figure 5. Block Diagram of Experimental Setup

The Figure 6 and Figure 7 show the line to line voltage as obtained from simulation and experimental result. The line to line voltage shows the presence of three-levels, hence providing the output more closer to the sinusoidal wave shape.

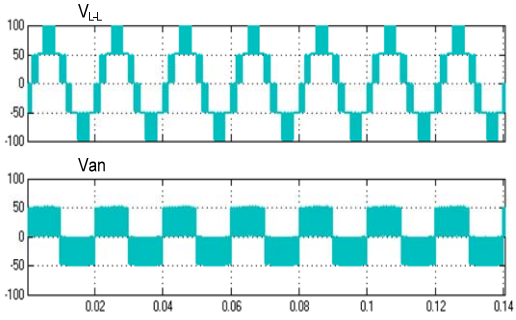

Figure 6. Simulation Results of Inverter Ouput

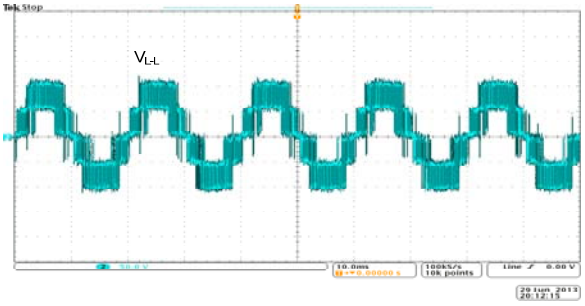

Figure 7. Experimental Result of Inverter Output Line to Line Voltage

Zero sequence injection algorithm based on multicarrier modulation is used to balance the neutral point voltage. Figure 8 and Figure 9 shows the neutral point voltage and the voltage

across two capacitors. In Figure 8 the capacitance of two capacitors is taken 1800uf while in Figure 9 the capacitances of the two capacitors are 1800μf and 1300μf respectively. Besides, the initial voltage of the capacitors is also different in Figure 9. From both figures it can be seen that, the neutral point voltage have been effectively controlled. Figure 10 represents the experimental waveform of neutral point voltage. It can be seen that, the neutral point voltage is maintained around 1V which is quite good. Figure 11 is the experimental waveforms of voltage on C1 and C2 which shows the capacitors voltage are well maintaind also validate that neutral point voltage is under control.

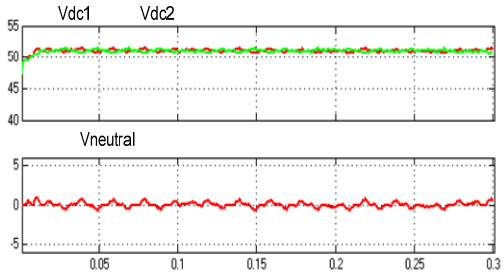

Figure 8. NP Voltage Control Waveform with Same Capacitance

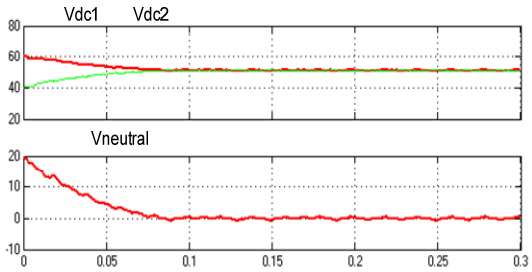

Figure 9. NP Voltage Control Waveforms with Different Capacitance

Figure 10. Neutral Point Voltage Waveform

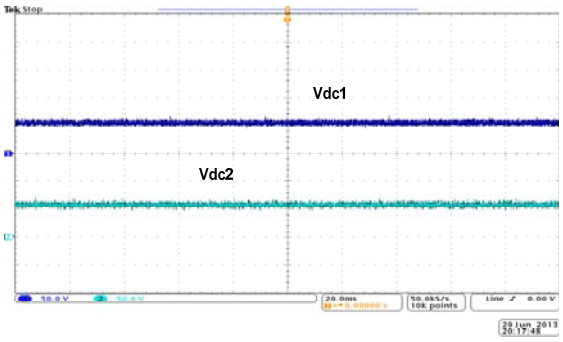

Figure 11. Two Capacitor Voltage Waveform

The simulation and experimental results prove the proper working of NPC inverter topology. The difference in voltage between two capacitors is negligible presenting that neutral point voltage imbalance is not a big issue and can be dealt with.

6. Conclusion

This paper presented the brief summary of NPC multilevel inverter by using three-level circuit topology. Different modulation strategies suitable for NPC inverter like Carrier-based PWM, SVM and SHE is discussed. The problem of neutral point voltage balance which is considered as one of the most extensive drawbacks of this topology is also addressed. Through discussion, simulation and experimental results it is proved that the problem of neutral-voltage balance does not limit the effectiveness of this topology. So the NPC is completely mature topology for medium voltage high power applications.

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