Indonesian Journal of Electrical Engineering and Computer Science
Vol. 37, No. 3, March 2025, pp. 1464~1475
ISSN: 2502-4752, DOI: 10.11591/ijeecs.v37.i3.pp1464-1475

Analysis of FinFET based SRAM cells with improved performance parameters

Deepak Garg[1], Rupali Singh[1], Devendra Kumar Sharma[2]
[1]Department of Electronics and Communication Engineering, SRM Institute of Science and Technology, Delhi-NCR Campus, Ghaziabad, India
[2]Department of Electronics and Communication Engineering, ABES Engineering College, Ghaziabad, India

Article Info

Article history:

Received Mar 5, 2024
Revised Sep 26, 2024
Accepted Sep 30, 2024

Keywords:

Chip area
Fin-FET
MOSFET
Noise voltage
Power dissipation
SRAM

ABSTRACT

To resist the advanced process variation and enable ultra-low power operation, static random-access memory (SRAM) undergoes an expansion stage. The most common type of memory is SRAM, which occupy more than 60% of the chip area. All memories have occupied more than 80% of the circuit area in that day's micro devices, and this trend is expected to continue. This paper develops into the deployment of SRAM using FinFET technology for implementation, with a primary objective of mitigating critical memory parameters, including parameters named as power dissipation, data retention and noise voltage. In this article, multiple simulations are carried out among conventional SRAM cells and FinFET based SRAM cells (6T, 7T, and 8T) utilizing the Cadence Virtuoso tool with a 45nm technology node. In modern era, FinFET is gaining increased preference over CMOS for high controllability of short-channel effects and flexible adjustment of threshold voltage (Vth) through the presence of a double gate. The thinner width of FinFET (Wfin) shows less degradation in performance in compared to thicker width of FET. To improve the circuit performance, the key factors like area, power and delay should be reduced. In the proposed SRAM cell using FinFET, power dissipation is lowered by 17% data retention voltage is reduced by 7% and noise voltage abridged up to 35% as compared to conventional SRAM cell.

Corresponding Author:

Deepak Garg
Department of Electronics and Communication Engineering, SRM Institute of Science and Technology Delhi-NCR Campus
Ghaziabad, Uttar Pradesh, India
Email: deepakgarg1985@gmail.com

1. INTRODUCTION

The increase in transistor densities within very large-scale integration (VLSI) has led to a growth in on-chip cell sizes, resulting in higher power dissipation due to thermal agitation. This phenomenon significantly impacts memory and escalates over generations, driven by increasing demands in various fields and the pursuit of high-performance speeds. The semiconductor industry now finds it imperative to design low-power solutions for integrated circuits (ICs) without compromising data integrity. Beyond the reduction in feature size (W/L), the continuous scaling down of wire sizes plays a crucial role in advancing process technology. Following the era of the "Bi-polar Junction Transistor", the MOSFET emerged, transforming the landscape of VLSI with its scaling capabilities. In 1984, Sekigawa and Hayashi introduced the multi-gate MOSFET (MuGFET), and in 1989, D. with His moto proposed the first fully "Depleted Lean Channel Transistor (DELTA)". The team of UC Berkeley, led by Dr. Chenming Hu, brought Fin-FET to the on-chip

scene in the 1990s. This innovative transistor design effectively mitigates short channel effects, reduces leakage current, and minimizes power dissipation. Memory cells typically utilized complementary metal–oxide–semiconductor (CMOS) design; however, at lower technology nodes, CMOS encountered several challenges including leakage current Ileakage and gate-induced barrier lowering (GIBL). In contrast, FinFET techniques offer solutions to these issues [1]. For error-free read operations, the read-out path, threshold voltage, and stacking scheme of the memory cell can minimize Ileakage [2].

Figure 1 [3] are illustrates the structure of Figure 1(a) planner FET and Figure 1(b) FinFET respectively. FinFET technology enhances controllability for low voltage operations by adding a second gate across from the conventional gate. The functions of both gates are used in a FinFET [4]. When both gates having same potential than FinFET work in shorted gate (SG) mode. SG is a three-terminal device. Independent-gate (IG) Fin-FETs having a physical isolation between gates and it has four terminals. The flexibility of IG FinFET surpasses that of SG FinFET. IG operation initiates when two gates have different voltages, and the remaining gate is used to switch devices and regulates the transistor threshold voltage [5]-[7]. The channel length of Fin-FET is given by (1).

$$\lambda = \sqrt{\frac{\epsilon_{si}}{\epsilon_{ox}}} * t_{si} * t_{ox} \quad (1)$$

Where, short-channel effect is denoted by λ, device body thickness by t_{si}, t_{ox} gate oxide thickness by t_{ox}, permittivity (electric constant) for silicon is denoted by ϵ_{si} and permittivity for oxide is denoted by ϵ_{ox} [8].

In a FinFET the side walls of the fins are called channels [9]. The channel width is given by (2).

$$FinW_{eff} = Fin_{WIDTH} + 4\ \frac{\epsilon_{si}}{\epsilon_{ox}} t_{ox} \quad (2)$$

Where, effect channel width of FinFET is denoted by $FinW_{eff}$ and width of FinFET is denoted by Fin_{WIDTH}.

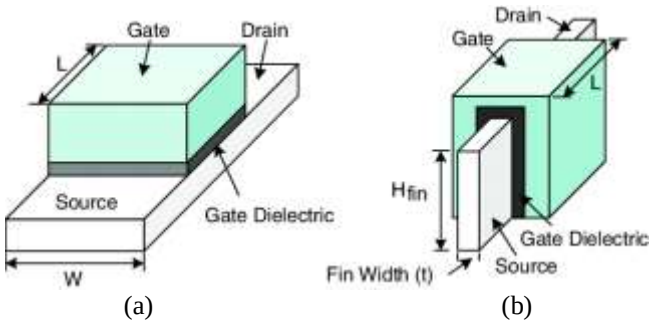

Figure 1. Structure (a) planar FET and (b) FinFET

The static random-access memory (SRAM) cell continues to captivate a broad spectrum of applications, particularly in wireless high-performance system on chip (SoC) and analog mixed signals within the field of microelectronics. In accordance with the international technology roadmap for semiconductors (ITRS), the predictable percentage of SRAM cells in ICs rose from 84% to 94% in year 2014 [10]. SRAM cells are used in 45 nm technology node to store single-bit performance with bi-stable latching circuitry or cross-coupled inverter designs [11].

This type of memory is integral for its ability to store data using cross-coupled inverters, creating a bi-stable latching circuit. In the pursuit of enhancing performance, FinFET based SRAM is strategically designed to replace CMOS based SRAM cells. The objective is to achieve lower power consumption, minimize data noise, and optimize data retention voltage.

The average power dissipation, denoted as P_{avg} is represented in (3).

$$P_{avg} = \frac{1}{T} \int V * I(t)\, dt \quad (3)$$

Where, f (1/T) is frequency, I denotes the current and V the supply voltage.

To study noise voltage level, another parameter which is examine is data retention voltage (Vdr) defined as the minimum supply voltage necessary for retaining data within the SRAM cell, here noise is

considered to undesired signals generated through wire resistance and thermal agitations. The RMS value of noise voltage is denoted as:

$$V_n = \sqrt{4K_B T \Delta f R} \quad (4)$$

where, K_B is Boltzmann constant ($1.3806504 \times 10^{-23}$ J/K), Δf is bandwidth (0.1 Hz to 100 GHz), R is the resistance of circuit element, T is the room temperature.

$$L_V = 20 \log_{10} \frac{V}{V_O} dB \quad (5)$$

$$V = V_o \, 10^{\frac{L_V}{20}} \text{ Volts} \quad (6)$$

Where L_V is noise voltage level, V is noise voltage, V_0 is reference voltage (1.0 V).

The FinFET features a fin-shaped source-drain configuration in a singular strip covered by the gate. The gate functions either independently or with the application of the same signal. The performance parameters of the suggested SRAM cell are presented along with their impressions of process parameter alterations and are compared with those of previously proposed SRAM cells.

The resolution to the stability problem in SRAM cells can be categorized in two main approaches. The first involves circuit topologies, while the second entails employing nonconventional MOSFETs. In a 7T SRAM, Akashe and Sharma [12] proved that reducing the power supply lowers gate $I_{leakage}$. Subsequently, the ground voltage was improved through power gating, effectively reducing gate leakage current $I_{leakage}$. Additionally, adjustments were made to the effective voltages between the two terminals, leading to a significant decrease in both leakage currents $I_{leakage}$. The dual-feedback 8T SRAM cell, as outlined [13], effectively reduces leakage power. In this study, the researchers applied a power gating method to a standard 6T SRAM cell. This technique involves reducing the supply voltage during standby mode by disconnecting the power supply from the cell and elevating the ground potential to prevent a direct path to ground. Consequently, there has been a reduction in leakage power.

Moradi *et al.* [14] proposed a novel SRAM design incorporating body biasing to decrease the power supply to an exceptionally low 0.3 V, which is extremely for efficient SRAM cell functionality. Zhang *et al.* [15] investigated three distinct types of $I_{leakage}$ in bit cells. They also scrutinized various leakage reduction methods including device body biasing, controlled source biasing, negative word line (WL) voltage, energetic supply voltage and bit line (BL) floating structures.

Table 1 summarizes several different FinFET-based SRAM design cells [16]. Ahmad *et al.* [17] proposed cells employing 11T to improve read SNM and write SNM while reducing power consumption. This configuration, developed to meet 45 nm technological standards, occupies twice the surface area of 6T cells. According to Tiwari *et al.* [18], SRAM cells typically feature two straightforward inverters which are cross-coupled and two access transistors. These access transistors, which link the BL, are activated by switching them ON to facilitate operations. The primary advantages include medium power consumption and decreased leakage current ($I_{leakage}$). Lakshmi and Kamaraju [19] presented an 8T FinFET SRAM cell as a solution to overcome the limitations of the conventional 6T cell. A low stationary noise margin (SNM) in read mode may suggest increased writing capabilities. Consequently, circuit designers enjoy greater flexibility for optimization, with functions being effectively isolated.

An investigation of SRAM technology has been presented, focusing on achieving low power consumption and high execution [20], [21]. In efforts to minimize leakage current and short channel effects in deep-submicron circuits, FinFET technology has appeared as a viable choice to bulk FETs. Its advantageous device properties render it well-suited for the design of nano-scale memory circuits, particularly given the growing influence of procedure variations in ultra-deep submicron methods. Consequently, Fin-FETs are gaining popularity in industry owing to their efficiency. Since its inception, the IC industry has placed significant emphasis on optimizing performance parameters like leakage, speed, power and delay [22]. There has been a continuous escalation in efforts to attain extreme throughput from the settings, particularly concerning the power source voltage. This pursuit is the cornerstone of Moore's Law.

Jiang *et al.* [23] note a scarcity of studies comparing the performance of state-of-the-art soft error-tolerant SRAM cells operating at or near sub-threshold voltage levels in terms of factors like read/write access time, read SNM across temperature, write stability, and process corner variations. The existing literature predominantly focuses on conventional soft error-prone SRAM cells.

According to Xue *et al.* [24], computer memory serves the purpose of storing both information and instructions, and it may be categorized as either temporary or permanent. In contrast to random access

memory (RAM), serial access memory offers at once access for both writing and reading operations. Ongoing technological progress facilitates complex designs on a single chip, resulting in compact size, affordability, high speed and low power consumption. Within the VLSI industry, it's essential to anticipate and accommodate variability tolerance to ensure the optimized performance of FinFET circuits.

Table 1. Comparison of FinFET based SRAM

S.No.	Author	Work done	Findings	
			Propagation delay	Power consumption
1.	Ravikishore and Nandhitha [25]	Designed a 6T-SRAM using FinFET technology to optimize delay.	Propagation delay is 33.28 pS	NA
2.	Vallabhuni *et al.* [26]	Comparative validation of SRAM cells designed using FinFET.	Propagation delay is 0.2943 nsec, 0.915nsec and 0.2255 nsec at V_{DD}= 0.1 volt for 7, 8 and 9 transistor respectively.	Power consumption is 1.224 µW, 1.239 µW and 6990 µW at V_{DD}= 0.1 volt for 7,8 and 9 transistors respectively.
3.	Mushtaq and Sharma [27]	Design and analysis of INDEP FinFET SRAM cell at 7-nm technology.	Propagation delay is 12.8 psec and 13.98 psec for a read and writes operation respectively. Propagation delay is 18.01 psec and 16.1psec for a read and writes operation respectively.	Leakage power is 31.01µW and 10.68 µW for a write and read operation respectively. Leakage power is 26.5 µW and 7.26 µW for a write and read operation respectively.
4.	Duari *et al.* [28]	Design a dual port 8T SRAM cell using FinFET and CMOS logic for leakage reduction and enhanced stability.	NA	Leakage power is 52.3 pW and 5.63 nW at 0.5 V for FinFET based and CMOS based SRAM respectively. Leakage power is 572 pW and 62.2 nW at 0.9 V for FinFET based and CMOS based SRAM respectively.
5.	Birla *et al.* [29]	Performance analysis of 8T FinFET SRAM Bit-cell.	NA	The leakage power is 12.61 nW at 0.5 V and 8.92 nW for IG SRAM.
6.	Turi and Delgado-Frias [2]	Design 6T and 8T FinFET SRAMs cells using reverse-biased FinFETs and power gating technique.	NA	Power consumption and speed both are reduced.
7.	Verma *et al.* [30]	Design 10-transistor SRAM using FinFET technology.	Write mode For 6-transistor: 0.0219 nS For 8-transistor: 0.0383 nS	Write mode For 6-transistor: 0.0236 µW For 8-transistor: 0.0268 µW
8.	Ensan *et al.* [31]	Design a low-power single-ended SRAM using FinFET technology.	Propagation delay is 394 psec and 318 psec for a read and writes operation respectively.	Average power: 1.77 µW
9.	Ensan *et al.* [32]	Design a low-power near-threshold SRAM using FinFET technology.	Propagation delay is 491.8 psec and 230.46 psec for a read and writes operation respectively.	The average and static power consumption is 137.66 nW and 5.17 nW respectively.

2. CONVENTIONAL SRAM CELL

2.1. SRAM cell using 6 transistor

Mishra and Akashe [33] defined the most conventional circuit in SoC technology is SRAM cell which goes under the scaling of size and voltage. A 6T SRAM cell comprises six transistors-four NMOS and two PMOS. Among these, four transistors (two NMOS and two PMOS) come together to structure a inverter-pair in a bi-stable latched configuration, In Figure 2, the bi-stable latched style allows the flow of BL data through the remaining two NMOS transistors (N3 and N4).

Two-bit lines, BL as well as BLB, function as complements to one another within the 6T SRAM Cell and have the same period. Similarly, a single WL is complemented by the outputs Q and QB. The SRAM cell functions in three distinct modes: Hold, Active, and Standby mode. In Standby mode, the WL transitions from high to low (WL=0), and the BL, whether 0 or 1, merely retains the data within the inverters which are cross-coupled.

During the write mode, the WL undergoes a transition from low to high (WL=1), enabling the introduction of new data into the BL. This data is then written onto the Q and QB outputs through pass transistors. Subsequently, when the WL transitions WL=0 which directive high to low, the data on the BL is either pre-charged or unconnected. During the write operation, the value stored at output Q is directed through a pass transistor to discharge one of the BLs, while the other BL undergoes pre-charging. Sense amplifier detects the charging and discharging data under the process of read operations. The sensed data is subsequently amplified by the sense amplifier and further utilized at the Q and QB outputs.

2.2. SRAM cell using 7 transistor

The 7-transistor SRAM cell possess of five NMOS and two PMOS. Likewise, the 6T SRAM cell it features a paired inverter configuration (P1 & P2 and N1 & N2) arranged in a bi-stable latch pattern. Additionally, two NMOS transistors (N3 and N4) serve as pass transistors operated by the write line (WL) on their gate terminals. Another NMOS transistor (N5) controls the MOSFET acting as a bridge between the two latches [34].

Before storing the data at output Q and QB, the write function is controlled by the N5 transistor with only BLB performs during this operation. During read operations, the N5 transistor is working, and the value of the SRAM cell output is sensed by a sense amplifier. The BL and BLB can be either pre-charged or in a discharged state during this phase. The standby mode operates similarly to the 6T SRAM cell, and the circuit configuration is illustrated in Figure 3.

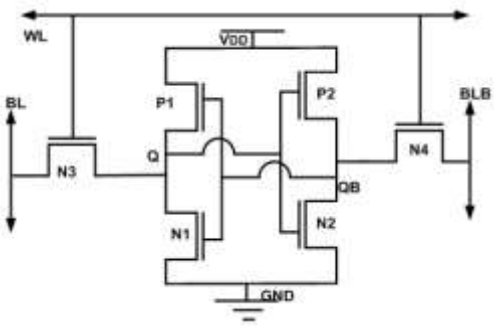

Figure 2. Conventional SRAM cell using 6T

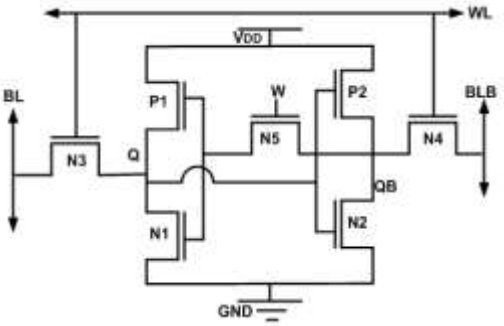

Figure 3. Conventional SRAM cell using 7T

2.3. SRAM cell using 8 transistor

To address stability issues encountered in the standby and read modes of earlier SRAM cells, an 8T SRAM cell has been developed. This design incorporates a bi-stable latch comprising four MOSFETs (P1 & P2 and N1 & N2) and two pass transistors (N3 and N4). In the 8T configuration, two additional transistors operate on the QB output data as depicted in Figure 4. The storage SRAM cell includes RWL and WL (N5 and N6) or read bit line (RBL) and BL representing the read and write BL respectively. This dual-port design enables one port for writing data and the other for reading stored data.

In the write mode, the operation is similar that of the 6T SRAM cell where the WL=1 transitioning from low to high results in the storage of BLB and BL data in the Q and QB outputs. During read mode, the stored data at QB is accessed by activating the RBL=1 from low to high. This operation is facilitated by N6 and N7 transistors using the ground node and is sensed by a sense amplifier. Importantly, these operations are performed independently [1]. Consequently, the 8T SRAM cell exhibits high performance, albeit with a 32% increase in cell size, as indicated ITRS in 2014.

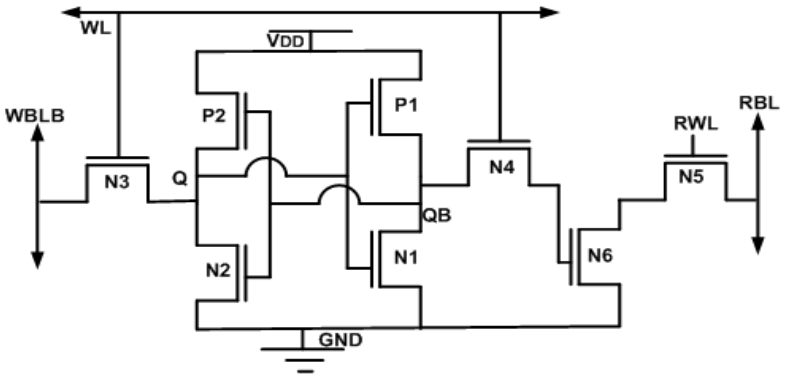

Figure 4. Conventional SRAM cell using 8T

3. PROPOSED SRAM CELL UTILIZING FINFET TECHNOLOGY

In the starting phase of VLSI, memory design was relatively simple as it considered storing only single bits of data. However, in the current scenario, the memory utilized in various applications is no longer singular; instead, it comprises an array of memory. This transition is prompted by the necessity to tackle issues like power dissipation, noise immunity and data retention in densely populated ICs.

To tackle these issues, future technology demands inherent scaling capabilities to reduce size making FinFET a pivotal solution for this evolving landscape. FinFET stands out as a superior choice compared to conventional CMOS, offering better mitigation of short-channel effects, scalability in power supply and lower power dissipation [4], [35]. The circuit diagram of FinFET based SRAM cell using 6T, 7T, and 8T is shown in Figures 5-7 respectively.

CMOS technology which is based on MuGFET is applied to SRAM cells and e-memory, addressing cell stability problems, minimizing leakage current, and improving components mismatch. The low-power design is particularly advantageous with FinFET, as it eliminates body biasing for leakage reduction and operates on a lower power supply voltage as compared to CMOS logic.

Fin-FET width obligatory efforts to design SRAM cell by adjusting the threshold voltage (V_{th}) of SRAM cell [36]. So, in this article, 6T, 7T, and 8T SRAM cells are designed using model [1] and studied at various voltages.

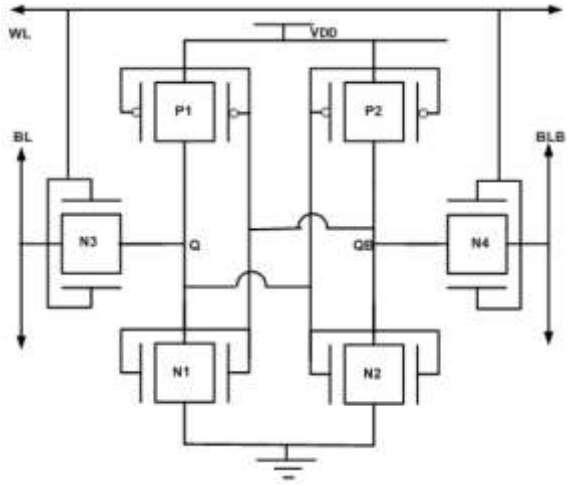

Figure 5. FinFET based SRAM cell using 6T

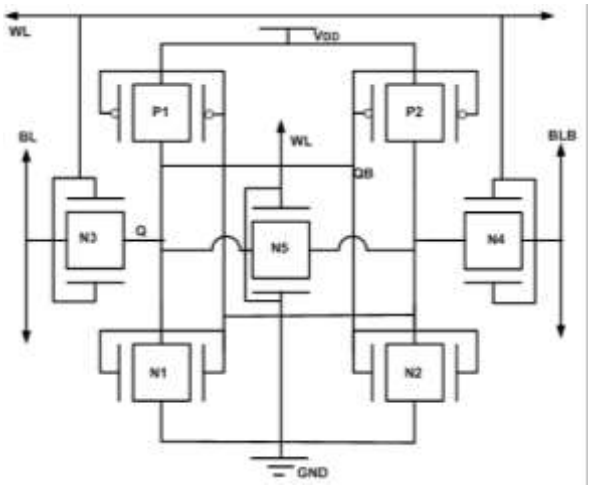

Figure 6. FinFET based SRAM cell using 7T

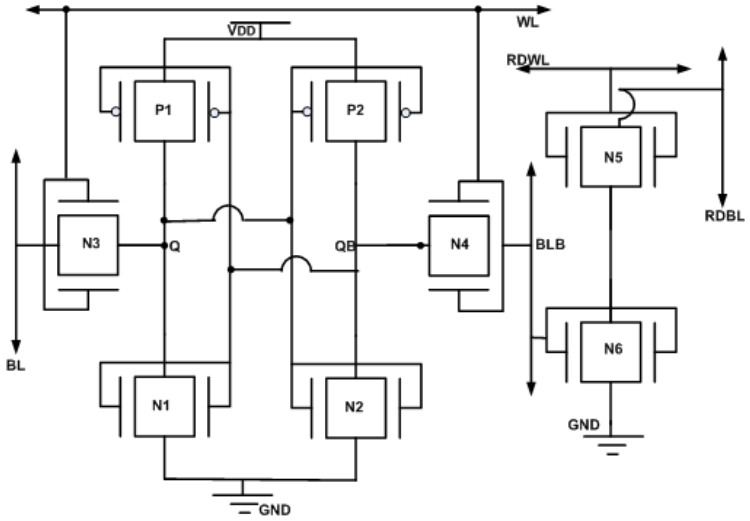

Figure 7. FinFET based SRAM cell using 8T

4. SIMULATION RESULTS AND DISCUSSION

4.1. Self-heating and power dissipation

The occurrence of self-heating in a circuit is attributed to parasitic elements present within it, impacting the local temperature (27 °C). The average power dissipation occurs due to biasing, wiring and loose connection that affects mobility and threshold voltage [37]. This dissipation can be managed through voltage control or technological variations. The design of a low-power solution involves the utilization of a Fin-FET-based SRAM cell. A comparative analysis of average power between conventional and Fin-FET based SRAM is presented in Table 2.

Table 2. Comparison of average power between conventional and Fin-FET based SRAM

Supply voltage (V)	Average power dissipation (nW)					
	Conventional SRAM cell			FinFET based SRAM cell		
	6T SRAM	7T SRAM	8T SRAM	6T SRAM	7T SRAM	8T SRAM
0.7	57.24	45.92	81.64	25.462	33.48	73.56
0.6	23.24	20.68	36.69	21.76	17.76	32.86
0.5	11.34	9.83	13.46	8.96	8.26	11.24
0.4	6.94	6.54	7.96	2.968	4.986	5.042
0.3	2.348	2.132	2.865	2.161	1.946	2.368
0.2	0.424	0.386	0.542	0.384	0.326	0.386
0.1	0.047	0.047	0.072	0.047	0.0526	0.056

As per Table 2, FinFET based SRAM cell power dissipation has lesser than conventional based SRAM cell. Let us take overview at 0.7 V, 6T SRAM cell gives 52.32 nW is power dissipation but in FinFET based 6T SRAM cell which is offered in this paper gives 21.687 nW. Similarly, due to movement from conventional to FinFET based SRAM cell power dissipation decreases up to 21%.

4.2. Average noise

Noise, an undesired signal, has the potential to distort data within an SRAM cell particularly during write operations. When the output data in the cross-coupled inverters are in a hold mode, noise can introduce variations at the output terminals specifically at Q and QB. A comparative analysis is presented in Table 3 which illustrates the operation of various SRAM cells, highlighting the distinctions between conventional and FinFET-based memory technologies.

Next work emphasizes on Noise Voltage of CMOS based and FinFET based SRAM cell for 45 nm technology [38]. Noise, an undesired signal, distorts data in SRAM cell, primarily impacting write operation. During the hold mode of the cross-coupled inverter, Noise can alter the data at the terminals of output Q and QB [39].

As per the Table 3, the SRAM cell using FinFET exhibits a lower average noise voltage compared to the conventional SRAM cell. Taking a closer look at the overview with a voltage of 0.7 V, the 6T SRAM cell yields an average noise voltage of 7.591 nV whereas the FinFET-based 6T SRAM cell proposed a reduced value of 6.003 nV. This transition from conventional CMOS to FinFET-based SRAM cells results in a noteworthy decrease in noise involvement in the voltage value of data, amounting to a reduction of 24%.

Table 3. Comparison of average noise voltage between conventional and Fin-FET based SRAM

Supply voltage (V)	Average noise voltage (nV)					
	Conventional SRAM cell			FinFET based SRAM cell		
	6T SRAM	7T SRAM	8T SRAM	6T SRAM	7T SRAM	8T SRAM
0.7	7.392	8.909	7.246	6.018	5.824	5.926
0.6	7.382	8.924	7.584	6.232	6.324	6.182
0.5	7.126	7.678	7.056	6.124	6.436	6.044
0.4	5.180	5.184	5.164	4.892	5.424	4.784
0.3	2.462	2.564	2.462	2.446	2.862	2.348
0.2	1.056	1.030	1.058	0.998	1.184	0.982

4.3. Data retention voltage

To maintain data retention at the high states in standby mode, the supply voltage is reduced to achieve the Vdr [40]. With a decrease in the power supply, the state of the SRAM cell remains unchanged, leading to a reduction of the static noise margin to zero as illustrated in table 4.0. A comparative analysis is presented in Table 4 illustrates the operation of various SRAM cells, highlighting the distinctions between conventional and FinFET-based memory technologies.

Table 4. Comparison of data retention voltage between conventional and Fin-FET based SRAM

Mode	Data retention voltage (Vdr)					
	Conventional SRAM cell			FinFET based SRAM cell		
	6T SRAM	7T SRAM	8T SRAM	6T SRAM	7T SRAM	8T SRAM
Transient	0.4	0.39	0.43	0.336	0.349	0.346
DC	0.5	0.5	0.5	0.1515	0.249	0.195

The data retention voltage in a SRAM cell using is lower than that in a conventional SRAM cell. Specifically, in a 6T SRAM cell, data is secured at 0.4V while in the proposed SRAM cell using FinFET cell it is achieved at a slightly lower voltage of 0.376V. This transition from conventional CMOS to SRAM cell using FinFET results in a reduction in the data retention voltage value of data by 6-10%.

The Table 5 compares the performance parameters of FinFET-based SRAM cells with those of several other SRAM cell configurations and Figure 8 demonstrates that SRAM cell designs based on Fin-FET technology exhibit lower average noise voltage and average power dissipation.

Table 5. Performance comparison of SRAM

Author	SRAM size	Average noise voltage	Average power
Duari *et al.* [28]	6T-SRAM	NA	5.23E-05
Mushtaq and Sharma [27]	6T-SRAM	NA	4.17E-05
Mishra *et al.* [41]	6T-SRAM	NA	2.64E-05
Lakshmi and Kamaraju [19]	7T-SRAM	NA	2.63E-05
Athe and Dasgupta [42]	8T-SRAM	NA	6.7E-05
Premalatha *et al.* [43]	7T-SRAM	NA	10.534E-05
Premalatha *et al.* [43]	8T-SRAM	NA	9.317E-05
Lakshmi and Kamaraju [19]	8T-SRAM	NA	3.59E-05
Athe and Dasgupta [42]	8T-SRAM	NA	10.1E-05
Proposed	6T-SRAM	6.23E-09	2.18E-05
	7T-SRAM	6.32E-09	1.78E-05
	8T-SRAM	6.18E-09	3.29E-05

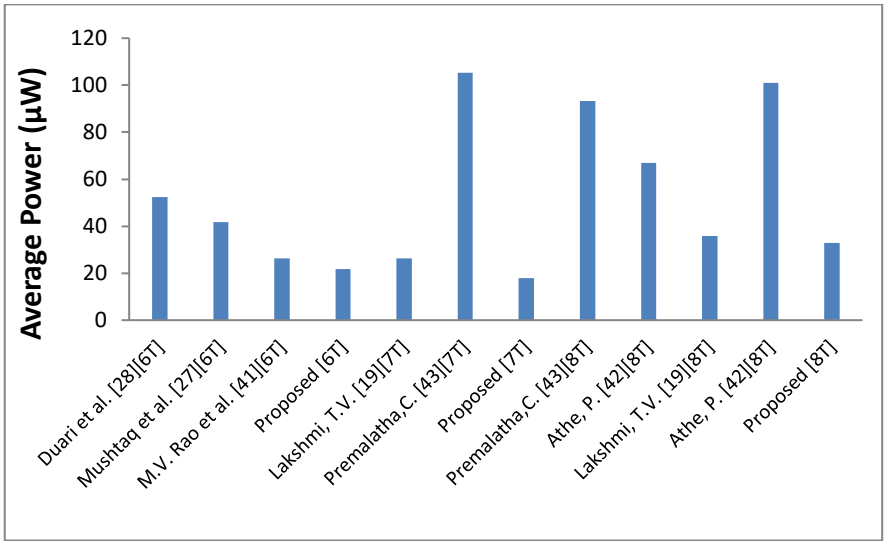

Figure 8. Comparative chart for various SRAM cell

4.4. Procedure to design SRAM cell

The proposed work is done in Virtuoso platform using 45 nm technologies. The flow of design is as shown Figure 9 and used steps in designing are given as:

Step-1: Start Cadence Virtuoso tool and draw the schematic diagram of SRAM cell using instances
Step-3: Instruction for checking errors in schematic diagram
Step-4: Save the diagram and create the symbol
Step-5: Instruction for checking errors in symbol
Step-6: Save the symbol and build the remaining design

Step-7: Start the simulation using spectre and verify the analysis reports
Step-8: If satisfied with reports, generate the report using parametric analysis and note down the reading.

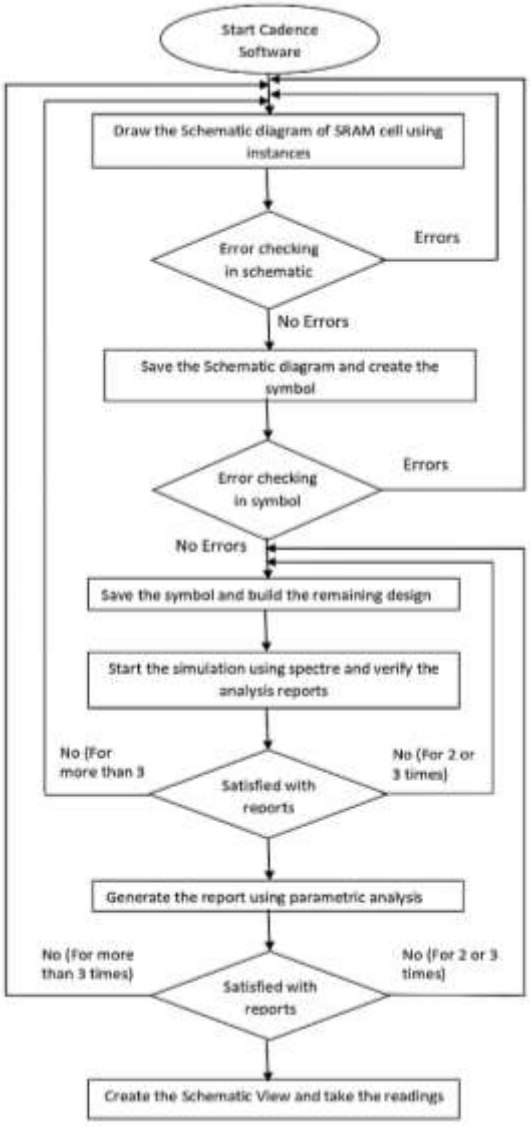

Figure 9. Flow chart for designing of SRAM cell

5. APPLICATIONS IN REAL TIME WORLD

Proposed technology widely utilized in some applications in real time world are:

a) High-performance computing: used in processors and high-speed caches where performance is critical.
b) Mobile devices: essential for smartphones and tablets, where low power consumption and compact size are crucial.
c) Consumer electronics: found in various gadgets and electronics where power efficiency and performance are important.
d) Networking equipment: utilized in routers and switches where high-speed data access and low latency are required.

6. CONCLUSION

This study explores the design of 45 nm SRAM cells using both traditional and FinFET technologies, with a specific focus on key factors like data retention voltage, average power usage, and noise

voltage. It starts by investigating Vdr, a crucial parameter to understand the minimum voltage required for FinFET-designed SRAM cells to function properly without corrupting stored data. The analysis reveals that the FinFET-based 6T SRAM cell outperforms its conventional counterpart primarily due to its smaller size. Additionally, across various metrics, SRAM cells utilizing FinFET consistently demonstrate superior performance compared to the conventional ones. Specifically, in the 45 nm technology context, FinFET-based SRAM cells exhibit reduced power usage from 76.65 to 21.687 nW (lowered by 17%), decreased noise voltage up to 35% and reduce up to 7% Vdr. Looking ahead, there is a growing emphasis on minimizing power consumption, noise voltage, area, and latency.

The performance and durability of FinFET based SRAM cells in the future need to increase to meet the increasing demands of microprocessors. Further investigation into compute-in-memory within the framework of in-memory digital domain computing is necessary for the advancement of artificial intelligence in small electronic devices. Because the power of these devices is restricted, computing requires low-power, dependable processes. It is anticipated that bulk-Si MOSFET SRAM cells will perform less well than FinFET-based SRAM cells.

REFERENCES

[1] J. V. Suman, K. K. Cheepurupalli, and H. L. Allasi, "Design of polymer-based trigate nanoscale FinFET for the implementation of two-stage operational amplifier," *International Journal of Polymer Science*, vol. 2022, 2022, doi: 10.1155/2022/3963188.

[2] M. A. Turi and J. G. Delgado-Frias, "Effective Low Leakage 6T and 8T FinFET SRAMs: using cells with reverse-biased FinFETs, near-threshold operation, and power gating," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 4, pp. 765–769, 2020, doi: 10.1109/TCSII.2019.2922921.

[3] X. Guo, V. Verma, P. Gonzalez-Guerrero, S. Mosanu, and M. R. Stan, "Back to the future: digital circuit design in the FinFET Era," *Journal of Low Power Electronics*, vol. 13, no. 3, pp. 338–355, Sep. 2017, doi: 10.1166/jolpe.2017.1489.

[4] S. Kaushal and A. K. Rana, "Negative capacitance junctionless FinFET for low power applications: an innovative approach," *Silicon*, vol. 14, no. 12, pp. 6719–6728, Aug. 2022, doi: 10.1007/s12633-021-01392-x.

[5] M. S. Badran, H. H. Issa, S. M. Eisa, and H. F. Ragai, "Low leakage current symmetrical dual-k 7 nm trigate bulk underlap FinFET for ultra low power applications," *IEEE Access*, vol. 7, pp. 17256–17262, 2019, doi: 10.1109/ACCESS.2019.2895057.

[6] K. S. Palanisamy and R. Ramachandran, "FinFET-based power-efficient, low leakage, and area-efficient DWT lifting architecture using power gating and reversible logic," *International Journal of Circuit Theory and Applications*, vol. 48, no. 8, pp. 1304–1318, Aug. 2020, doi: 10.1002/cta.2794.

[7] S. S. Ensan, M. H. Moaiyeri, B. Ebrahimi, S. Hessabi, and A. Afzali-Kusha, "A low-leakage and high-writable SRAM cell with back-gate biasing in FinFET technology," *Journal of Computational Electronics*, vol. 18, no. 2, pp. 519–526, Jun. 2019, doi: 10.1007/s10825-019-01327-1.

[8] N. Rahman and B. P. Singh, "Static-noise-margin analysis of conventional 6T SRAM cell at 45 nm technology," *International Journal of Computer Applications*, vol. 66, no. 20, pp. 975–8887, 2013.

[9] Y. Atalla, Y. Hashim, and A. N. Abd. Ghafar, "The impact of channel fin width on electrical characteristics of Si-FinFET," *International Journal of Electrical and Computer Engineering (IJECE)*, vol. 12, no. 1, p. 201, Feb. 2022, doi: 10.11591/ijece.v12i1.pp201-207.

[10] S. Singh and V. Mishra, "Enhanced static noise margin and increased stability SRAM cell with emerging device memristor at 45-nm technology," *Radioelectronics and Communications Systems*, vol. 61, no. 5, pp. 200–206, May 2018, doi: 10.3103/S0735272718050035.

[11] S. M. Koh, G. S. Samudra, and Y. C. Yeo, "Contact technology for strained nFinFETs with silicon-carbon source/drain stressors featuring sulfur implant and segregation," *IEEE Transactions on Electron Devices*, vol. 59, no. 4, pp. 1046–1055, Apr. 2012, doi: 10.1109/TED.2012.2185799.

[12] S. Akashe and S. Sharma, "Leakage current reduction techniques for 7T SRAM cell in 45 nm technology," *Wireless Personal Communications*, vol. 71, no. 1, pp. 123–136, Jul. 2013, doi: 10.1007/s11277-012-0805-1.

[13] A. Vaknin, O. Yona, and A. Teman, "A double-feedback 8T SRAM bitcell for low-voltage low-leakage operation," in *2013 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference, S3S 2013*, Oct. 2013, pp. 1–2, doi: 10.1109/S3S.2013.6716565.

[14] F. Moradi, S. K. Gupta, G. Panagopoulos, D. T. Wisland, H. Mahmoodi, and K. Roy, "Asymmetrically doped FinFETs for low-power robust SRAMs," *IEEE Transactions on Electron Devices*, vol. 58, no. 12, pp. 4241–4249, Dec. 2011, doi: 10.1109/TED.2011.2169678.

[15] L. J. Zhang, C. Wu, Y. Q. Ma, J. Bin Zheng, and L. F. Mao, "Leakage power reduction techniques of 55 nm SRAM cells," *IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India)*, vol. 28, no. 2, pp. 135–145, 2011, doi: 10.4103/0256-4602.78105.

[16] V. Kumbar and M. Waje, "A Comparative Analysis of FinFET Based SRAM Design," *International Journal of Electrical and Electronics Research*, vol. 10, no. 4, pp. 1191–1198, 2022, doi: 10.37391/ijeer.100468.

[17] S. Ahmad, M. K. Gupta, N. Alam, and M. Hasan, "Single-ended schmitt-trigger-based robust low-power SRAM cell," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 8, pp. 2634–2642, Aug. 2016, doi: 10.1109/TVLSI.2016.2520490.

[18] N. Tiwari, V. Neema, K. J. Rangra, Y. C. Sharma., "Performance parameters of low power sram cells: a review," *i-manager's Journal on Circuits and Systems*, vol. 6, no. 1, p. 25, 2018, doi: 10.26634/jcir.6.1.14495.

[19] T. V. Lakshmi and M. Kamaraju, "A review on SRAM memory design using FinFET technology," *International Journal of System Dynamics Applications*, vol. 11, no. 6, pp. 1–21, Jun. 2022, doi: 10.4018/ijsda.302665.

[20] S. Oza, "Finfet based sram design for low power applications," *International Journal of Electrical*, vol. 3, no. 2, pp. 2320–2084, 2014.

[21] L. F. Rahman, M. F. B. Amir, M. Bin Ibne Reaz, M. Marufuzzaman, and H. Husain, "Advances on low power designs for SRAM cell," *TELKOMNIKA Indonesian Journal of Electrical Engineering*, vol. 12, no. 8, Aug. 2014, doi: 10.11591/telkomnika.v12i8.5538.

[22] A. Chakraborty, R. S. Tomar, and M. Sharma, "Optimization of low power 12 T SRAM bit cell using FinFET in 32 nm technology," *Materials Today: Proceedings*, vol. 80, pp. 226–232, 2022, doi: 10.1016/j.matpr.2022.12.078.
[23] J. Jiang, Y. Xu, W. Zhu, J. Xiao, and S. Zou, "Quadruple cross-coupled latch-based 10T and 12T SRAM Bit-cell designs for highly reliable terrestrial applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 3, pp. 967–977, Mar. 2019, doi: 10.1109/TCSI.2018.2872507.
[24] X. Xue *et al.*, "Design and performance analysis of 32 × 32 memory array SRAM for low-power applications," *Electronics (Switzerland)*, vol. 12, no. 4, p. 834, Feb. 2023, doi: 10.3390/electronics12040834.
[25] G. Ravikishore and N. M. Nandhitha, "6T-SRAM design to optimize delay using finfet technology," in *Proceedings of the 3rd International Conference on Intelligent Communication Technologies and Virtual Mobile Networks, ICICV 2021*, Feb. 2021, pp. 540–544, doi: 10.1109/ICICV50876.2021.9388559.
[26] R. R. Vallabhuni, K. C. Koteswaramma, B. Sadgurbabu, and G. A, "Comparative validation of SRAM cells designed using 18 nm FinFET for memory storing applications," *SSRN Electronic Journal*, 2020, doi: 10.2139/ssrn.3733530.
[27] U. Mushtaq and V. K. Sharma, "Design and analysis of INDEP FinFET SRAM cell at 7-nm technology," *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, vol. 33, no. 5, Sep. 2020, doi: 10.1002/jnm.2730.
[28] C. Duari, S. Birla, and A. K. Singh, "A dual port 8T sram cell using finfet & cmos logic for leakage reduction and enhanced read & write stability," *Journal of Integrated Circuits and Systems*, vol. 15, no. 2, pp. 1–7, Jul. 2020, doi: 10.29292/jics.v15i2.140.
[29] S. Birla, N. K. Shukla, N. Singh, and R. K. Raja, "Performance analysis of 8T FinFET SRAM bit-cell for low-power applications," in *Proceedings of the 2020 International Conference on Computing, Communication and Security, ICCCS 2020*, Oct. 2020, pp. 1–4, doi: 10.1109/ICCCS49678.2020.9277237.
[30] J. Verma, A. Passi, S. Sindhu, and S. Gayathiri, "Design 10-transistor (10t) Sram using FinFET technology," *International Journal of Engineering and Advanced Technology*, vol. 9, no. 1, pp. 566–572, Oct. 2019, doi: 10.35940/ijeat.A9690.109119.
[31] S. S. Ensan, M. H. Moaiyeri, M. Moghaddam, and S. Hessabi, "A low-power single-ended SRAM in FinFET technology," *AEU - International Journal of Electronics and Communications*, vol. 99, pp. 361–368, Feb. 2019, doi: 10.1016/j.aeue.2018.12.015.
[32] S. S. Ensan, M. H. Moaiyeri, and S. Hessabi, "A robust and low-power near-threshold SRAM in 10-nm FinFET technology," *Analog Integrated Circuits and Signal Processing*, vol. 94, no. 3, pp. 497–506, Mar. 2018, doi: 10.1007/s10470-018-1107-7.
[33] V. Mishra and S. Akashe, "Calculation of average power, leakage power, and leakage current of FinFET based 4-bit priority encoder," in *International Conference on Advanced Computing and Communication Technologies, ACCT*, Feb. 2015, vol. 2015-April, pp. 65–69, doi: 10.1109/ACCT.2015.82.
[34] J. R. Schwank, V. Ferlet-Cavrois, M. R. Shaneyfelt, P. Paillet, and P. E. Dodd, "Radiation effects in SOI technologies," *IEEE Transactions on Nuclear Science*, vol. 50 III, no. 3, pp. 522–538, Jun. 2003, doi: 10.1109/TNS.2003.812930.
[35] H. Amrouch *et al.*, "Impact of variability on processor performance in negative capacitance FinFET technology," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 9, pp. 3127–3137, Sep. 2020, doi: 10.1109/TCSI.2020.2990672.
[36] A. Navaneetha and K. Bikshalu, "Reliability analysis of FinFET based high performance circuits," *Electronics (Switzerland)*, vol. 12, no. 6, p. 1407, Mar. 2023, doi: 10.3390/electronics12061407.
[37] M. V. N. Rao *et al.*, "Design and development of efficient SRAM cell based on FinFET for low power memory applications," *Journal of Electrical and Computer Engineering*, vol. 2023, pp. 1–13, Jun. 2023, doi: 10.1155/2023/7069746.
[38] V. Mishra, A. Kumar, and S. Akashe, "New non-volatile memory technologies and neuromorphic computing," in *Proceedings - 2023 IEEE World Conference on Applied Intelligence and Computing, AIC 2023*, Jul. 2023, pp. 857–862, doi: 10.1109/AIC57670.2023.10263872.
[39] S. Akashe, S. Bhushan, and S. Sharma, "High density and low leakage current based 5T SRAM cell using 45 nm technology," *Romanian Journal of Information Science and Technology*, vol. 15, no. 2, pp. 155–168, 2012.
[40] S. Khandelwal and S. Akashe, "Design of 10T SRAM with sleep transistor for leakage power reduction," *Journal of Computational and Theoretical Nanoscience*, vol. 10, no. 1, pp. 165–170, Jan. 2013, doi: 10.1166/jctn.2013.2673.
[41] V. Mishra, S. Singh, U. Pradesh, and U. Pradesh, "Design optimization of memristor based 6T and 7T SRAM cells using sleep transistor at nanoscale techniques," *International Journal of Computational Engineering & Management*, vol. 19, no. 2, pp. 2–5, 2016.
[42] P. Athe and S. Dasgupta, "A comparative study of 6T, 8T and 9T decanano SRAM cell," in *2009 IEEE Symposium on Industrial Electronics and Applications, ISIEA 2009 - Proceedings*, Oct. 2009, vol. 2, pp. 889–894, doi: 10.1109/ISIEA.2009.5356318.
[43] C. Premalatha, K. Sarika, and P. M. Kannan, "A comparative analysis of 6T, 7T, 8T and 9T SRAM cells in 90 nm technology," in *Proceedings of 2015 IEEE International Conference on Electrical, Computer and Communication Technologies, ICECCT 2015*, Mar. 2015, pp. 1–5, doi: 10.1109/ICECCT.2015.7226147.

BIOGRAPHIES OF AUTHORS

Deepak Garg received his B. Tech. in Electronics and Communication Engineering from U.P.T.U., Lucknow and M.Tech. from Shobhit University, Meerut in 2007, 2010 respectively. Currently, he is pursuing Ph.D. from SRM Institute of Science and Technology, Delhi-NCR Campus, Ghaziabad. His research interests include digital circuit design, VLSI. He can be contacted at email: deepakgarg1985@gmail.com.

Rupali Singh received his B. Tech. in Electronics and Communication Engineering from Nagpur University and M. Tech. from Shobhit University, Meerut, and Ph.D. degree from SRMIST, Ghaziabad, India in 2001, 2009 and 2021 respectively. Currently, she is working at the Department of Electronics and Communication Engineering, SRM IST, Ghaziabad as an associate professor and head. Her research area includes low power circuits, reversible logic, and QCA. She can be contacted at email: rupalis@srmist.edu.in.

Devendra Kumar Sharma received his B.E. degree in Electronics Engineering from M.N.R. Engineering College, Allahabad, M.E. degree from University of Roorkee, and Ph.D. degree from NIT Kurukshetra, India in 1989, 1992, and 2016 respectively. He served PSUs in different positions for more than 8 years in QA & Testing/R&D departments. Currently, he is working in ABES Engineering College, Ghaziabad, India as a professor and director. His research interests include VLSI interconnects, digital design, testing, and signal processing. He can be contacted at email: d_k_s1970@yahoo.co.in.