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Design and analysis of low power sense amplifier for static random access memory

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ABSTRACT

Today's era is a digital world where each and every section of the society is experiencing and encountering with semiconductor chips. In very large-scale integration (VLSI) circuits the design of static random-access memory (SRAM) plays a crucial role in ensuring both low-power consumption and high-speed performance. The sense amplifiers (SA) are integral parts for information accessing storage in SRAM IC design. This paper introduces a dual voltage latch sense amplifier (DVLSA) for SRAM integrated circuits (IC). The comparative analyses of various SA are studied and then design a low-power SA through the implementation of energy-efficient technique. Further, we have elucidated the causes of delay and power dissipation in different SA with useful solutions and performance evaluation is conducted by comparing the proposed design with existing SA reported in the literature. The performance parameters such as power 1.604 uw, energy 470.50 fJ, delay 80.04 ps, and current 5.406 are scrutinized to assess the efficiency of the designs. The cell outcomes have been validated with cadence tool on 180 nm technology and operate at 1.8 V. The proposed design, namely, DVLSA demonstrates minimal energy consumption and low power dissipation, making it a promising advancement in SRAM IC technology.

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1. INTRODUCTION

In the growing realm of high-speed and low-power very large-scale integration (VLSI) circuits, the sense amplifier (SA) has become a focal point for extensive utilization in CMOS memory and circuits. The SRAM circuit plays a pivotal role, exerting a significant impact on power consumption, delay and overall design stability. Consequently, static random-access memory (SRAM) cache emerges as a critical component in modern VLSI systems, especially for portable electronic devices [1]. Embedded within "silicon on chip" (SOC) circuits, permanent memory retains data even after power disconnection facilitating high-level integration.

SRAMs find applications in consumer appliances, exerting a profound influence on system performance in terms of energy consumption, speed, and reliability [2]. Their ability to perform high-speed and low-power operations makes them particularly desirable. However, a key challenge in SRAM circuits lies in striking a balance between writing and reading operations [3].

The SA plays a critical role in the peripheral circuit for SRAM, identifying and reading the information stored within the bit cell during the action. The SA senses low signal voltage differences on the bit lines and amplifies them to the desired level, primarily functioning during memory read operations.

It is instrumental in amplifying the low signal difference to the preferred logic level [4]. Differential SAs, also known as voltage mode ASs (VMSA), are employed, as they do not pass static current. To enhance memory performance and speed, it is imperative to identify and analyze the significance and benefits of various VMSAs. Among them, dual voltage latch SAs stand out for their power and speed performance, although careful control is required due to the input line also serving as the output line [5]. Notably, the proposed SA demonstrates minimal power consumption among these SAs.

In this study, an enhanced dual-voltage cross-coupled latch SA is devised, employing low-power techniques such as multiple threshold CMOS (MTCMOS), VTCMOS, and DTCMOS. This design demonstrates superior performance in terms of energy efficiency, delay and power consumption when compared to other SA documented in the literature. The SA plays a crucial role in the read circuitry, tasked with detecting low-power signals from a bit line that signifies the stored data (0 or 1) in a memory cell. Its primary function is to magnify the small voltage difference to a discernible level, allowing for accurate interpretation of data from the memory cell's exterior. SA are categorized as either voltage or current SA based on the nature of the input signal.

2. EARLIER IMPLEMENTED TOPOLOGIES

2.1. Voltage-mode/current-mode SA

In this section, various well-established SA topologies reported earlier are outlined. The SA serves as an essential component in the assembly of memory integrated circuit (IC) chips within the semiconductor industry. It plays a crucial role in the reading circuit systems employed for data retrieval in memory, making it indispensable for overall functionality and performance. SAs are instrumental in extracting data from memory cells, with their primary function being to sense stored data through bit-line voltage discharge. They, then, amplify the subtle voltage signal differences to reach an optimal voltage level, ensuring accurate demonstration of the stored data by logic external to the memory [6]. One prominent and effective SA is based on SRAM utilizing a dual-voltage cross-coupled voltage latch SA. Figure 1 (in APPENDIX) illustrates a selection of existing SAs that successfully achieve the desired objectives.

Figure 1(a) illustrates the design of the high-speed voltage latch sense amplifier (HSVLSA) [7]. The circuit incorporates three negative channel metal-oxide-semiconductor (NMOS) transistors (N1, N2, and N3), two PMOS transistors (P1 and P2), and a CMOS inverter. Operation initiates with an active enable signal (EN), where the SA detects the voltage differences on the bit lines "BL" and "BLB," and the resulting output voltage is generated. Achieving an optimal SA design is a primary consideration in the design of SRAM-based circuits [8]. To enhance magnitude, a CMOS inverter is connected to the SA output. However, the high gain of the inverter leads to elevated output (Vout) and incurs a higher cost for HSVLSA.

Figure 1(b) presents the schematic of the conventional cross-coupled voltage latch sense amplifier (CCVLSA) [9]. The circuit is divided into three sections: driver, access, and load transistors. Literature contains diverse SAs designed for various memory cells with voltage latch sense amplifier (VMSA) gaining recognition for its simplicity and performance. Careful selection of the EN is crucial in voltage latch SA, as the output line also functions as an input line. The footer transistor N3 is employed to mitigate leakage current during standby mode, and when EN is high, the SA operates in an active mode.

Enhancements in both performance and current path for the CCVLSA were achieved through modification resulting in the creation of the double switch cross-coupled voltage latch sense amplifier (DSCVMSA) [10]. Figure 1(c) illustrates the standard current mode sense amplifier (CMSA) which is based on the latch-type VMSA [11]. This circuit comprises four PMOS transistors (P1, P2, P3, and P4) and five NMOS transistors (N1, N2, N3, N4, N5). The positive feedback is provided by two cross-coupled inverters, similar to previous circuits but with an added bit line connection through two NMOS transistors, N3 and N4, resulting in high input impedance. Precharge transistors P3 and P4 are activated when the enable (EN) signal is "0," charging the out nodes to the supply voltage (Vdd). When EN is "1," P3 and P4 turn "OFF," and N5 turns "ON," pulling the drain of N5 down to ground level. This allows for amplification without current passing through bit lines to the output reducing power consumption.

To further enhance performance and reduce costs, the dual voltage cross-coupled voltage latch sense amplifier (DVCVMSA) is designed, as depicted in Figure 1(d). This design utilizes nine transistors and operates similarly to the conventional cross-coupled voltage latch SA, with two additional PMOS transistors (P1 and P2) connected to Vdd. Double voltage with swing restoration logic and additional parameters such as stability and delay are incorporated. These types of circuits increase noise margins while decreasing sizing requirements. The transmission gate voltage latch sense amplifier (TGVLSA) design, shown in Figure 1(e), consists of four PMOS (P1, P2, P3, and P4) and five NMOS (N1, N2, N3, N4, and N5) transistors. TGVLSA operates similarly to CCVLSA with two additional transistors (N4 and N5) connected with PMOS transistors P3 and P4 to form a transmission gate. This transmission gate acting as a bi-directional switch, is used to

control gate signals and allows or rejects a signal toward the output improving both delay and power efficiency compared to CCVLSA [12], [13]

The dual switch current latch sense amplifier (DSCLSA) [14], designed to reduce power consumption and eliminate leakage current, is depicted in Figure 1(f). The circuit is composed of six PMOS transistors (P2, P3, P4, P5, P6, and P7) and five NMOS transistors (N1, N2, N3, N4, and N5). The bit line inputs BL and BLB are connected to column bit lines, and the SA includes a cross-coupled inverter for full swing at the output. The bit lines operate the gates of N3 and N4. Precharge transistors P2, P5, P6, and P7 are activated when (EN) is "1," turning off when transistor N5 is turned "ON." As N3 and N4 have different channel currents, either Vout or VoutB responds faster, and cross-coupled inverters set this difference. The dual switch and reduced leakage current result in decreased energy consumption and increased speed.

The dual voltage dual tail level restoration voltage latch sense amplifier (DVDTLR-VLSA) in Figure 1(g), featuring two sleep transistors, is presented in the paper. The schematic design of the SA includes ten transistors, similar to the double switch cross coupled VMSA, with two additional PMOS transistors, M1 and M2. The circuit is divided into two sections connected to Vdd. The DVDTLR-VLSA amplifies the bit-line voltage difference, using level restoration circuits common in MOS logic designs to provide a low-to-high valid logic level of voltage swing in response to a low swing input signal. The dual voltage with swing restoration logic is employed [15]. When EN is "1" and ENB is "0," enabling transistors M8 and M5 turn "ON." Assuming (BLB = "0") and (BL = "1") and the sleeping transistor is turned "OFF." When the EN signal and BL are high, Vout follows BL. Similarly, when ENB is active low and BLB is high, the output VOUTB responds in accordance with BLB.

3. METHOD

3.1. MTCMOS

MTCMOS logic serves as an effective technique for controlling standby leakage, but its implementation poses challenges due to the dependence of sleep transistor sizing on the discharge pattern within the circuit block as shown in Figure 2. To address this issue, dual Vt domino logic has been proposed as an alternative, mitigating the sizing difficulties and inherent performance concerns associated with MTCMOS. In proposed design transistor N5 and P5 designed for high threshold. In this approach, high Vt cells are strategically employed in areas where leakage must be minimized, while low Vt cells are utilized in regions where speed is a primary consideration. Both types of cells are judiciously integrated within the MTCMOS technique. During active operation, the high Vt transistors are turned off, allowing the logic gates comprised of low Vt transistors to function with reduced switching power dissipation and smaller propagation delay. In standby mode, the high Vt transistors are deactivated, effectively disconnecting the internal low Vt circuitry and preventing unnecessary leakage. This dual Vt approach thus overcomes the challenges associated with sleep transistor sizing in MTCMOS, offering an efficient solution for both active and standby modes of operation [16]. When the circuit work in active mode, high threshold voltage transistors are utilized to achieve high speeds and better performance.

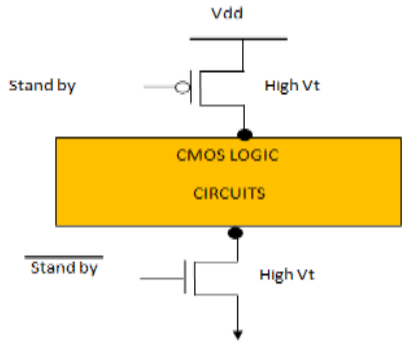


Figure 2. MTCMOS logic

3.2. Proposed design

The design of the dual supply latched sense amplifier (DVLSA) is illustrated in Figure 3. This voltage SA adopts a latch-type configuration, integrating strong positive feedback with a high-resistance input. The flow of current through the differential input transistors, N3 and N4, governs the serially

connected latch. It is imperative to ensure that the latch is in a meta-stable state before the reading process, as this stage is critical to the functioning of the latch-type SA.

The high gain positive feedback SA is realized through the actions of transistors P2, P3, N1, and N2. Meanwhile, transistors N3 and N4 function as a differential amplifier. P6 and P7 are employed to connect the bit lines to Vdd, and transistor N5 is used to enable the SA. During the sensing phase, after precharging the bit lines to Vdd, the EN signal is elevated to turn on N5, consequently driving N3 and N4 to operate as a common source differential amplifier. Transistors P2, N1, P3, and N3 then amplify the small voltage difference to achieve full swing at the output node.

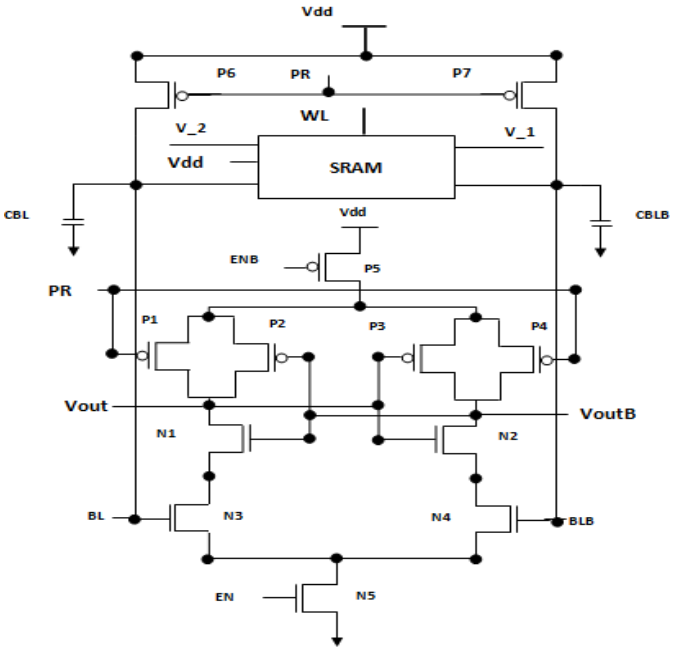


Figure 3. Proposed design

As inputs are fed into the differential amplifier, it detects the small voltage difference of the bit lines and amplifies it. The strong positive feedback at the output stage and the presence of a differential amplifier at the input stage collectively enhance the performance of the latch-type SA. Upon completing the latching process, the SAis turned off preventing any current flow and thereby reducing power dissipation. The application of the MTCMOS method can further improve the speed of the SA. When EN is "1" and ENB is "0," enabling transistors M8 and M5 turn "ON." Assuming (BLB = "0") and (BL = "1") and the sleeping transistor is turned "OFF." When the EN signal and BL are high, Vout follows BL. Similarly, when ENB is active low and BLB is high, the output VoutB responds in accordance with BLB. Transistor N5 and P5 work as high threshold transistor in MTCMOS low power technique. It is used for reducing power dissipation and increase speed of operation. CBL and CBLB used for charging and discharging in the SRAM circuits.

4. PERFORMANCE ANALYSIS

This section delves into the examination of simulated results for the proposed SA. When the enable (EN) signal and bitline (BL) are both high, the output Vout mirrors the state of BL. Similarly, when ENB is active low and BL is high, the output VoutB aligns with the state of BLB.

As inputs are applied to the differential amplifier, it detects the small voltage difference between the bit lines and amplifies this discrepancy. The incorporation of strong positive feedback at the output stage and a differential amplifier at the input stage significantly enhances the performance of the latch-type SA. Upon completion of the latching process, the SA is turned off, preventing any current flow. Consequently, both dynamic and static power dissipation are reduced, contributing to an overall reduction in power consumption.

This section provides a comparative performance analysis between the proposed SA and various existing SAs. The primary focus of VLSI industry designs centers on key factors such as speed, delay, and power. The paper is summarized with an emphasis on the design extent to evaluate stability within these

parameters, as highlighted in references [17], [18]. The importance of achieving low power consumption is underscored, especially in the context of portable devices, as indicated in reference [19].

4.1. Energy and power performance

Power consumption stands out as a critical parameter for overall VLSI circuits. Given the growing demand for low-power circuits, there is a notable surge in research dedicated to reducing power consumption in SA [20]. A comparative energy analysis is illustrated in Figure 4.

4.1.1. Power dissipation

- Static power dissipation: this action takes place when the circuit is not active. It means circuits behave in quiescent mode. Leakage power dissipation in CMOS is inversely proportional to the threshold voltage [21].

$$Ps = Vcc \times Icc \quad (1)$$

where Vcc is voltage applied to a logic circuit and Icc is static supply current:

- Dynamic power dissipation: when the CMOS circuit is in operation the power is consumed that is known as dynamic power consumption [22].
- Short circuit power dissipation: due to short circuit in CMOS logic this power dissipation takes place [23].
- Switching power dissipation: it is taking place due to the charge ad discharge of capacitors. Switching power dissipation (Psw) is given in (2):

$$Psw = \alpha \times (Vdd)2 \times C \times f \quad (2)$$

where α is switching activity
V_{dd} is supply voltage
C is total capacitances
f is the frequency of operation.
Figure 5 suggests that, among existing SAs, the proposed design exhibits both low energy and the lowest power consumption.

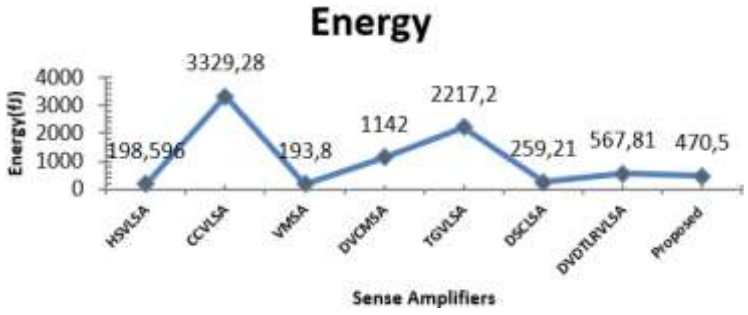


Figure 4. Energy of SA

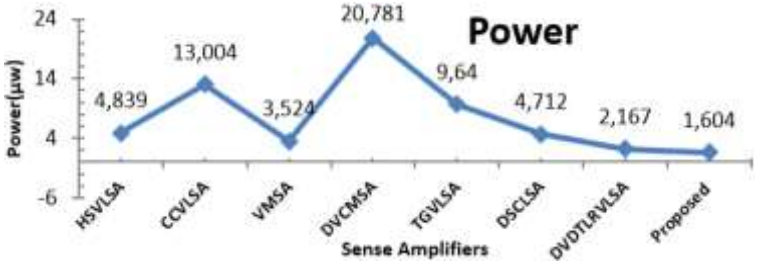


Figure 5. Power analysis of SA

4.2. Delay analysis

As the demand for high-speed circuits rises, the delay factor gains increased significance in VLSI circuits [24]. Figure 6 show the HSVLSA exhibits the least delay. However, considering other parameters, there appears to be a trade-off, as indicated in Table 1. The Table 1 shows the power dissipation, delay, energy, and average current values for all existing SA. Upon comparison, it is evident that the DVLSA stands out with the lowest delay and power values, making it the optimal choice [25].

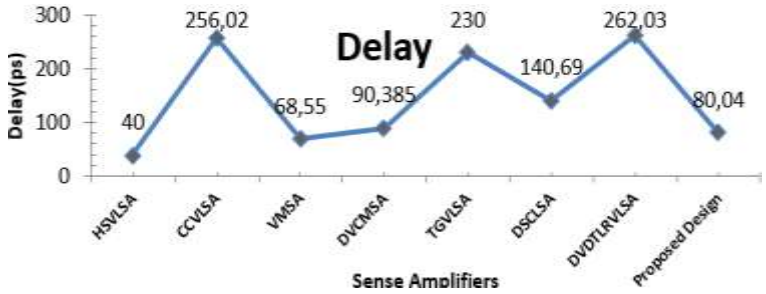


Figure 6. Delay of SA

Table1. Performance analysis of SA [10], [14]

S.N.	Sense amplifier	Power (µw)	Energy (fj)	Delay (ps)	Average current(µA)
1	HSVLSA	4.839	198.596	40	0.412
2	CCVLSA	13.004	3329.28	256.02	0.796
3	VMSA	3.524	193.8	68.55	0.080
4	DVCMSA	20.781	1142	90.385	1.022
5	TGVLSA	9.64	2217.20	230.00	2.504
6	DSCLSA	4.712	259.21	140.69	0.058
7	DVDTLRVLSA	2.167	567.81	262.03	4.873
8	Proposed design	1.604	470.50	80.04	5.406

4.3. Average current analysis

Figure 7 illustrates the comparative current analysis of different SA. It is evident that the HSVLSA exhibits the lowest current at 0.058 µA, while the proposed sense amplifier registers the highest output current. This discrepancy is attributed to the transistor sizing and the dual concepts employed in the design. Despite having the highest current, the SA design manages to achieve the least power consumption and energy utilization.

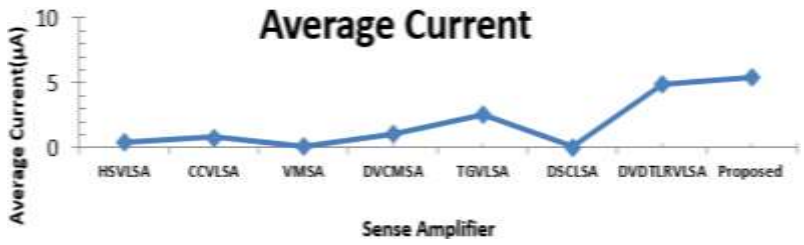


Figure 7. Average current of SA

5. RESULT

The proposed design simulated using CADENCE tool at 180 nm technology. Table 1 shows the comparative result analysis with various parameters of SA which reveals that proposed design has total power dissipation of 1.604 µw which is comparatively low to others while the no of transistor increases. Figure 8 show the transient response of proposed design. The proposed model also shows comparatively moderate energy 470.50 fJ, low delay 80.04 ps, and average current 5.406 µA, while power is low. Proposed designed is more superior in comparison to other types of SA.

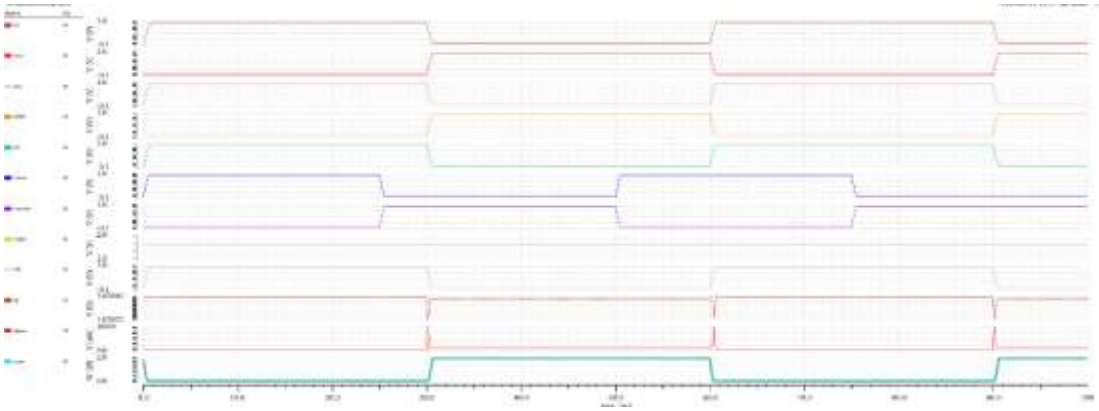


Figure 8. Output wave form of proposed SA

6. CONCLUSION

The study demonstrates the performance of upgraded SA and a DVLSA. The DVLSA is employed for high-speed and low power consumption integrated circuits. It is observed that the simulated result of proposed circuit design outperforms the others preexisting SA and it operates at the lowest power and delay. The proposed DVLSA exhibits a power consumption of 1.604 µW, showcasing notable improvements in current and delay results. This notably shows the performance improvement in comparison to existing SA. As in the case of SA without MTCMOS transistors, the power consumption of the amplifier circuit is increased. Thus, the proposed circuit design of DVLSA has been subjected to low power and high-speed.

APPENDIX

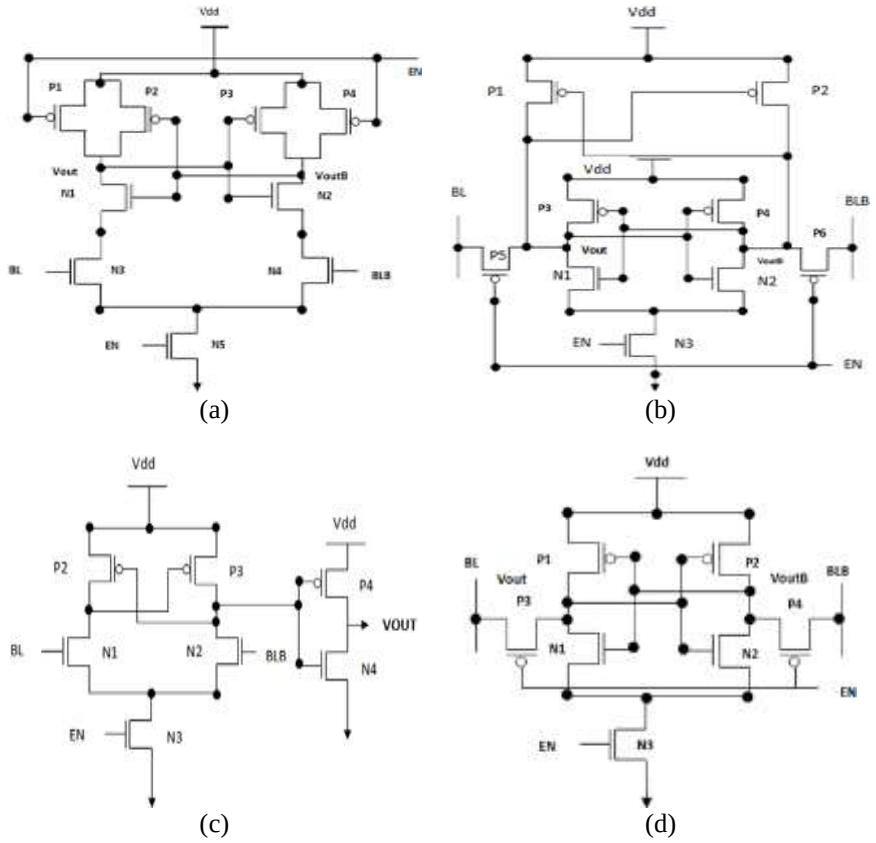
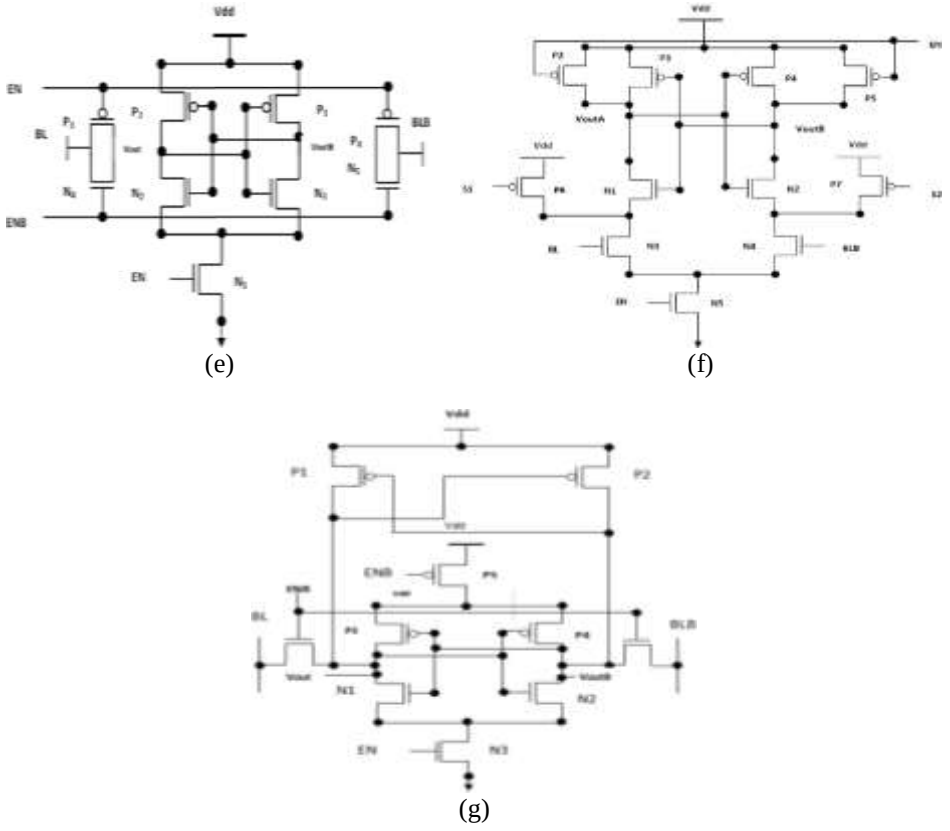


Figure 1. Schematic of various SA: (a) HSVLSA [9], (b) CCVLSA [9], (c) VMSA [10], (d) DVCMSA [10]



(e) (f) (g)

Figure 1. Schematic of various SA: (e) TGVLSA [9], (f) DSCLSA [10], and (g) DVDTLR-VLSA [15] (*Continued*)

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