

Hardware-realized secure transceiver for human body communication in wireless body area networks

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ABSTRACT

Wireless body area networks (WBANs), featuring wearable and implantable devices for collecting physiological data are increasingly critical in healthcare for enabling continuous remote monitoring, diagnostic improvements, and treatment optimization. Secure communication within WBANs is essential to protect sensitive health data from unauthorized access and manipulation. This paper introduces a novel secure digital (SD)-human body communication (HBC) transceiver (TR) system, tailored for WBAN applications, that prioritizes security and offers significant enhancements in size, power efficiency, speed, and data transmission efficiency over current solutions. Leveraging a combination of frequency-selective (FS) digital transmission with walsh codes (WCs) or quadrature amplitude modulation (QAM), and incorporating one-round encryption and decryption modules, the system complies with the IEEE 802.15.6 standard, ensuring broad compatibility. Specifically, the QAM-based SD-HBC TR system exhibits a 4% reduction in chip area, a 7.6% increase in operating frequency, a 3.4% decrease in power consumption, a 27.5% reduction in latency, and improvements of 33% in throughput and 35.5% in efficiency. Importantly, it achieves a bit error rate (BER) of up to 10^{-8} , demonstrating high reliability across communication methods. This research significantly advances secure communication in WBANs, offering a promising approach for enhancing the reliability, efficiency, and security of healthcare monitoring technologies.

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1. INTRODUCTION

Healthcare sensors were primarily employed in hospitals and laboratories in the past. This is altering due to the rise of affordable, potent, and cost-effective integrated gadgets that can be coupled into body area networks (BAN). With the help of these recently developed wearable sensors, residents may monitor their long-term wellness in open spaces through their regular activities. The provision and observation of healthcare could be significantly enhanced through wireless body area networks (WBANs), which are currently the subject of intense development and research efforts [1]. WBANs are primarily used with healthcare and social equipment that needs interconnected data, like health information. Many of these gadgets use short-range wireless communication requirements or those that operate within a few meters of the body. Since the human body collects high-frequency electromagnetic (EM) radiation within the 315 MHz to 2.4 GHz range, it is typically thought of as a barrier to communication via wireless technology [2]-[4].

Body-coupled communication (BCC) is called human-body communication (HBC). It is a system that eliminates the need for cables and radio frequency (RF) technology by using the human body as a medium for the transmission of electric fields [5]. An RF signal that travels into the human body in the near-field electric field or the surrounding quasi-electrostatic field in HBC facilitates the interaction between devices. Galvanic or capacitive coupling techniques are frequently employed to convey data through the human body. The electric field within the human body and the current passing through it contribute to transmission in both forms of HBC, but precise transmission modeling is still challenging [6]. The BCC or HBC can address problems with WBAN security, privacy, and EM radiation [7], [8].

The secure digital (SD)-HBC transceiver system using Walsh codes (WCs) and QAM approaches is designed in this manuscript. The proposed work offers low latency and high throughput with secured features suitable for WBAN applications. The contribution of the proposed work is highlighted as follows: The work introduces the quadrature amplitude modulation (QAM) approach in the frequency-selective (FS) spreading unit to improve the latency and data rate of the HBC system. The work introduces one-round encryption and one-round decryption as security algorithms in HBC to enhance the security features. The HBC using WCs is also designed and compared with the QAM approach. The performance comparison of proposed designs with recent HBC works is discussed with better improvements. The manuscript's organization is as follows: Section 2 discusses the current work of the HBC and its performance analysis. The SD-HBC TR system and its working operation are explained in detail in section 3. The simulation, performance, and comparative results are discussed in detail in section 4. Section 5 concludes the overall work with improvements.

2. RELATED WORKS

The recent works on the HBC system using different approaches for different applications are discussed in this section. Ando *et al.* [9] present the myoelectric signal-based wideband HBC to control the artificial robotic hand. The TX and RX modules are placed and communicated via artificial hand. The myoelectric signals operate in a 10 to 50 MHz frequency band. The myoelectric signals are detected at the RX end with a distance of 30 cm and a data rate of 1.25 Mbps. Lee *et al.* [10] describe the decision feedback equalization (DFE) based body channel communication system. The 8-tap DFE is deployed to compensate for the body channel's intersymbol interference (ISI). The system achieves a data rate of 150 Mbps and 10 Mbps for distances of 20 cm and 100 cm, respectively, in the body channel. Vale-Cardoso *et al.* [11] explain the HBC-based electronic system. The system has a direct current (DC) to DC converter, active common-mode rejection, an amplifier, and a low-pass filter (LPF). The system uses an on-off-keying (OOK) modulation approach with a frequency of 10 kHz. The system obtains a data rate of 11.11 kbps, a bit error rate (BER) of 10^{-4} , and consumes a power of 661.47 mW. Čuljak *et al.* [12] discuss the open challenges of ultra-wideband (UWB) and intrabody communication (IBC) systems concerning WBANs. The work analyzes the IEEE standards of 802.15.4a and 802.15.6 in detail with current works. Wideband signaling (WBS) applications are discussed in detail with emerging approaches. Chowdhury *et al.* [13] describe the various multi-integrating RX (MIR) front-end modules for lossy band-band channels (LBC)—the channels like HBC, body communication, and proximity communication—as LBCs for analysis purposes. The work analyzes the data rate, channel loss, energy efficiency, gain improvement, and BER for MIR modules under various LBCs.

Rahaman and Dyo [14] present human motion direction tracking on commodity wireless networks. The model uses convolutional neural networks (CNNs) to detect wireless directions. The impact of the filter size and wireless links concerning the time and accuracy of CNN configuration is discussed. The work achieves 88–92% accuracy based on the indoor environment and wireless links. Liao *et al.* [15] explain HBC-based signal transmission and path loss analysis. The electroencephalogram (EEG) signals are considered for transmission from the human wrist in HBC with a frequency band of 10 to 60 MHz. The HBC TR uses multiple pulse position modulation (MPPM) approaches and achieves a data rate of up to 20 Mbps with a BER of 10^{-3} . Sasaki and Ban [16] discuss the secure HBC, which is designed using the near neighbor classification (NNC) approach with binary channel states. The work analyzes the channel gain at different channel states. The k-NNC evaluates the channel states and observes the error rate. Iguchi *et al.* [17] explain the myoelectric signals with wireless control for wearable robots using HBC. HBC uses the MPPM approach, obtains a data rate of up to 20 Mbps, and covers up to 110 cm. Krimi *et al.* [18] describe modeling EM waves in biological tissues for WBANs. The work analyzes the path loss, propagation, and power loss density (PLD) in different communication scenarios. Ramaswamy and Gandhi [19] present trust-based data communication in WBAN for health applications. The work analyzes network specification, trust computation, node trust, and data trust. The throughput, packet delivery ratio, end-to-end delay, and node detection at different trusts are realized. Vizziello *et al.* [20] discuss HBC-based channel characterization using measured impulse response. The galvanic coupling (GC) and capacitive coupling (CC) approaches enable body-area transmission using wires. The work analyses the channel responses (impulses and

Frequency), mean amplitude, and peak-to-peak amplitude at different implanted scenarios. Nataraju *et al.* [21] provides an overview of the advancements in WBAN technologies and highlights the limitations of RF wireless technology in BANs. It introduces human body communication (HBC) as an alternative wireless communication technology that utilizes the human body as the signal transmission medium.

3. METHOD

The HBC transceiver system architecture is designed per IEEE 802.15.6 Standard specifications [22] with additional security features. The HBC TR System has a transmitter (TX), the human body acts as a channel, and receiver (RX) units. The HBC TR System is designed using two different approaches, namely: FS digital transmission (FSDT) using WCs and QAM. The secured digital (SD) HBC TR system architecture is illustrated in Figure 1.

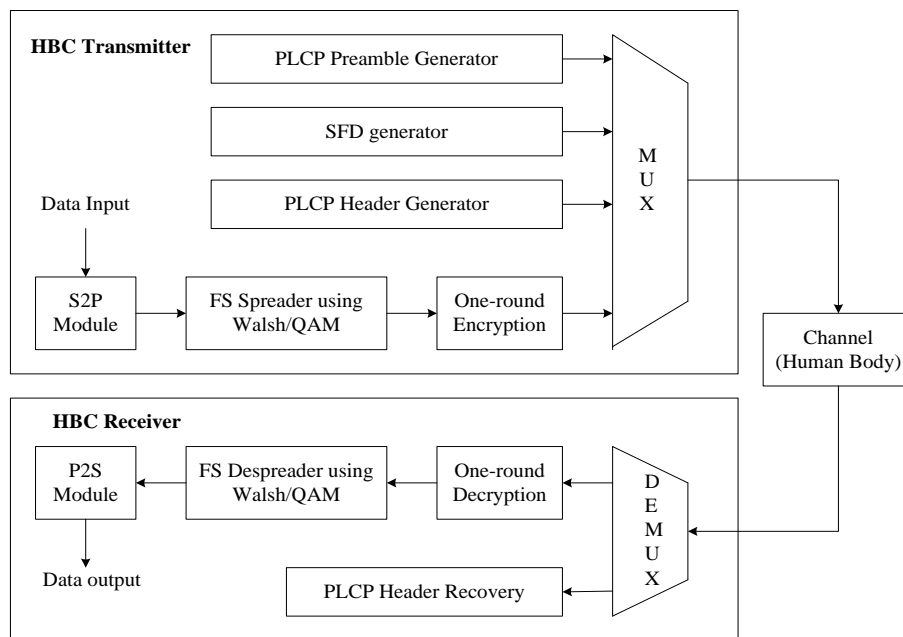


Figure 1. SD-HBC transceiver system architecture

The HBC TR unit is constructed using four significant components, namely: a physical layer convergence protocol (PLCP)-based preamble generator, a start of frame delimiter (SFD), a PLCP header, and a physical layer (PHY) service data unit (PSDU). The PLCP-based preamble generator generates the preamble sequences using gold code (GC) sequences and frequency shift codes (FSCs). The two 32-bit GCs are concatenated to form a 64-bit GC. The four 64-bit GCs are further concatenated to form a 256-bit GC sequence. This 256-bit sequence is multiplied with FSCs to form the 264-bit PLCP preamble sequence. The 80-bit SFD is constructed using FSCs and two predefined SFD constant values. The construction and operation of the SFD are similar to those of the PLCP Preamble Generator. In this work, the rate indicator is not considered to form the SFD. The primary 32-bit PLCP header with media access control (MAC) combines the 16-bit header, 8-bit address, and 8-bit cyclic redundancy check (CRC). The 16-bit PLCP header has a 3-bit data rate, 3-bit pilot insertion bits, 1-bit burst mode information, 1-bit seed, and an 8-bit reserve red bit for future use. The 8-bit CRC is generated using a linear feedback shift register (LSFR) with a polynomial of $x^8 + x^7 + x^3 + x^1 + 1$.

The PSDU collects the data from the HBC TX interface via first-in-first-out (FIFO) and is constructed using two design approaches: FSDT using WCs and QAM. The Serial to Parallel Module collects the 1-bit data from the FIFO interface and converts it to 4-bit parallel data using a shift register. The frequency selective (FS) spreader (FSS) is constructed concerning the WCs/QAM approach and FSCs. The 4-bit parallel data is replaced with WC or QAM data, and their results are multiplied with FSCs to form the 24-bit FSS output. The WC generation for FSS is tabulated in Table 1. QAM generation is illustrated in Figure 2. The QAM provides in-phase (I) and quadrature-phase (Q) data. The Q and I data are concatenated to form 16-bit QAM output. The one round encryption (ORE) module receives 24-bit FSS output as input,

performs encryption operations using a 24-bit key, and generates the 24-bit cipher text. The preamble, SFD, header, and cipher text input the multiplexor (MUX) module. The 2-bit mode input acts as a select line for the MUX module. If the mode is "00," then preamble, "01" for SFD, "10" for header, and "11" for data information. The MUX output is mixed with channel's additive white Gaussian noise (AWGN) noise to form the corrupted data. The human body acts as a channel in this work.

Table 1. WC generation for FS spreader

In	Out	In	Out
0	FFFF	8	FF00
1	AAAA	9	AA55
2	CCCC	10	CC33
3	9999	11	9966
4	F0F0	12	F00F
5	A5A5	13	A55A
6	C3C3	14	C33C
7	9696	15	9669

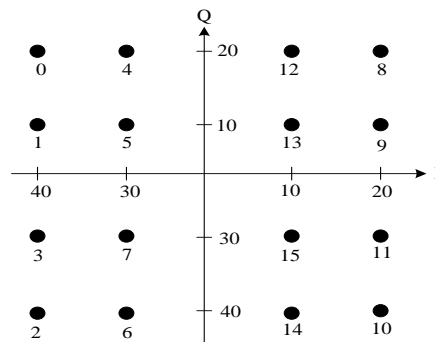


Figure 2. QAM generation

The HBC RX receives the corrupted data and segregates the data and header information using the same 2-bit mode signal. The data information is passed to one round of the decryption (ORD) module, and header information is passed to PLCP header recovery. The ORD module produces the decrypted data using the same 24-bit key. The FS-Despreader receives the 24-bit decrypted data and performs a despreading operation using WCs or QAM. The parallel to serial (P2S) module receives the 4-bit FS-Despreader output and produces the 1-bit serial output. The received 1-bit data and input data must match to validate the HBC TR system and also help to evaluate the BER. The HBC TX and RX units are designed with proper clock synchronization, which helps to realize the HBC TR system's latency, throughput, efficiency, and BER using both WCs and QAM approaches.

3.1. One round encryption and one round decryption

The ORE is one of the most straightforward approaches to offering the security feature to low-resource-constrained devices. The ORE is flexible to design for standard data (32/64-bits) and key sizes (32/64/96/128-bit). This work considers the 24-bit data and 24-bit key sizes for ORE and ORD operations. The ORE and ORD modules use combinational logic and are executed in parallel. The ORE/ORD produces the encrypted or decrypted output on the same cycle, which helps to improve the latency and performance of the HBC TR system. The encryption and decryption processes are illustrated in Figure 3. Figures 3(a) and 3(b) illustrate the ORE and ORD working operations. The ORE/ORD modules are constructed in a Feistel network (FN) structure and are operated in parallel. The 24-bit data and key are decomposed into two 12-bit (P1 and P2) and key (K1 and K2) units. The ORE/ORD module has four substitution units and performs six XOR operations. The two initialization vectors (IV1 and IV2) are considered and predefined. The substitution unit is constructed using Sbox and tabulated in Table 2. The 4-bit input data is replaced with Sbox data in the substitution unit. The reverse substitution unit uses the same Sbox, but input acts as output and vice versa. The ORE generates the two 12-bit cipher texts (C1 and C2), and the ORD generates the two 12-bit output texts (O1 and O2).

Table 2. Substitution box (Sbox) table

In	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Out	C	5	6	B	9	0	A	D	3	E	F	8	4	7	1	2

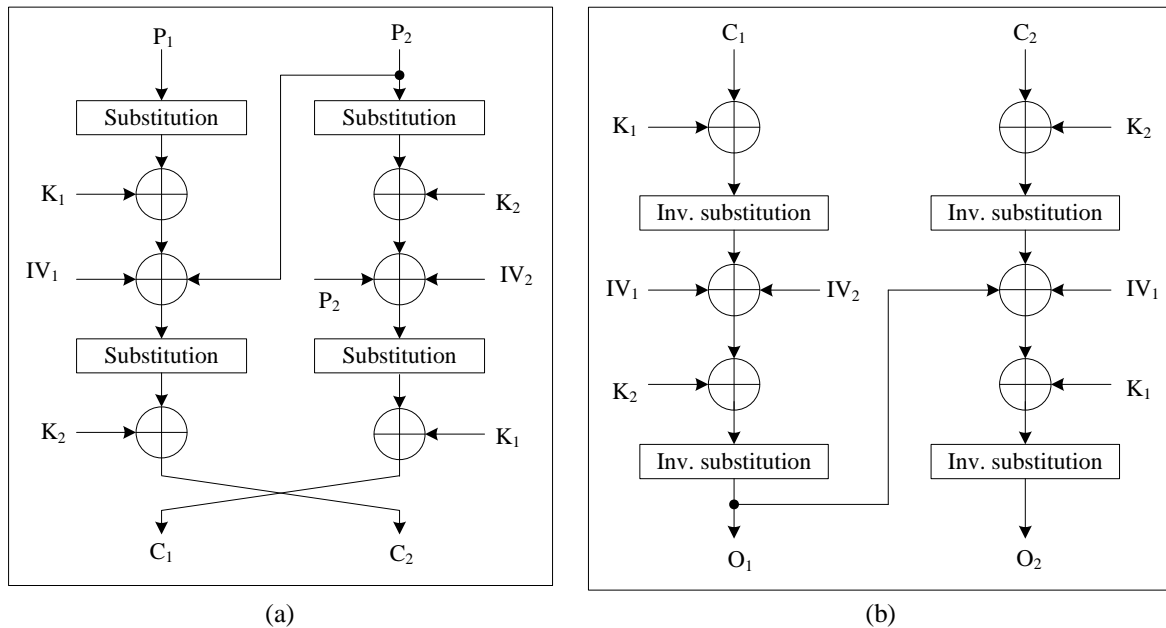


Figure 3. Encryption and decryption process (a) one round encryption and (b) one round decryption

4. RESULTS AND DISCUSSION

The detailed results of the SD-HBC TR system using WCs, or FSDT and QAM, are discussed in this section. The SD-HBC-TR using WCs and QAM is designed using Verilog HDL on the Xilinx ISE platform and implemented using the Artix-7 FPGA (Device: XC7A100T-5CSG324). The mentor graphics-based ModelSim Simulator verifies and visualizes the simulation waveform. The simulation results of the SD-HBC TR system are illustrated in Figure 4. The global clock (clk) is activated at 100 MHz with an active low reset (rst) to start the HBC process. The 2-bit mode signal is selected to "11" for the data transmission process with an active high enable signal. The 1-bit input (din) is generated randomly, the 8-bit PLCP header (plcp_in) is fixed to "ff," and the 24-bit key is defined as "012345". The 1-bit output (dout) is generated after the completion of the HBC process. Here, the delayed input is considered (delay_in), which is the same 1-bit input (din) with a delay to match the obtained output (dout). The error signal indicates low quality because the delayed input matches the obtained output. The total counter (total_cnt) counts the number of input bits transmitted during transmission.

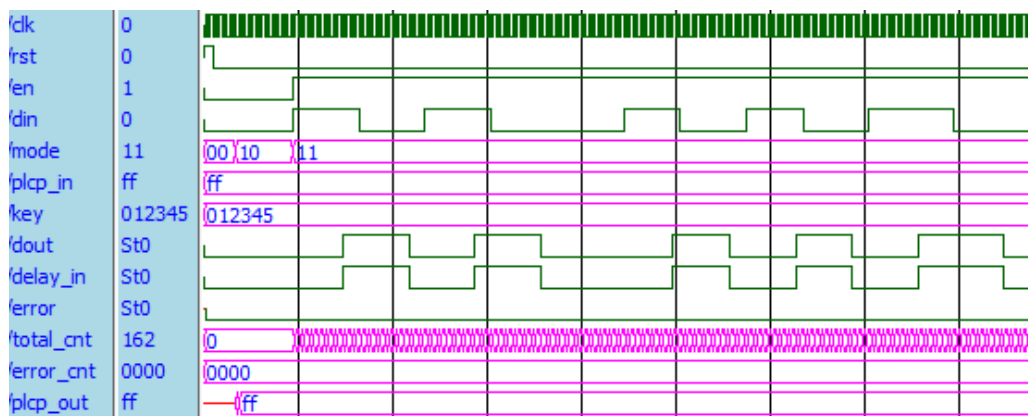


Figure 4. Simulation results of SD-HBC TR system

The performance of the HBC TR system using WCs and QAM approaches is realized using chip area utilization, and performance metrics are tabulated in Table 3. The chip area utilization contains slices, lookup tables (LUTs), LUT-flip-flops (FFs), and digital signal processing elements (DSP48Es). Metrics like latency in terms of clock cycles (CC), throughput (Mbps), and hardware efficiency (Kbps/slice) are considered for performance realization.

Table 3. Performance analysis of SD-HBC TR using WCs and QAM

Resources	HBC TR using WCs	HBC TR using QAM
Slices	199	191
LUTs	1,229	1,165
LUT-FF's	149	114
DSP48E1s	5	4
Max. frequency (MHz)	255.073	276.106
Total power (mW)	117	113
Latency (CC)	14.5	10.5
Throughput (Mbps)	17.6	26.3
Throughput (Mbps) at 100 MHz	6.9	9.53
Efficiency (Kbps/Slice)	88.44	137.69
Efficiency (Kbps/Slice) at 100 MHz	34.67	49.89

The HBC TR using WCs uses slices and LUTs of < 1% and operates at 255.07 MHz, consuming a total power of 117 mW. Similarly, the HBC TR using QAM uses slices and LUTs of < 1% and operates at 276.1 MHz, consuming a total power of 113 mW. The HBC TR using WCs considers 14.5 CC as latency, a throughput of 17.6 Mbps, and an efficiency of 88.44 Kbps/slice. Similarly, the HBC TR using QAM uses only 10.5 CC as a latency, a throughput of 26.3 Mbps, and an efficiency of 137.69 Kbps/slice. Generally, most of the HBC TR system operates in the 100 MHz frequency range. So the HBC TR using WCs and QAM obtains a throughput of 6.9 Mbps and 9.53 Mbps, respectively. The representation of the resource utilization of SD-HBC TR and its sub-modules is shown in Figure 5. The SD-HBC TR using QAM reduces chip area in terms of slices by 4%, LUTs by 5.2%, and DSP48E1s by 20%, operating frequency by 7.6%, and power by 3.4% compared to the SD-HBC TR using WCs. The performance metrics of the SD-HBC TR using QAM improve latency by 27.5%, throughput by 33%, throughput by 27.5% at 100 MHz, and hardware efficiency by 35.5% compared to the SD-HBC TR using WCs.

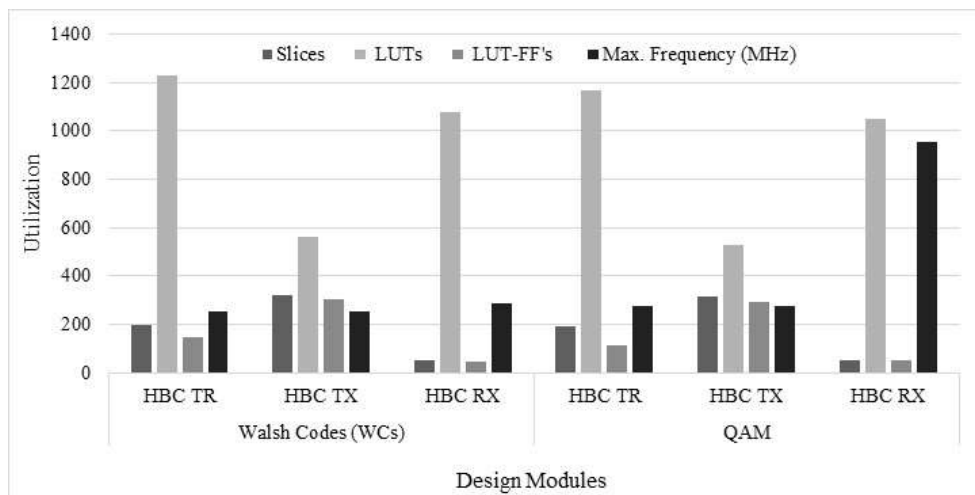


Figure 5. Resource utilization of SD-HBC TR and its sub-modules

The performance realization of the proposed SD-HBC TR system using FSDT and QAM with the existing HBC TR system is tabulated in Table 4. The design approach, technology, operating frequency band, core voltage, support security feature, data rate (Mbps), and BER parameters are considered for performance comparison. The complementary metal-oxide semiconductor (CMOS)-based nanometer (nm) technology and frequency bands may vary depending on the design approach. The proposed work is adaptable to any CMOS

technology and operating frequency. The proposed work added a security algorithm to improve confidentiality and restrict unauthorized access. The proposed HBC-TR system using QAM improves the data rate by 86%, 44.9%, 79%, and 79% compared to the existing HBC TRs [23]-[27], respectively. In contrast, the proposed HBC-TR system using FSDT also provides a better data rate than existing HBC systems. The proposed HBC-TR system using FSDT and QAM approaches reduces the BER by 50%, 12.5%, 25%, 62.5%, and 62.5% compared to the existing HBC TRs [24]-[28], respectively.

Table 4. Performance realization of the proposed work with the existing HBC system

Ref	[23]	[24]	[25]	[28]	[26]	[27]	Our work	our work
Approach	FSDT	FSDT	FSDT	NRZ	Autoencoder	FSK	FSDT	QAM
Technology (nm)	130	65	90	65	45	90	28	28
Frequency Band (MHz)	42	21	8 to 22	30	42	60	25 to 100	25 to 100
Core Voltage (V)	1.1	1.2	1.2	1	1.2	1.2	1	1
Security feature	No	No	No	No	No	No	Yes	Yes
Data rate (Mbps)	1.3125	5.25	2	30	5.25	2	6.9	9.53
BER	10^{-4}	10^{-7}	10^{-6}	10^{-3}	10^{-3}	$< 10^{-8}$	$< 10^{-8}$	$< 10^{-8}$

The performance comparison of the proposed designs with existing HBC designs on the FPGA platform is tabulated in Table 5. The HBC system using FSDT [29] is designed on an Artix-7 FPGA and operates at 32 MHz by obtaining a BER of 10^{-6} and a data rate of 6 Mbps. The proposed HBC using QAM utilizes fewer LUTs by 77%, improves the frequency by 89%, BER by 25%, and data rate by 37%. The HBC system using the WBS approach [30] is designed on a Virtex-2 FPGA and operates at 100 MHz by obtaining a BER up to 10^{-8} and a data rate of 3.125 Mbps. The proposed HBC using QAM utilizes fewer slices by 97%, LUTs by 779.9%, improves the frequency by 63%, reduces the power by 28.4%, and reduces the power by 28.4% and the data rate by 54.7%. The HBC system using FSDT [31] is designed on an Artix-7 FPGA and operates at 255.31 MHz by obtaining a BER up to 10^{-4} and a data rate of 9.52 Mbps. The proposed HBC using QAM utilizes fewer slices by 2.55%, improves the frequency by 7.6%, BER by 50%, and data rate by 0.1%. Overall, the proposed HBC system using FSDT and QAM methods offers better BER and data rate with security features than existing HBC systems.

Table 5. Performance comparison of the proposed designs with existing HBC works on FPGAs

Resources	[29]	[30]	[31]	Our work	Our work
Approach	FSDT	WBS	FSDT	FSDT	QAM
FPGA used	Artix-7	Virtex-2	Artix-7	Artix-7	Artix-7
Security feature	No	No	No	Yes	Yes
Slices	NA	6649	196	199	191
LUTs	5231	5272	1137	1229	1165
Frequency (MHz)	32	100	255.31	255.073	276.106
Power (mW)	113	158	101	117	113
BER	10^{-6}	$< 10^{-8}$	$< 10^{-4}$	$< 10^{-8}$	$< 10^{-8}$
Data rate (Mbps)	6	3.125	9.52	6.9	9.53





5. CONCLUSION

In this manuscript, we present a novel SD-HBC transceiver system designed for WBAN applications. The system leverages both WCs and QAM for communication while adhering to the IEEE 802.15.6 standard and integrating robust security measures. Implemented on the Artix-7 FPGA platform within the Xilinx ISE environment, the system prioritizes security for sensitive health data while achieving significant improvements in size, power consumption, speed, and data transmission efficiency compared to existing solutions. Our analysis revealed that the QAM-based HBC TR system outperforms the WC-based approach in terms of latency (27.5% improvement) and throughput (33% improvement). Additionally, it demonstrates superior performance against existing HBC systems in latency, throughput, and BER. These advancements position the QAM-based SD-HBC TR system as a promising candidate for next-generation WBANs, enabling more reliable, efficient, and secure healthcare monitoring. Future endeavors will focus on integrating the proposed HBC TR system with an analog front-end module. This integration will bridge the gap between theoretical design and real-world application, allowing for the validation of real-time performance metrics and further solidifying the system's potential for practical healthcare deployments.





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