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A high efficiency boost converter topology with least component count

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ABSTRACT

This paper presents a design and analysis of novel DC-DC boost converter with a least component count. The proposed converter produces high DC gain voltage in comparison to some recently presented high voltage DC-DC converter. Here one switch, one inductor, two capacitors and one diode are used to achieved a high voltage gain without compromising efficiency of converter. The converter's performance is evaluated using theatrical, simulation and experimental methods, with results indicating a four times of input voltage and a fast-transient response at various duty cycles is achieved. Due to its low component count the proposed converter is compact and hence it offers an effective solution for various power applications.

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1. INTRODUCTION

In recent years, with demand for high-power application need for efficient DC to DC boost converters, providing compact and effective power solutions. The DC-DC converters are commonly categorized into two types: isolated converters and non-isolated converters. "The isolated configurations are preferred for high-power applications where efficiency required is high, while non-isolated topologies are commonly employed in low to medium power scenarios where efficiency and electromagnetic interference (EMI) considerations are not significant concerns" [1]. To enhance the performance of converters much modification and research are done by researchers. In general, "the conventional boost converter is employed for increasing voltage within the non-isolated DC-DC converter family. Normally, it requires a high duty cycle to produce the desired high output voltage" [2]. "To enhance conversion efficiency and achieve high voltage gain, advancements in step-up converters include the integration of switched capacitor and coupled inductor techniques" [3], "utilization of voltage doubler configurations" [4], "adoption of diode-capacitor setups" [5], and "implementation of voltage lift methodologies" [6]. Additionally, the development of "Cuk converters, single ended primary inductor converters (SEPIC), and ZETA converters" aims to generate high DC voltage outputs. However, these approaches often encounter challenges such as elevated stress across switching devices and diminished efficiency. Operational limitations arise at very high duty ratios due to increased conduction losses stemming from parasitic resistances and voltage gain decreases. Consequently, "high-gain DC-DC converters employing multiple inductors and capacitors are being explored to augment the converter's gain" [7]. Notably, a proposed solution in [8] introduces "a single-switch modified SEPIC converter characterized by high voltage gain and low voltage stress".

Researchers have amalgamated various topologies, such as “the classical boost converter with the single ended primary inductor converter (SEPIC)” [9]-[11], the “integration of double boost with SEPIC” [12], the “fusion of boost with flyback converter configurations” [13], [14], and the “utilization of interleaved boost converters” [15], [16]. Coupled inductor topologies present significant benefits, including increased “voltage gain, improved efficiency, and decreased voltage and current stresses on switches”. However, a challenge associated with these topologies lies in “effectively managing the energy trapped in leakage inductance to prevent voltage transients across switch and improve overall circuit efficiency”. To address this issue, “additional clamped circuits” must be incorporated into these topologies [17]-[20], consequently increasing the complexity of the circuit design. “Multilevel DC-DC architectures employ multiple switched capacitors in the output stage to elevate the output voltage” [21]. Converters employing voltage “multiplier cell strategies effectively diminish voltage stress while enhancing high voltage gain. But the overall system size and cost are increased with several multiplier cell stages” [22]. “Various isolated and non-isolated configurations incorporate voltage multiplier cells (VMCs), which consist of switched inductors and capacitors, to boost the output voltage of the converter. Another advantage of VMC utilization is the attainment of high output voltage at lower duty ratios” [23]. “Quasi-Z source converters represent another family of DC-DC converters characterized by continuous input current and low stress across switching devices and capacitors. Nonetheless, these converters exhibit limited voltage gain and are unsuitable for operation at higher duty ratios” [24], [25]. Recent research explores “new and efficient topologies with high gain” [26], [27]. “Quadratic boost topologies offer the advantage of achieving very high gain ratios at low duty ratios. Low duty ratio operation reduces the stress across devices and improves the efficiency of the converter” [28]. The “Non-isolated quadratic boost converter delivers high gain while reducing stress on switches” [29]-[31]. Although the topology in [8] offers “less gain” compared to the proposed in [32], it employs “four inductors and a total of 14 components”. An “ultra-high gain boost converter” is proposed in [33], requiring 12 components, yet its “gain is inferior” to that of topology [32]. Observations indicate that topology [34] exhibits “the highest voltage gain within the duty cycle range of 0.1 to 0.65. Achieving a voltage gain of over 10 times is feasible by operating the converter at a 0.5 duty cycle”. Conversely, the topology in [35] yields “lesser gain” than [34] despite employing four inductors and two switches. The “switched capacitor topology” proposed in [36] surpasses the gain of topology [35] but falls short of that in [34]. The “switched inductor topology converter” introduced in [37] demonstrates marginally “higher gain” than the [34] converter for $D > 0.65$, yet its practical implementation is challenging due to the requirement of 8 inductors, 4 switches, and 17 diodes. “Quadratic boost topologies” in [28] and [37] incorporate three inductors akin to topology [34], albeit yielding significantly lower gain. Voltage stress across switch S1 is notably lower compared to other topologies, except for the one proposed in [31]. Voltage stress across S2 is twice that of S1 but remains lower compared to other topologies, except for [31], [33], and [36].

This study investigates the effects of integrating a capacitor in parallel with conventional converter inductor to enhance voltage gain without excessively increasing component count. While earlier studies have explored various methods to improve voltage gain, they have not explicitly addressed the potential of integrating capacitors in parallel with inductors to achieve this goal. The primary objective of this research is to develop a novel converter topology with the least component count, ensuring higher efficiency and faster transient response compared to existing designs, while maintaining reliability and stability across different operating conditions. The paper is structured as follows: section 2 outlines operational modes of proposed converter, section 3 details the steady-state analysis of proposed converter, section 4 presents simulation and experimental results along with discussion, and section 5 provides the conclusion of the paper.

2. THE PROPOSED CONVERTER

The boost converter proposed here integrates a single switch, one inductor, two capacitors, and one diode, as depicted in Figure 1. This design innovation introduces a parallel capacitor alongside the inductor of a traditional converter, maintaining efficiency without compromise. Utilizing a single switch, the converter functions in two distinct switching modes: mode-I and mode-II, both operating within the continuous conduction mode (CCM). In mode-I, the switch S is turned “on,” allowing input voltage Vin flows equally through inductor and parallel capacitor with inductor via switch S, causing a current to flow through it. The inductor and parallel capacitor with inductor stores energy during this mode. During mode-II operation switch S is turn “off”, the diode acts forward-biased, diodes D1 starts conducting and allows the current from the inductor and capacitor to flow through it and into the output capacitor. The stored energy within inductor and capacitor is effectively transferred to output capacitor, resulting in a boosted output voltage surpassing input voltage level. Incorporating a capacitor in parallel with inductor of a conventional boost converter significantly enhances performance of circuit. The capacitor functions as a low-pass filter, effectively smooths input voltage, diminishing high-frequency noise and ripple. This improvement translates to reduced

voltage spikes and EMI emissions, thereby optimizing converter functionality. Table 1 presents the components specification for various duty cycles.

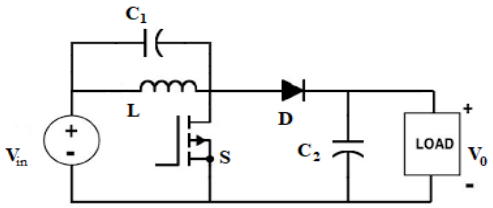


Figure 1. Proposed DC-DC boost converter topology

Table 1. Components specifications

Duty cycle	Components specification
0.2	L_1=200 uH,C_1&C_2=200 uF, P=2 Watt
0.3	L_1=90 uH, C_1&C_2=65 uF, P=20 Watt
0.4	L_1=60 uH, C_1&C_2=165 uF, P=5 Watt
0.5	L_1=50 uH, C_1&C_2=150 uF, P=9 Watt
0.6	L_1=120 uH, C_1&C_2=48 uF, P=3 Watt
0.7	L_1=30 uH, C_1&C_2=180 uF, P=9 Watt

3. MATHEMATICAL MODELLING OF PROPOSED CONVERTER

This section provides a comprehensive analysis of proposed boost converter's performance in CCM across various resistive loads. Initially examining the steady-state characteristics of converter, particularly focusing on parameters such as output voltage, input current, and duty cycle across varying load conditions to ensure stability and reliability. Subsequently, an efficiency analysis, quantifying losses across different components like the MOSFET, diode, and inductor to assess the converter's effectiveness.

The time period of converter is $T = T_{ON} + T_{OFF}$ and the switching frequency is $\frac{1}{T}$.

The duty cycle of boost converter is, $D = \frac{T_{ON}}{T}$.

The voltage across V_{C_1},

$$V_{in}D + \left(V_{in} - V_{C_1}\right)(1 - D) = 0$$
$$V_{C_1} = \frac{1}{1 - D}V_{in}$$

the voltage across V_{L_1},

$$V_{in}D + \left(V_{in} - V_{L_1}\right)(1 - D) = 0$$
$$V_{L_1} = \frac{1}{1 - D}V_{in}$$

the output current i_o and output voltage are:

$$i_0 = i_L + i_c$$
$$V_0 = V_{C_2} = V_{R+}i_0X\ (R//X_{C_2}) = (i_L + i_C)(R//X_{C_2}) = V_{C_1} + V_{L_1}$$
$$V_{C_2} = V_{C_1} + V_{L_1} = \frac{1}{1 - D}V_{in} + \frac{1}{1 - D}V_{in} = \frac{2}{1 - D}V_{in}$$

To find out efficiency of converter various losses need to evaluated. Among these, the power loss in the MOSFET is a critical consideration. This encompasses the total of static and dynamic loss. The static loss is the power dissipation resulting from the MOSFET's inherent characteristics and operating conditions, such as conduction losses due to finite on-state resistance and switching losses during the transition between on and off states. On the other hand, the dynamic loss is the MOSFET's switching behaviour and the associated dynamic processes occurring during transitions between on and off states of MOSFET which is mathematically given as:

$$P_{Static} = r_{ds_{on}}.{I_{rms}}^2$$
$$P_{Dynamic} = \frac{V_{in}.I_{out}}{3}$$
$$P_{MOSFET_{Loss}} = P_{Static} + P_{Dynamic}$$
$$P_{MOSFET_{Loss}} = r_{ds_{on}}.{I_{rms}}^2 + \frac{V_{in}.I_{out}}{3}$$

where, $r_{ds_{on}}$ and ${I_{rms}}^2$ are the on-state resistance and rms current flowing through MOSFET.

The power loss in diode given as:

$$P_{Diode_{Loss}} = V_F.I_{D_{Avg}} + r_D.I_{D_{rms}}^2$$

where, V_F, r_D and $I_{D_{Avg}}$ are forward voltage drop, forward junction resistance and average current flowing through the diode while it's in the on state.

The power losses in the inductor and capacitor are:

$P_{Capacitor_{Loss}} = ESR.I_{C_{rms}}^2$ and $P_{Inductor_{Loss}} = r_{Series}.I_{L_{rms}}^2$

where, ESR, $I_{C_{rms}}^2$,r_{Series} and $I_{L_{rms}}^2$ are equivalent series resistance, capacitor rms current, inductor series resistance and rms current passing through inductor.

The power loss within the converter is:

$$P_{loss} = P_{MOSFET_{Loss}} + P_{Diode_{Loss}} + P_{Capacitor_{Loss}} + P_{Inductor_{Loss}}$$

the efficiency of the converter is given as:

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}}$$

4. RESULT WITH DISCUSSION

The proposed converter reveals a strong correlation between duty cycle and output voltage, with consistently achieves higher output voltages in comparison to conventional converter. The simulation results depict output waveforms of both the conventional and proposed converters operating at a frequency of 25 kHz, as demonstrated in Figure 2. These simulations encompass a duty cycle range from 0.2 to 0.7, as illustrated in Figures 3 to 8. The simulations are conducted using a 12 V input voltage in the PSIM platform. Through these analyses, the behavior and performance characteristics of the converters are thoroughly examined across various duty cycle values. At 0.2 duty cycle, the conventional converter yields an output of 15 V as shown in Figure 3(a), while our proposed converter generates 27.5 V as shown in Figure 3(b), achieving steady-state response earlier. Similarly, at a duty cycle of 0.3, the output voltages are 18 V and 29.5 V for the conventional and proposed converters respectively, shown in Figures 4(a) and 4(b). Notably, at 0.4 duty cycle, the proposed converter reaches a gain voltage of 33.5 V, with saturation beginning at 2 msec shown in Figure 5(a), whereas conventional converter with 20 V gain fails to demonstrate steady-state response even after 4 msec shown in Figure 5(b). For 0.5 duty cycle shown in Figure 6(a) gain voltage for proposed converter is 35 V with the used of one extra capacitor with conventional converter and fast steady-state response is achieved without oscillation whereas for conventional converter gain is 24 V as shown in Figure 6(b). At a 0.6 duty cycle, with proposed converter a gain of 45 V with fast response is obtained as illustrated in Figure 7(a) whereas for conventional converter achieves a gain of 30 V with saturation after 8 msec as shown in Figure 7(b). Further enhancements are observed with the proposed converter, such as at 0.7 duty cycle gain of 48 V is achieved as illustrated in Figure 8(a) whereas for conventional converter gain is 40 V as shown in Figure 8(b). The incorporation of a resonant circuit in the proposed converter, featuring a parallel capacitor with an inductor, facilitates higher gain, stability, and steady-state output. This resonant circuit exhibits peak response, enhancing converter performance by enabling more efficient energy transfer. The simulation results, depicted in Figure 9(a), illustrate the gain versus duty cycle for both conventional and proposed converters, with proposed converter achieving a gain of 4 at 0.7 duty cycle, compared to 3.3 for the basic converter. Furthermore, Figure 9(b) provides a comparison of theoretical, simulation and experimental outcomes of proposed converter, showcasing its performance in terms of gain versus duty cycle.

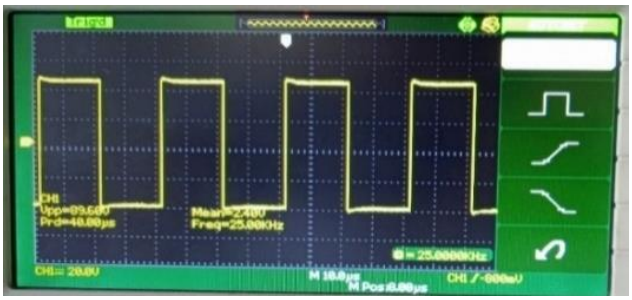
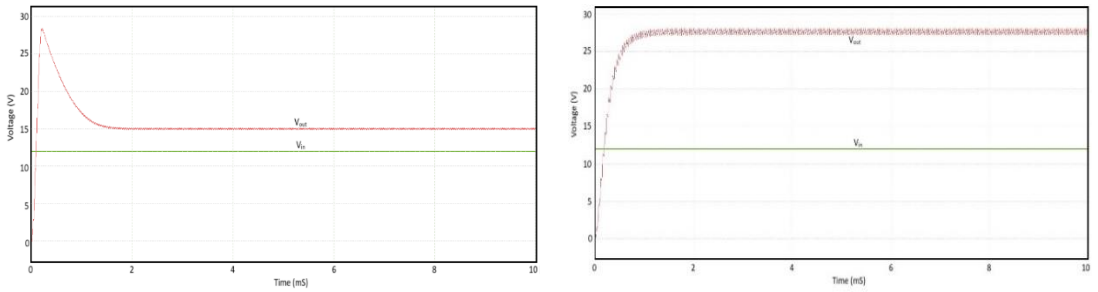
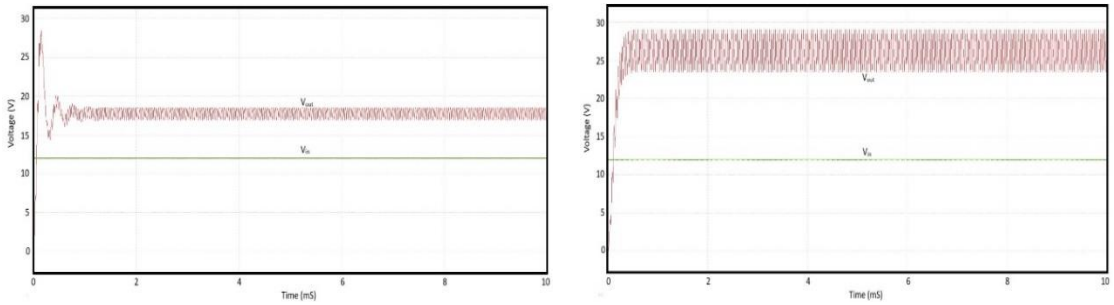


Figure 2. Gate triggering PWM signal



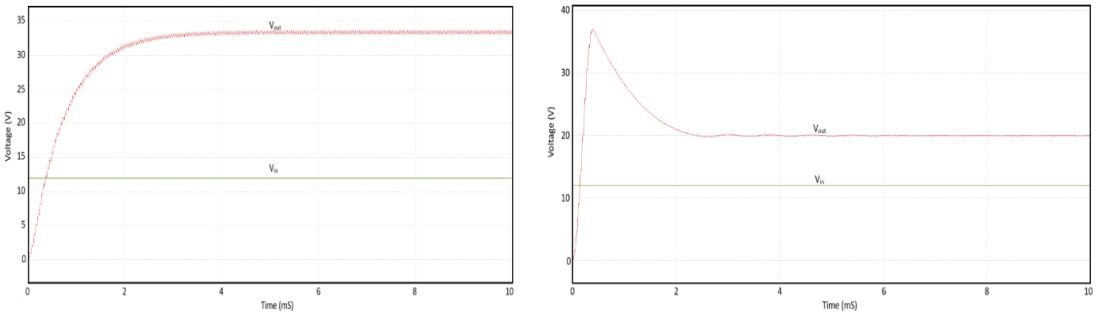
(a) (b)

Figure 3. Output waveform at 0.2 duty cycle (a) conventional boost converter and (b) proposed boost converter



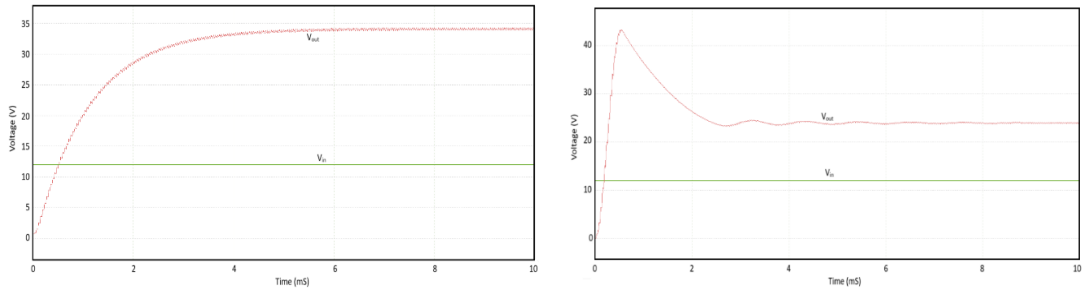
(a) (b)

Figure 4. Output waveform at 0.3 duty cycle (a) conventional boost converter and (b) proposed boost converter



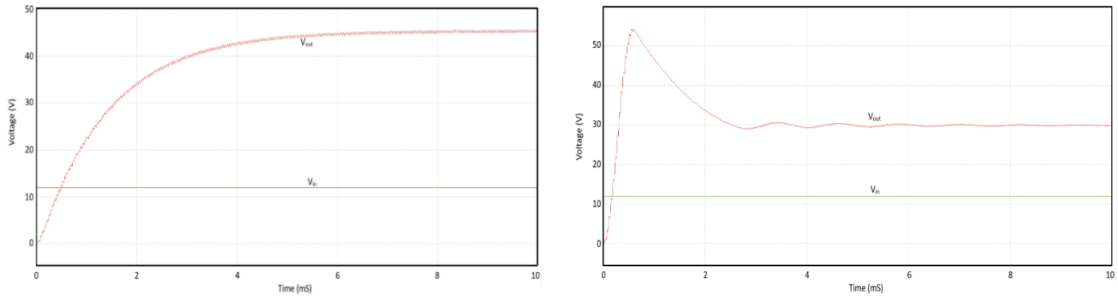
(a) (b)

Figure 5. Output waveform at 0.4 duty cycle (a) proposed boost converter and (b) conventional boost converter



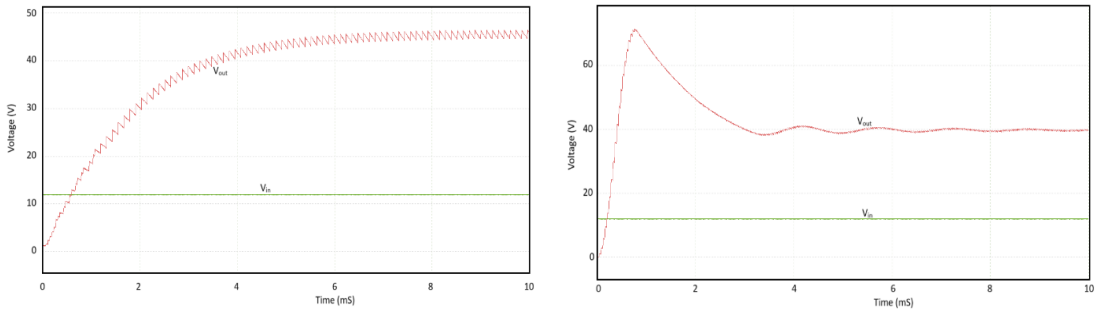
(a) (b)

Figure 6. Output waveform at 0.5 duty cycle (a) proposed boost converter and (b) conventional boost converter



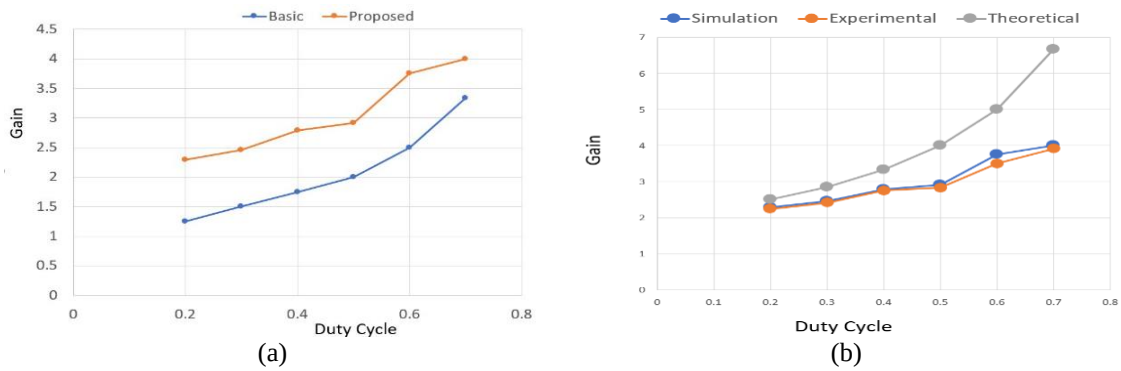
(a) (b)

Figure 7. Output waveform at 0.6 duty cycle (a) proposed boost converter and (b) conventional boost converter



(a) (b)

Figure 8. Output waveform at 0.7 duty cycle (a) proposed boost converter and (b) conventional boost converter



(a) (b)

Figure 9. Comparison of gain versus duty cycle (a) simulation results for basic and proposed converters and (b) theoretical, simulation and experimental results for the proposed converter

Our study suggests that the novel high-efficiency boost converter topology, characterized by minimized component count while maintaining optimal performance, exhibits a significant improvement in efficiency compared to conventional converters. Contrary to previous approaches that emphasized complexity for efficiency optimization, our simplified design achieves notably higher efficiency levels with faster saturation times, promising cost reduction and increased reliability. However, the slight performance degradation observed under extreme load variations highlights the necessity for further research to enhance robustness and adaptability of proposed converter, ensuring its long-term reliability across varying environmental conditions. This study contributes to improve energy efficiency and promote sustainability across various industries, and future research may focus on exploring methods to bolster the converter's resilience and performance stability under dynamic operating conditions.

5. CONCLUSION

In conclusion, our study presents a novel high-efficiency boost converter topology designed to minimize component count while ensuring optimal performance. Our findings demonstrate a substantial efficiency enhancement compared to conventional converters, emphasizing the importance of simplicity without compromising efficiency. By prioritizing simplicity, our topology offers potential cost reductions and increased reliability. These implications address the need for compact and cost-effective power conversion solutions, with broad applications across diverse industries.

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