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Simulation of Cascaded H-Bridge Multilevel Inverter Based DSTATCOM

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Abstract

This paper presents an investigation of five-Level Cascaded H-bridge (CHB) inverter as distribution static compensator (DSTATCOM) in power system (PS) for compensation of reactive power and harmonics. The advantages of CHB inverter are low harmonic distortion, reduced number of switches and suppression of switching losses. The DSTATCOM helps to improve the power factor and eliminate the total harmonics distortion (THD) drawn from a non-liner diode rectifier load (NLDRL). The D-Q reference frame theory is used to generate the reference compensating currents for DSTATCOM while proportional and integral (PI) control is used for capacitor DC voltage regulation. A CHB Inverter is considered for shunt compensation of a 11kV distribution system. Finally a level shifted PWM (LSPWM) and phase shifted PWM (PSPWM) techniques are adopted to investigate the performance of CHB Inverter. The results are obtained through Matlab/Simulink software package.

Keywords: *DSTATCOM, level shifted carrier Pulse width modulation (LSPWM), phase shifted carrier pulse width modulation (PSPWM), Proportional-Integral (PI) control, CHB multilevel inverter, D-Q reference frame theory*

1. Introduction

Power Quality (PQ) is the key to successful delivery of quality product and operation of an industry. The increased application of electronic loads and electronic controllers which are sensitive to the quality of power makes serious economic consequences and of revenues loss each year. Poor PQ can cause malfunctioning of equipment performance, harmonics, voltage imbalance, sag and flicker problems, standing waves and resonance – are some of the issues that adversely affect production and its quality leading to huge loss in terms of product, energy and damage to equipment. Thus, it becomes imperative to be aware of quality of power grid and the deviation of the quality parameters from the norms / standard such as IEEE-519 standard [1] to avoid breakdown or equipment damage.

In present day distribution systems (DS), major power consumption has been in reactive loads. The typical loads may be computer loads, lighting ballasts, small rating adjustable speeds drives (ASD) in air conditioners, fans, refrigerators, pumps and other domestic and commercial appliances are generally behaved as nonlinear loads. These loads draw lagging power-factor currents and therefore give rise to reactive power burden in the DS. Moreover, situation worsens in the presence of unbalanced and non-linear loads, affect the quality of source currents to a large extent. It affects the voltage at point of common coupling (PCC) where the facility is connected. This has adverse effects on the sensitive equipments connected to PCC and may damage the equipment appliances. Excessive reactive power demand increases feeder losses and reduces active power flow capability of the DS, whereas unbalancing affects the operation of transformers and generators [2-3].

Many techniques have been proposed to improve the supply side power factor to cancel out the harmonics generated by power electronic loads. The remedies to PQ problems are reported in the literature and are known by the generic name of custom power devices (CPD) [4]. The DSTATCOM (Distribution static compensator) is a shunt-connected CPD, with the load which takes care of the compensation of reactive power and unbalance loading in the DS (i.e PQ problems). Similarly, the application of Cascaded H-Bridge (CHB) Multilevel Voltage source converter with split capacitors for three-phase three-wire system is found to be satisfactory [6-12]. Among the different control techniques applied to three-phase three-wire compensators, the

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SRFT (synchronous reference frame theory) based technique is found to be suitable for the control of DSTATCOM [14].

This paper presents various issues in design of Proportional Integral (PI) and comparison between the level shifted carrier (LSCPWM) and phase shifted carrier pulse width modulation (PSCPWM) Techniques are used to obtain switching logic for DSTATCOM. The performance of these controllers is demonstrated with linear resistive-inductive (R-L) loads through simulation results using Power System toolboxes (PST) of Simulink / MATLAB.

2. Design of Multilevel Based DSTATCOM

2.1 .Principle of DSTATCOM

A D-STATCOM (Distribution Static Compensator), which is schematically depicted in Figure 1, consists of a two-level Voltage Source Converter (VSC), a dc energy storage device, a coupling transformer connected in shunt to the distribution network through a coupling transformer. The VSC converts the dc voltage across the storage device into a set of three-phase ac output voltages. These voltages are in phase and coupled with the ac system through the reactance of the coupling transformer. Suitable adjustment of the phase and magnitude of the D-STATCOM output voltages allows effective control of active and reactive power exchanges between the DSTATCOM and the ac system. Such configuration allows the device to absorb or generate controllable active and reactive power.

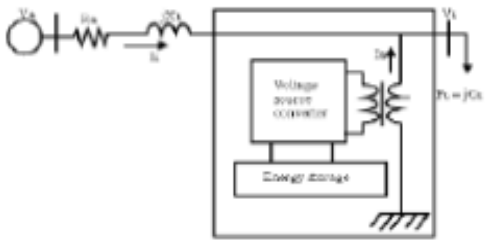

Figure 1. Schematic Diagram of a DSTATCOM

The VSC connected in shunt with the ac system provides a multifunctional topology which can be used for up to three quite distinct purposes:

1. Voltage regulation and compensation of reactive power;
2. Correction of power factor
3. Elimination of current harmonics.

Here, such device is employed to provide continuous voltage regulation using an indirectly controlled converter. As shown in Figure 1 the shunt injected current Ish corrects the voltage sag by adjusting the voltage drop across the system impedance Zth. The value of Ish can be controlled by adjusting the output voltage of the converter. The shunt injected current Ish can be written as:

$$I_{sh}=I_L-I_S$$

$$I_{sh}=I_L-(V_{TH}-V_L)/Z_{TH} \quad (1)$$

The complex power injection of the D-STATCOM can be expressed as:

$$S_{TH}=V_L I_{SH} \quad (2)$$

It may be mentioned that the effectiveness of the DSTATCOM in correcting voltage sag depends on the value of Zth or fault level of the load bus. When the shunt injected current Ish is kept in quadrature with VL, the desired voltage correction can be achieved without injecting any active power into the system. On the other hand, when the value of Ish is minimized, the same voltage correction can be achieved with minimum apparent power injection into the system.

2.2. Control for Reactive Power Compensation

The aim of the control scheme is to maintain constant voltage magnitude at the point where a sensitive load under system disturbances is connected. The control system only measures the root mean square (rms) voltage at the load point, i.e., no reactive power measurements are required. The VSC switching strategy is based on a sinusoidal PWM technique which offers simplicity and good response. Since custom power is a relatively low-power application, PWM methods offer a more flexible option than the fundamental frequency switching methods favored in FACTS applications. Apart from this, high switching frequencies can be used to improve on the efficiency of the converter, without incurring significant switching losses.

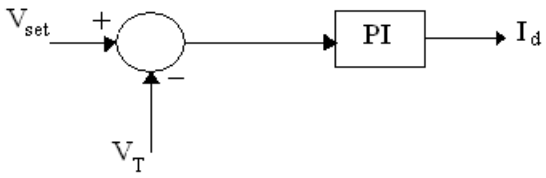

Figure 2. PI control for Reactive Power Compensation

The controller input is an error signal obtained from the reference voltage and the rms terminal voltage measured. Such error is processed by a PI controller; the output is the angle δ, which is provided to the PWM signal generator. It is important to note that in this case, of indirectly controlled converter, there is active and reactive power exchange with the network simultaneously. The PI controller processes the error signal and generates the required angle to drive the error to zero, i.e. the load rms voltage is brought back to the reference voltage.

2.3. Control for Harmonics Compensation

The Modified Synchronous Frame method is presented in [7]. It is called the instantaneous current component (id-iq) method. This is similar to the Synchronous Reference Frame theory (SRFT) method. The transformation angle is now obtained with the voltages of the ac network. The major difference is that, due to voltage harmonics and imbalance, the speed of the reference frame is no longer constant. It varies instantaneously depending of the waveform of the 3-phase voltage system. In this method the compensating currents are obtained from the instantaneous active and reactive current components of the nonlinear load. In the same way, the mains voltages V (a,b,c) and the available currents il (a,b,c) in α-β components must be calculated as given by (4), where C is Clarke Transformation Matrix. However, the load current components are derived from a SRF based on the Park transformation, where „θ" represents the instantaneous voltage vector angle (5).

$$\begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} = C \begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} \quad (3)$$

$$\begin{bmatrix} I_D \\ I_Q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} \quad (4)$$

$$\theta = \tan^{-1}\frac{V_\beta}{V_\alpha}$$

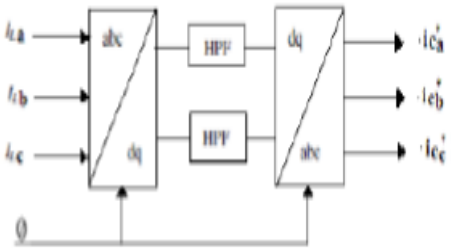

Figure 3. Block Diagram of SRF Method

Figure 3 shows the block diagram SRF method. Under balanced and sinusoidal voltage conditions angle „θ" is a uniformly increasing function of time. This transformation angle is sensitive to voltage harmonics and unbalance; therefore dθ/dt may not be constant over a mains period. With transformation given below the direct voltage component is:

$$\begin{bmatrix} I_{LD} \\ I_{LQ} \end{bmatrix} = \frac{1}{\sqrt{V_\alpha{}^2 + V_\beta{}^2}} \begin{bmatrix} V_\alpha & V_\beta \\ -V_\beta & V_\alpha \end{bmatrix} \quad (5)$$

$$\begin{bmatrix} I_{C\alpha} \\ I_{C\beta} \end{bmatrix} = \frac{1}{\sqrt{V_\alpha{}^2 + V_\beta{}^2}} \begin{bmatrix} V_\alpha & V_\beta \\ -V_\beta & V_\alpha \end{bmatrix} \begin{bmatrix} I_{cq} \\ I_{cd} \end{bmatrix} \quad (6)$$

2.4. Cascaded H-Bridge Multilevel Inverter

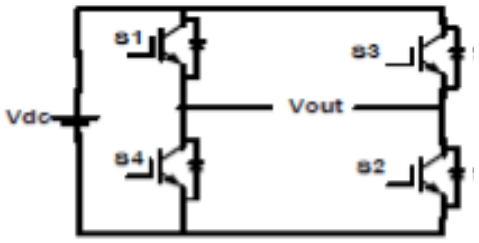

Figure 4. Circuit of the Single Cascaded H-Bridge Inverter

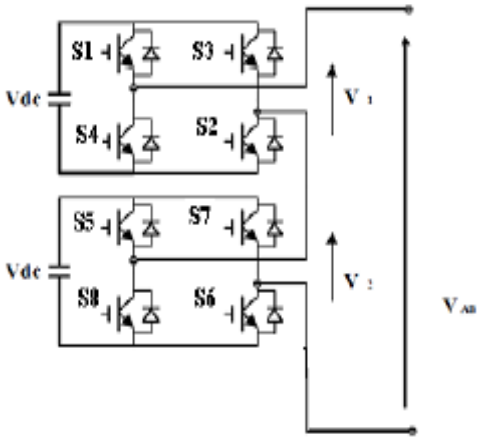

Figure 5. Block Diagram of 5-level CHB Inverter Model

Figure 4 shows the circuit model of a single CHB inverter configuration. By using single H-Bridge we can get 3 voltage levels. The number of output voltage levels of CHB is given by 2n+1 and voltage step of each level is given by Vdc/2n, where n is number of H-bridges connected in cascaded. The switching table is given in Table 1.

Table 1. Switching Table of Single CHB Inverter

Switching states	Voltage levels
S1,S2	V_{DC}
S3,S4	$-V_{DC}$
S4,D2	0

The switching mechanism for 5-level CHB inverter is shown in Table 2.

Switching turn	Voltage levels
S1,S2	V_{DC}
S1,S2,S5,S6	$2V_{DC}$
S4,D2,S8,D6	0
S3,S4	$-V_{DC}$
S3,S4,S7,S8	$-2V_{DC}$

2.5. PWM Techniques for CHB Inverter

The most popular PWM techniques for CHB inverter are:

1. Phase Shifted Carrier PWM (PSCPWM),
2. Level Shifted Carrier PWM (LSCPWM).

Case-1:- Phase Shifted Carrier PWM (PSCPWM)

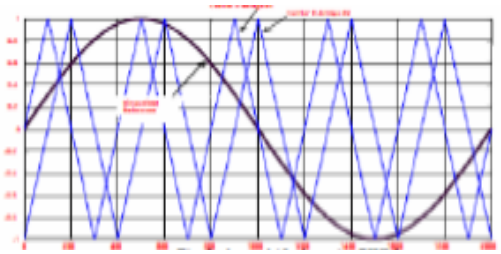

Figure 6. Phase Shifted Carrier PWM

Figure 6 shows the Phase shifted carrier pulse width modulation. In general, a multilevel inverter with *m* voltage levels requires (*m* – 1) triangular carriers. In the phase shifted multicarrier modulation, all the triangular carriers have the same frequency and the same peak-to-peak amplitude, but there is a phase shift between any two adjacent carrier waves, given by$\emptyset_{CR} = \frac{360}{M-1}$.

The modulating signal is usually a three-phase sinusoidal wave with adjustable amplitude and frequency. The gate signals are generated by comparing the modulating wave with the carrier waves. It means for the five level inverter, four are triangular carriers are needed with a 90° phase displacement between any two adjacent carriers. In this case the phase displacement of Vcr1 = 0°, Vcr2 = 90°, Vcr1- = 180° and Vcr2- = 270°.

Case-2:- Level Shifted Carrier PWM (LSCPWM)

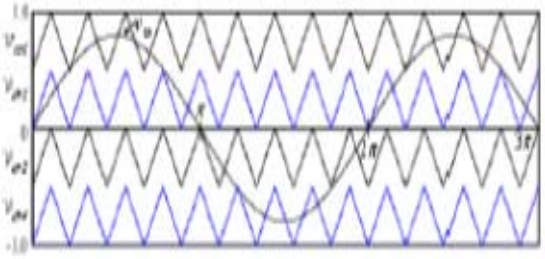

Figure 7. Level Shifted Phase Shifted Carrier PWM

Figure 7 shows the Level shifted carrier pulse width modulation. An m-level Cascaded H-bridge inverter using level shifted modulation requires (*m–1*) triangular carriers, all having the same frequency and amplitude. The frequency modulation index is given by *mf* = *fcr* / *fm*, which remains the same as that for the phase-shifted modulation scheme. For PID modulation, the

multilevel converter with multilevel requires (m1) triangular carriers with same amplitude and frequency. The frequency modulation index „mf" which can be expressed as:

$$m_f = \frac{f_{cr}}{f_m}$$

Where „fm" is modulating frequency and „fcr" are carrier waves frequency. The amplitude modulation index „ma" is defined by:

$$m_a = \frac{V_m}{V_{cr}*(m-1)} \text{ for } 0 \leq ma \leq 1$$

Where Vm is the peak value of the modulating wave and Vcr is the peak value of the each carrier wave [1]. The amplitude modulation index, ma is 1 and the frequency modulation index, mf is 6. The triggering circuit is designed based on the three phase sinusoidal modulation waves, Va, Vb, and Vc. Three of the sine wave sources have been obtained with same amplitude and frequency but displaced 120° out of the phase with each others. For carriers wave sources block parameters, the time values of each carrier waves are set to [0 1/600 1/300] while the outputs values are set according to the disposition of carrier waves. After comparing, the output signals of comparator are transmitted to the IGBTs. Figure 10, 11, 12 shows the waveforms based on three schemes of level shifted multilevel modulations: (a) in phase disposition (IPD) fig-10, where all carriers are in phase; (b) alternative phase opposite disposition (APOD) fig-11, where all carriers are alternatively in opposite disposition; and (c) phase opposite disposition (POD) fig-12, where all carriers above zero reference are in phase but in opposition with those below the zero reference [1]. Out of IPOD, APOD and POD, IPOD gives better harmonic performance.

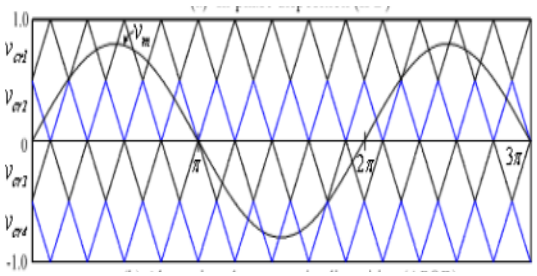

Figure 8. Alternative Phase Opposite Disposition (APOD)

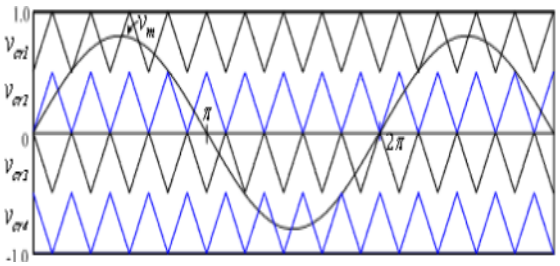

Figure 9. Phase Opposite Disposition (POD)

3. MATLAB/SIMULINK Modeling and Simulation Results

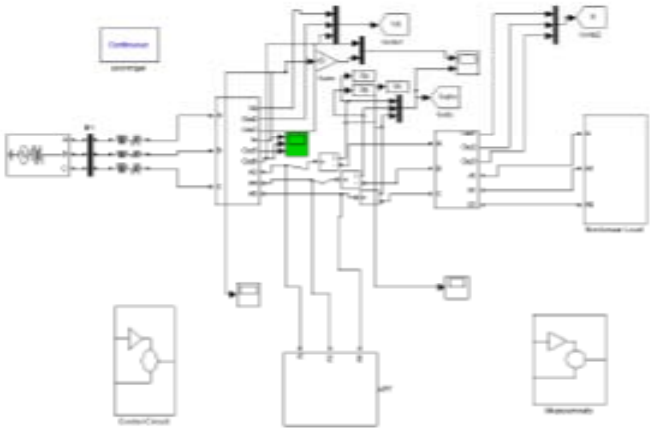

Figure 10. Matlab/Simulink Power Circuit Model of DSTATCOM

Figure 10 shows the Matlab/Simulink power circuit model of DSTATCOM. It consists of five blocks named as source block, nonlinear load block, control block, APF block and measurements block. The system parameters for simulation study are source voltage of 11KV, 50Hz AC supply, DC bus capacitance 1550e-6 F, Inverter series inductance 10mH, Source resistance of 0.1 ohm and inductance of 0.9 mH. Load resistance and inductance are chosen as 30mH and 60 ohms respectively.

Case-1 Phase shifted carrier PWM technique results

Figure 11 shows the phase-A voltage of five level output of phase shifted carrier PWM inverter.

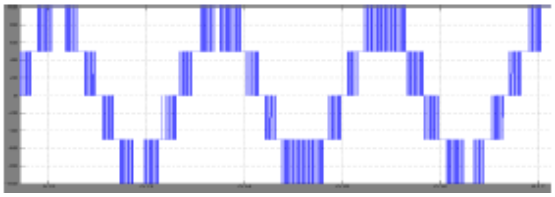

Figure 11. Five Level PSCPWM Output

Figure 12 shows the three phase source voltages, three phase source currents and load currents respectively without DSTATCOM. It is clear that without DSTATCOM load current and source currents are same.

Figure 13 shows the three phase source voltages, three phase source currents and load currents respectively with DSTATCOM. It is clear that with DSTATCOM even though load current is non sinusoidal source currents are sinusoidal

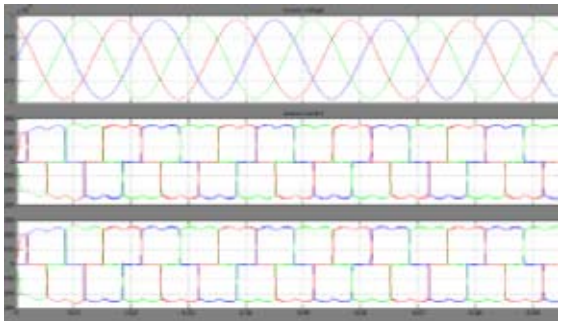

Figure 12. Source Voltage, Current and Load Current without DSTATCOM

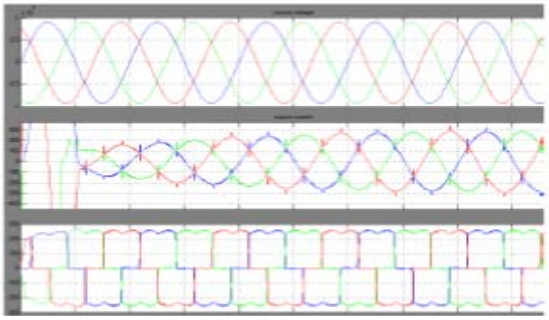

Figure 13. Source Voltage, Current and Load Current with DSTATCOM

Figure 14 shows the DC bus voltage. The DC bus voltage is regulated to 11kv by using PI regulator.

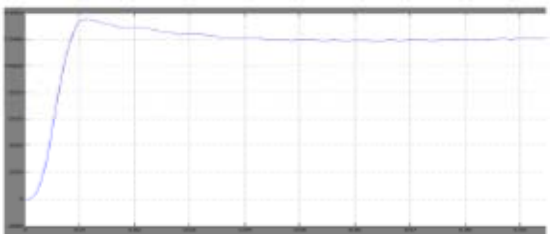

Figure 14. DC Bus Voltage

Figure 15 shows the harmonic spectrum of Phase–A Source current without DSTATCOM. The THD of source current without DSTACOM is 36.89%.

Figure 16 shows the harmonic spectrum of Phase–A Source current with DSTATCOM. The THD of source current without DSTACOM is 5.05%

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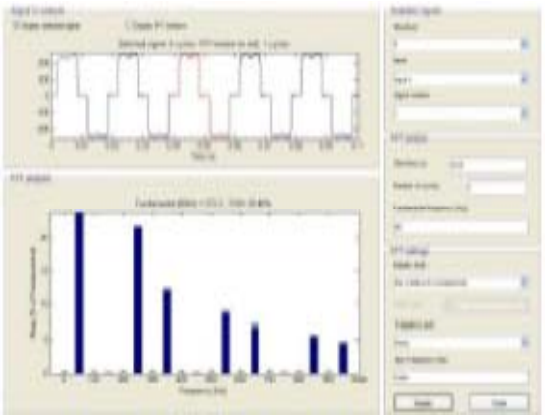

Figure 15. Harmonic Spectrum of Phase-A Source Current without DSTATCOM

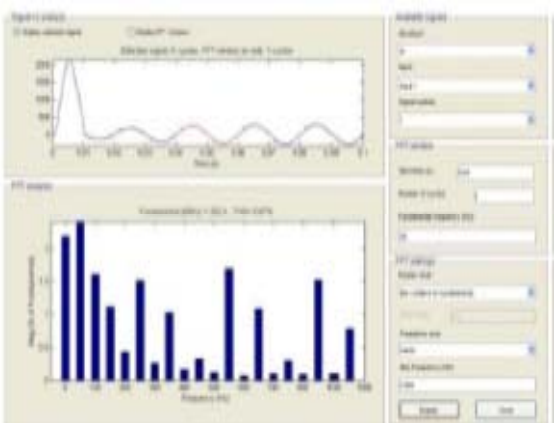

Figure 16. Harmonic Spectrum of Phase-A Source Current with DSTATCOM

Case-2 Level shifted carrier PWM technique results

Figure 17 shows the three phase source voltages, three phase source currents and load currents respectively with DSTATCOM. It is clear that with DSTATCOM even though load current is non sinusoidal source currents are sinusoidal.

Figure 18 shows the DC bus voltage with respect to time. The DC bus voltage is regulated to 11kv by using PI regulator.

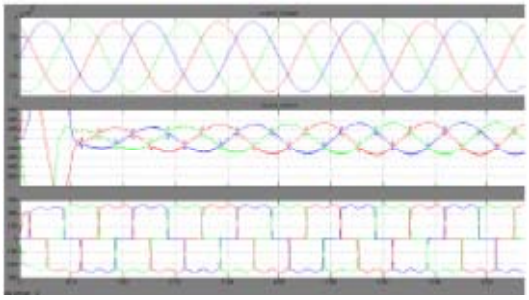

Figure 17. Source Voltage, Current and Load Current with DSTATCOM

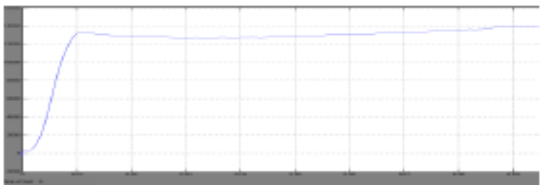

Figure 18. DC Bus Voltage

Figure 19 shows the harmonic spectrum of Phase–A Source current without DSTATCOM. The THD of source current without DSTACOM is 29.48 %.

Figure 20 shows the harmonic spectrum of Phase –A Source current with DSTATCOM. The THD of source current without DSTACOM is 7%.

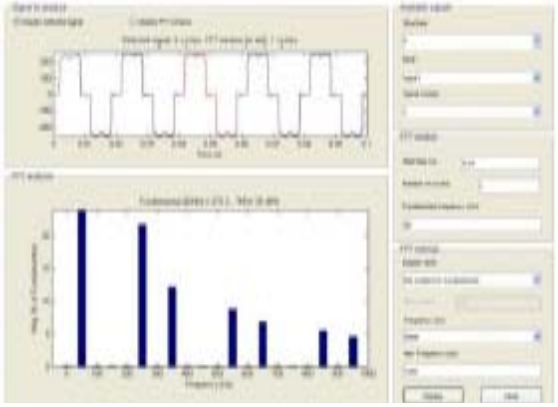

Figure 19. Harmonic Spectrum of Phase-A Source Current without DSTATCOM

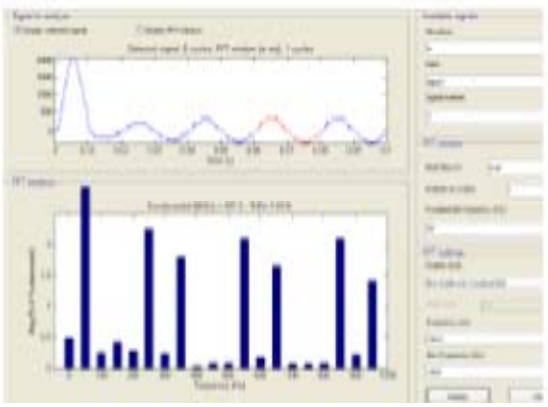

Figure 20. Harmonic Spectrum of Phase-A Source Current with DSTATCOM

4. Conclusion

A DSTATCOM with five level CHB inverter is investigated. Simulation model for single H-Bridge inverter is developed which can be extended to multi H-Bridge. The source voltage, load voltage, source current, load current, power factor simulation results under non-linear loads are investigated for both PSCPWM and LSCPWM and are tabulated. Finally with the help of Matlab/Simulink based model simulation we conclude that PSCPWM is better than LSCPWM techniques and the results are presented.

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