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On-chip based power estimation for CMOS VLSI circuits using support vector machine

Sridevi Nagarajan, Prasanna Kumar Mahadeviah
Department of Electronics and Instrumentation Engineering, Dr. Ambedkar Institute of Technology, Bangalore, India

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ABSTRACT

Power estimation has a major impact on the reliability of very-large-scale integration (VLSI) circuits. As a results power estimation is highly needed in VLSI circuits at the early stages. One of the evident challenges in integrated circuit (IC) industry is development and investigation of techniques for the reduction of design complexity due to the growing process variations and reduction of chip manufacturing turnaround time. Under these conditions, the higher design levels of average power estimation before the chip manufacturing process is highly essential for the calculation of power budget and to take the necessary steps for the reduction of power consumption. Over the years, most of the approaches were designed to estimate the power usage, however, most of the conventional techniques are time consuming, resource-intensive and largely manual. Machine learning techniques have received much attention in many of the engineering applications and are capable for modelling the complex systems through historical data. Hence, in this work on chip-based power estimation for complementary metal-oxide-semiconductor (CMOS) VLSI using support-vector machine (SVM) is presented to estimate the power. The SVM is employed to estimate the usage of power at runtime. The performance of this model is evaluated in terms of Power usage, delay, data accuracy and error rate.

Corresponding Author:

Sridevi Nagarajan
Department of Electronics and Instrumentation Engineering, Dr. Ambedkar Institute of Technology
Bangalore, Karnataka, India
Email: sridevravi@gmail.com

1. INTRODUCTION

The range of integrated circuit (IC) increases with decreasing technology. This could lead to time differences between silicon and simulation. According to the international technology roadmap for semiconductors, yields and manufacturability will face major challenges due to parameter variations [1]. The increasing complexity of ICs has made it essential to build effective automation tools for tasks like design, validation, and debugging [2]. Verification, problem detection, and correction processes in digital systems are becoming more and more important, particularly for digital systems, as a result of the rapid advancements in digital technology. Large-scale circuits and a number of design problems make fault detection in sophisticated large systems difficult [3].

Device engineers are facing both new opportunities and multiple challenges as a result of the aggressive downscaling of complementary metal-oxide-semiconductor (CMOS) technology. Transistor size decrease with increasing semiconductor process complexity. Eventually, basic scaling loses off as they get closer to atomic dimensions [4]. Despite their tiny size, defects have a negative impact on several areas of their performance, such includes more sensitive to modifications in the manufacturing process, lower gain, and increased leakage. The essential increase in process variances has a substantial effect on that the circuit

functions, resulting in inconsistent performance in transistors of the same size. It also has an effect on the circuit's propagation delay, it operates as a stochastic random variable, which lowers chip yield and complicates timing-closure techniques [5].

Millions of transistors can now be developed on a single chip due to recent advancements in very-large-scale integration (VLSI) technology. The primary concern in submicron technology is an increase in transistor count and operating speed within a device, which ultimately leads to higher power consumption [6]. Because power estimation has a significant impact on VLSI circuit reliability, it is important to perform it early in the design process. In considering this, estimating average power at higher design abstraction levels prior to chip produce is essential for determining power budgets and taking necessary steps to lower power usage [7]. Today's high-performance processors with multiple cores are primarily limited by power, thermal and related reliability challenges. This is particularly true when power density begins to increase with advancements in IC technology, after the collapse of the so-called Dennard scaling. Numerous power/thermal regulation or dynamic management techniques, such as task migration to increase dependability, researchers have developed power gating, clock gating, and dynamic voltage and frequency scaling (DVFS) [8]. The circuit's power dissipation is determined by its operating voltage, frequency, and inputs. The two primary categories for estimating average power are simulation and non-simulation-based methods.

Because it is difficult to estimate the normal amount of power required by an electronic system, estimating power consumption can be difficult. This is not to be associated with the voltage drop problem, a requirement for estimating the instantaneous power in the worst-case scenario. The average amount of power collected from the chip is directly correlated with the temperature and heating it produces [9]. In VLSI circuits, power estimation at an earlier stage is highly needed, because it has a major impact on the reliability of VLSI circuits. Under this condition, at the higher levels of design abstraction average power estimation before a chip manufacturing is very much essential to calculate power budget and to take necessary steps to reduce power consumption. Therefore, simpler and less expensive power estimation methods are required [10]. Artificial intelligence (AI) has produced notable answers to numerous issues across a wide range of industries. The concept of AI is founded on the idea that human intelligence can be easily reduced by machines, it can subsequently carry out variously challenging tasks. Within AI as the subfield of machine learning (ML). Perception is the first of AI/ML's four primary goals, learning, reasoning, and prediction. This AI/ML enables users to make important decisions by quickly recognizing patterns and trends in large amounts of data [11]. High computing speeds are available for handling multi-dimensional and multivariate data using AI/ML algorithms. As these algorithms gather additional experience, the predicted accuracy and efficiency increase [12].

Applications for machine learning have been expanding in VLSI recently. Many electronic design automation (EDA) and IC design firms are investigating ML techniques to ensure IC operating while reducing manufacturing runtime and time-to-market. As a result, a wide range of applications are utilizing various techniques and at various design stages [13]. Since these computationally inexpensive models are capable of reproducing the behavior of non-linear systems and can be used directly for their design and optimization, ML based modeling to this domain has contributed to several breakthroughs in the interconnect design and development process [14]. ML and AI have the potential to significantly increase the automation of the chip design cycle. Applications requiring real-time target value estimate that effectively proved the applicability of data-driven models [15].

Different techniques were described to estimate on chip power and performance of VLSI circuits, however most of the works are not accurate and cost effective. To solve these issues, this research presents chip-based power estimation using support vector machine (SVM) for CMOS VLSI. The main aim of this work is to accurately estimate and evaluate the performance of on-chip CMOS VLSI circuits. This model estimates and evaluates on chip performance using SVM algorithm. The performance of on-chip will be evaluated in terms of power usage, delay, data accuracy, and error rate. The organization of the research is arranged as follows: in section 2, the literature survey is described. In section 3 on chip-based power estimation for CMOS VLSI using SVM is presented. The section 4 evaluates the performance validation. The section 5 presents the conclusion.

2. LITERATURE SURVEY

In this analysis, a new approach to on-chip power-noise modeling during the initial system-on-chip (SoC) design stage is presented. Simplified chip power models (SCPMs) are established for each SoC sub-block, and these unit SCPMs are combined into a single SCPM that includes multiblock features. In order to prevent overestimating the analog current (AC) current, SCPM integrates the background current and offers a number of current profiles to help estimate the maximum current peak with accuracy. Finally, since physical circuit information is not required, set designers are able to assess system power noise and address SoC power-noise issues through adaptable cooperation between IC and set designs [16].

In order to achieve true motion estimation (ME), further inter-frame data reuse, this analysis presents an innovative approach to inter-frame data reuse. A case study of real ME, specifically, frame rate up-conversion (FRUC-ME) using ME is used. Instead of being placed twice, a frame is only placed once in the on-chip buffer, and utilized with the new inter-frame data reuse technique for two interpolated frames for FRUC-ME. The novel technique is proposed in two levels: new Inter-E and Inter-D. These numbers offer a reasonable solution between the off-chip memory's bandwidth and the on-chip buffer's size. Utilizing a new technique to data reuse, there must be an additional data access order. In comparison to its intra-frame cousin, less off-chip memory bandwidth is needed for the recommended data reuse technique (Inter-D); additionally, with FRUC-ME, both power consumption and off-chip memory traffic are decreased by 37.5% [17].

An efficient ML framework is offered to give the chip designer a reliable foundation for measuring network on chip (NoC) performance characteristics. It is made utilizing various machine learning regression algorithms, such as artificial neural networks (ANNs) with different activation functions and different kernels for support vector regression (SVR). The performance metrics of NoC designs based on mesh and torus can be examined using the suggested learning methodology. The acquired results are compared with the cycle-accurate Booksim simulator which is frequently used. Variables such as traffic patterns, injection rates, and topological sizes ranging from 2×2 to 30×30 were used in the experiments. A 5% to 8% approximation in prediction error was demonstrated using the framework [18].

Two situations are taken into consideration while proposing a ML model: a floorplan-based delay among NoC components and a fixed delay between components. In order to forecast NoC performance characteristics while taking uniform random and transposition traffic patterns taken into consideration, several ML regression algorithms are used to describe this framework. With the suggested ML framework, it is possible to conduct an extensive performance analysis of mesh NoC architecture. The efficiency of the suggested architecture is confirmed by the Booksim simulator results, which demonstrated an overall speedup of 2,000× to 2,500× [19].

For register transfer level (RTL) combinational circuits, an approach to estimate pin-to-pin delays based on ML is presented. They integrate delay and slew estimation to increase accuracy. In order to achieve this, a training dataset is built using the features of a model-driven hardware generator framework. Using tools for static timing analysis and open-source logic synthesis, ground truth labels for delays and interdependencies, their slews are retrieved. According to the evaluations in untested designs, the delay estimation is 13 x times faster and has an average accuracy of 87% when compared to timing analysis and synthesis tool results. An early in the design flow, appropriate microarchitecture selections can be made based on the estimation of the design's essential areas [20].

An intelligent new procedure for choosing important process parameters in order to assess performance goals like leakage and time. Applying to the international symposium of circuits and systems in 1985 (ISCAS'85), ISCAS'89 (ISCAS in 1989) the flow that is being provided the most common parameters in 32 and 45 nm CMOS technologies, and benchmark circuits for international workshop on logic and synthesis (IWLS 05). The authors determine the effective gate length, temperature, gate-oxide thickness, and supply voltage to be the four main parameters impacting time and leakage through this flow. According to experimental data, the recommended process parameters in the benchmark circuits produce high evaluation accuracy (on average, <1% errors in leakage and <3% errors in timing). As a result, the suggested flow can choose dominating parameters for performance goals, and the four parameters identified correctly evaluates timing and leakage in CMOS technology developed at 32 and 45 nm [21]. A new model is presented with two levels namely Inter-D and new Inter-E that can provide a better tradeoff between on-chip buffer size and off-chip memory bandwidth. To implement the new data reuse model, new data access order is used. This data reuse model (Inter-D) demands less off-chip memory bandwidth compared to its intra-frame counterpart (Intra-D) and both power consumption and off-chip memory traffic is reduced by 35% [22].

To determine the most suitable accelerated test circumstances and accelerated test region for the time dependent dielectric breakdown (TDDB) accelerated test of logic circuits, a framework is proposed. They look into middle-of-line (MOL) TDDB as well as gate-oxide breakdown. A Leon3 microprocessor where the possibilities of the framework are demonstrated using two digital circuits and an 8-bit fast fourier transform (FFT) circuit. Finding the test settings that result in the least amount of error makes it possible to identify the optimal accelerated test area. This is done during accelerated test settings by predicting the wear out parameter errors. For each test condition, the necessary sample size is found given a forecasting error objective. Since this work only takes into consideration the MOL and TDDB, more work is required [23].

The purpose of this analysis was to study the power cycling behavior of high-power modules that have several small silicon carbide (SiC) diode chips installed in parallel on each substrate. Moreover, the applicability of advanced lifetime models for traditional silicon power modules to silicon carbide power modules with this substrate arrangement was examined. This that numerous power cycling experiments were carried out on power modules at various changes in temperature. The results indicate that performance is

below that the CIPS 08 model predicted, but if an additional factor was applied, the model might accurately reflect the test results, at least for temperature swings from 60K to 100K [24].

Field programmable gate array-based designs initial power estimation model is explained. Using a low-level virtual machine intermediate representation, they analyze at the C-level. Then, using the profiling data, they train a neural network to provide an estimation model. The accuracy of the model is demonstrated using benchmark applications such as Rosetta-master, MachSuite, and CHStone. With an exceptional 87-fold increase in estimating speed over the Xilinx Vivado design suite, for the benchmark designs, a small relative error of 0.21% to 5.12% is seen during analysis [25].

3. ON CHIP-BASED POWER ESTIMATION FOR CMOS VLSI

In this section, on chip-based power estimation for CMOS VLSI using SVM is presented. The described system's block diagram is displayed in Figure 1. Power estimation refers to the problem of estimating average power dissipation of digital circuits. The use of ML approaches to predict the activity of all test patterns globally and to estimate power usage and save run time is supported by the fact that it is not practical to reproduce every test pattern accurately in order to obtain its power profile. The chip data includes input ports, output ports, input pins, output pins, and memory pins. The system chip data is considered and the data is pre-processed. Pre-processing data can increase the amount of information's accuracy, quality by removing data values that are missing or inconsistent could have been the result of human or computer mistakes, they can improve its reliability. Data consistency is achieved. The most important elements for using learning algorithms are the features and the training data. To predict test power and distribute it throughout the layout, features need to be taken out in various design flow phases. The data connected to design it was available in many formats and is utilized by various tools; therefore, it must be processed appropriately. These files include information that is utilized for various purposes. For the learning part, the necessary data must be retrieved and prepared.

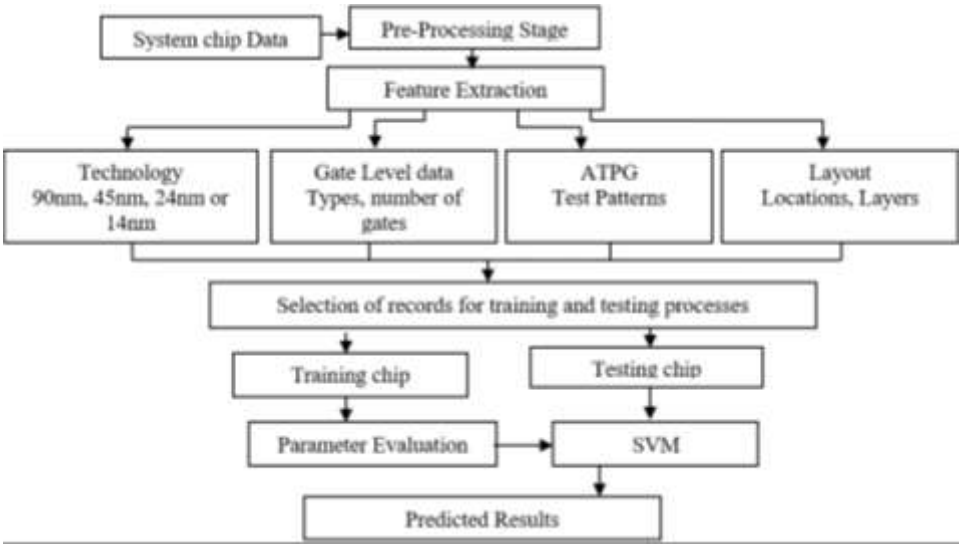

Figure 1. Block diagram of on chip-based power estimation for CMOS VLSI

The physical locations of the gates and other layout information are not necessary when aiming for the global power usage. To find local hotspots, this data needs to be processed and kept. As a result, the layout data such as that found in the .def and .lef files is used to extract the cell locations and sizes. To identify power-critical locations, this data can be input into commercial EDA tools or used in various ways, such as heatmap analysis. In VLSI, "nanometer" refers to the measurement of the feature size of transistors and other components on a semiconductor chip. The term "nanometer" (nm) represents one billionth of a meter. Common nanometer technology nodes used in VLSI fabrication include 45 nm, 32 nm, and 22 nm.

"Gate level" describes the netlist perspective of a circuit, which is typically generated by logic synthesis. Gate level data describes the types of gates and number of devices, and gates. Gate-level data provides a specific implementation using logic gates and flip-flops. The gate level data describes the number

of gates, flip-flops required for chip design. Automatic test pattern generation (ATPG) generated test patterns the test patterns, also known as test vectors are essential components of the test and are produced using ATPG tools. Generally, scan structures allow the flip-flops in the circuit to be assigned directly, without the need for functional operations. Scan structures are frequently used to achieve a high-test coverage with a low-test application time. Using shift cycles, a scan test is first applied before being applied during the capture cycle (s). Scan tests have the disadvantage of non-functional behavior it comes to test power since it is not always possible to reach the scanned state of the flip-flops in the functional mode.

The necessary information, or the contents of the scan cells during each scan chain and test pattern operation, this taken out of the test-pattern files and saved for later processing in this suggested technique. In this method, the relevant information is extracted from automated test logs and stored for further examination; that is, the content of the scanning cells is transitioned and retrieved for each scan chain, allowing for a comprehensive analysis. To save time, it is suggested that ML technology be used to predict that every training set would behave on both a national and international scale.

SVM, also known as SVM, is among the most popular supervised learning techniques for issues involving both classification and regression. Essentially assigning a new data point to the relevant category going forward, in order to partition n-dimensional space into classes, the SVM method looks for the best line or decision boundary. An optimal decision boundary is called a hyperplane. Selecting the extreme points and/or vectors is that SVM creates a hyperplane. SVM is the name given to the technique since these extreme cases are known as support vectors. The continuous-valued output class is determined by the hyperplane, which functions more like an equation. In this analysis, they take into consideration the non-linear nature of the data by developing an SVM regression model with a third order polynomial kernel. The features of the third order polynomial kernel are described by the (1):

$$K(x, y) = (x^T y + c)^3 \quad (1)$$

where c is a free parameter that trades off the impact of higher-order against lower-order parts in the polynomial and x and y are vectors in the input space that resemble feature vectors generated from training or testing data points.

Firstly, the primary information of chip (power required, usage purpose, and no-of pins) are collected and the collected data is preprocessed. From the preprocessed data, relevant features are extracted and irrelevant features are removed. After the feature extraction, the appropriate data such as technology used for chip fabrication, number of gate levels, transistors are required for the chip design, APTG test patterns of chips and location and layer of chip are selected for training and testing the chip performance. The data is tested and trained and applied to SVM. Here, in this analysis SVM is employed to estimate the power usage, delay, data rate accuracy and errors of on-chip. Finally, the SVM predicts the power usage of on-chip, error rate, data accuracy and delay of on-chip. The new contribution of this work is achieving better performance in terms of power usage of on-chip, error rate, data accuracy, and delay of on-chip.

4. RESULT ANALYSIS

In this section, result analysis of on chip-based power estimation for CMOS VLSI using SVM is demonstrated. The performance of presented method is validated in terms of power usage, accuracy of the data, delay, and error rate. The Table 1 shows the performance evaluation. Compared to LR and RF algorithms, SVM has shown better performance for on-chip based power estimation. The Figure 2 shows the data accuracy comparison. In Figure 2, the x-axis represents different ML algorithms and y-axis indicates the data accuracy values in terms of percentage. The SVM algorithm has high data accuracy for on-chip based power estimation approach than LR and RF algorithms. The Figure 3 shows the error rate comparison.

Table 1. Performance evaluation

Metrics/methods	Logistic regression (LR)	Random forest (RF)	SVM
Data accuracy (%)	85	89.34	96.6
Error rate (%)	13.2	10.7	3.2
Power usage (%)	45	35	10
Delay (ms)	25	17	2

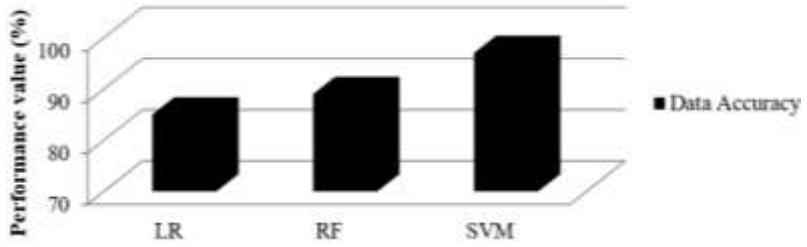

Figure 2. Data accuracy performance comparison

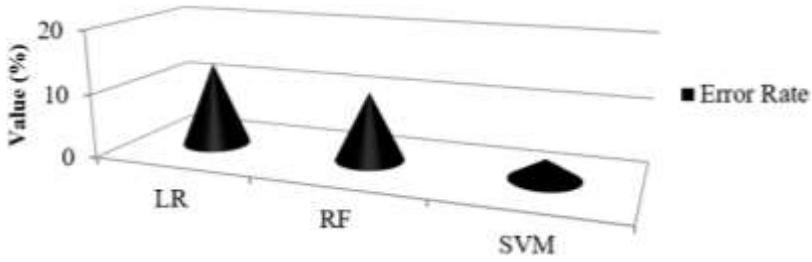

Figure 3. Error rate comparison

In Figure 3, the x-axis represents different ML algorithms and y-axis indicates the error rates values in terms of percentage. The SVM algorithm has very low error rate than RF and LR algorithms. The Figure 4 shows power usage comparison.

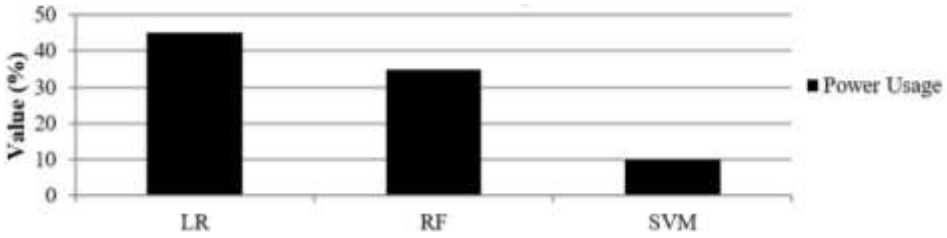

Figure 4. Power usage comparison

Compared to LR and RF methods, the SVM has used very less power. The Figure 5 shows delay comparison. In Figure 5, y-axis shows the delay in milliseconds (ms), while the x-axis displays several ML algorithms. The SVM has very less delay than RF and LR algorithms. Hence from the results, it is observed that the SVM has shown significant performance for on-chip power estimation with accurate results and consumed very less power with very less delay. Therefore, this approach will be a better solution to estimate the chip power in real time with very low cost.

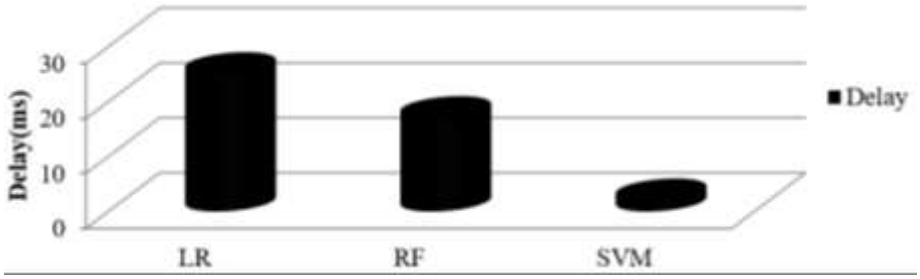

Figure 5. Delay comparison

5. CONCLUSION

This paper presents on chip-based power estimation for CMOS VLSI using an SVM. A supervised learning technique for estimating the power of CMOS VLSI circuits is provided in this analysis. The SVM model is an alternative model, to more traditional approaches like simulation program with integrated circuit emphasis (SPICE) circuit simulations which are based on the application of arbitrary parameters and predetermined empirical equations. Here in this analysis SVM is used to predict the on-chip performance. The performance of presented method is validated in terms of data accuracy, error rate, power usage, and delay. The SVM has shown better data accuracy, very less delay, less error rate, and used very less amount of power in CMOS VLSI circuits. The results demonstrate that SVM is the best choice for CMOS VLSI circuit power estimate. Hence, this system has effectively estimated the on-chip CMOS VLSI circuit performance. It will be used to estimate the power of any circuit, regardless of technology, design style, functionality, and architecture in future, deep learning-based model will be designed to detect and protect the on-chip CMOS VLSI circuits from faults.

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BIOGRAPHIES OF AUTHORS

Sridevi Nagarajan obtained her B. E. degree from UBDTCE, Davangere, M. Tech degree, from VTU, Karnataka and Ph.D. from VTU, Karnataka. She is working as Associate Professor in the Department of Electronics and Instrumentation Engineering, Dr. Ambedkar Institute of Technology, Bangalore, Karnataka. She has more than 40 publications in international journals, national and international conferences. Her areas of interests include VLSI design, image and video processing, process automation, robotics and control. She can be contacted at email: sridevravi@gmail.com.

Prasanna Kumar Mahadeviah completed his B E from SJCE, Mysore, Karnataka and M. Tech from NIT Suratkal, Karnataka. Currently pursuing Ph.D. in VTU, Belagavi, Karnataka, India. He has authored or co-authored more than 30 papers including international journal, national and international conferences. He completed 3 research projects. His research interests include embedded systems, data base management system, VLSI design. He can be contacted at email: prasannakm13@gmail.com.