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An Improved A Low Power CMOS TIQ Comparator Flash ADC

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Abstract

This paper was presented the design of a threshold inverter quantized (TIQ) comparator in flash analog to digital converter. The TIQ-comparator has a high speed response; however this circuit involves a lot of transistors hence wasteful power consumption. The design is intended to obtain a low-power TIQ-comparator and reduces the area of the chip in 0.18 µm CMOS technology. The method was proposed to set each of the transistor channel length for the threshold voltage difference gained of the inverter each in the TIQ-comparator and adding a transistor as compensation to overcome the limitations of the length channel expansion due to the body effect influence. This method has reduced the drain current of CMOS transistors; hence the power dissipation can be reduced. The event has achieved low power dissipation of 31.14 µW and a chip size of 1065 µm2 with 0 to 0.6 V input signal condition.

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Keywords*: TIQ-comparator, low power, CMOS technology*

1. Introduction

Analog to digital converter (ADC) is a useful building block in many applications such as a data storage read channel and an environment condition monitoring receiver because they represent the interface between the real world analog signal and the digital signal processors. Many implementations have been reported in the literature in order to obtain high performance ADC, for example successive approximation, delta sigma and flash ADC.

Flash ADC architecture is known for its high-speed operation. An analog input voltage is simultaneously compared by 2^n – 1 voltage comparators in an n-bit flash ADC [1]. The comparators are the most critical components in a flash ADC. In this design, the comparators are realized with the inverters, which avoid the complexity in the design of conventional comparators. An inverter is used as a comparator known as threshold inverter quantization (TIQ)-Comparator.

The TIQ-comparator has been often proposed and simulated in flash ADC design for high speed, small size, low power consumption, and linearity [1-3]. A basic TIQ comparator circuit consists of two cascaded CMOS inverters as shown in Figure 1 [2, 4]. Here, the first inverter threshold voltage (V_{th}) acts as voltage reference. The second inverter serves as the gain booster to keep the linearity in balance from the voltage rising and falling intervals [5].

For the construct a comparator requires two inverters. An inverter contains two CMOS transistors, so for the single comparator requires four of CMOS transistors such as Figure 1. Therefore, it is in the construct of the 64-bit TIQ-comparator requires as much as 4 X 64 = 256 CMOS transistors. The operation of the transistor as it will not slightly power consume and large chip area, if not caution more planned.

The previous researchers have proposed many ways to set the TIQ-comparator for quantization of data in flash-ADC system. Yoo and Tangel have been suggested that the analog input signal quantization level is set in the first stage by changing the voltage transfer curve (VTC) [5, 6]. They were confirmed that to get the V_{th} shift is to set the *W* ratio of PMOS and NMOS, whereas the *L* is fixed. The other hand, the size of transistor channel lengths, *L* and width, *W* are adjusted [4].

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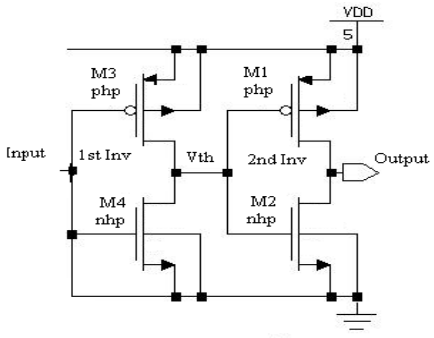

Figure 1. A TIQ Comparator Basic Circuit

This research applies to another method, by adjusting *L* and keeping *W* fixed and adding 1 or 2 transistors as compensation to overcome the limitations of the *L* channel expansion due to the body effect influence. The advantages of this method are reduced power consumption and area of the layout. Increasing *L* reduces the transistor drain current, I_D according to [7] for a transistor in saturated condition as:

$$I_D = \frac{1}{2}\frac{\mu\,\varepsilon_{ox}}{t_{0x}}\frac{W}{L}(V_{GS} - V_t)^2(1+\lambda V_{DS}) \quad (1)$$

Where μ is electron mobility, εox is the permittivity of the silicon dioxide, tox is the thickness of the oxide layer, V_{GS} is the gate–source va channel length modulation coefficient λ is a channel length modulation coefficient and V_{DS} is drain-source voltage. Moreover, in the proposed method, the physical form is more symmetrical to ease the arranging and layout of devices.

The basic design of the TIQ-Comparator for a n-bit flash ADC requires 2^n-1 comparators [8]. Therefore a 6-bit flash ADC requires (2^6) - 1 = 63 TIQ comparators. Meanwhile, according to [9, 10, 11], *L* of each first inverter PMOS of the comparator is derived from the mathematical expression for V_{th} of any quantized sub-unit given approximately as:

$$V_{th} = \frac{VDD - |V_{tp}| + V_{tn}\sqrt{\frac{K_n}{K_p}}}{1+\sqrt{\frac{K_n}{K_p}}} \quad (2)$$

Where V_{tn} and V_{tp} are the threshold voltages for NMOS and PMOS devices respectively, and $K_n = (W/L)_n$. $\mu n\, C_{ox}$, $Kp = (W/L)_p$. $\mu_p\, C_{ox}$ and μ_n and μ_p are the electron and hole mobility's of NMOS and PMOS, respectively. C_{ox} denotes gate-oxide capacitance per unit area.

Section II shows the methodology of this work. Section III shows Result and discussion. Section IV shows the conclusion.

2. Research Method

We used the following design process to develop the proposed TIQ-Comparator.

a) Firstly, the development of the comparator was based on the basic circuit given in Figure 1.
b) Secondly, Equation (2) was used to calculate *L* of the first inverter PMOS, according to the desired value of threshold voltage and this result is shown in Figure 2. The graph in Figure 2 showed an increase *L* of TIQ-comparator each number from no. 1 to no. 21. The increase in the graph is not linear due to the Equation (2) contains of the square root elements. Therefore the TIQ-comparator for the next number is required addition transistors as compensation.

c) Lastly, the input voltage range of the TIQ Comparator is matched to the output voltage of temperature sensor, which extends from 360mV to 560mV with 1.6V supply voltage.

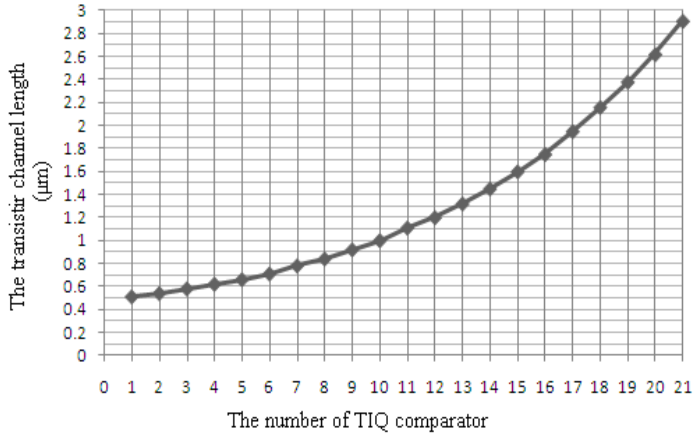

Figure 2. The Calculation Results of the PMOS Transistor Channel Length

d) Further implementation of the design is done as follows: the design size of *L* and *W* of the second inverter is fixed, according to the design standard of the 0.18-µm CMOS Technology. The standard design is 0.18 µm for *L* and 1.4 µm for *W* of PMOS and NMOS transistors. PMOS transistor's *W* on the first inverter is fixed at 1.4 µm, whereas the channel *L* is adjustable for each sub-unit according to Fig. 2. However, NMOS of all first inverters follow the standard design.

The calculation is made starting from most significant bit (MSB) of quantization to the least significant bit (LSB) with the value of V_{th}, 600mV to 285mV. In this calculation, only the size of *L* for the comparator no. 1 to 21 are obtained, with the channel *L* from 0.51 µm to 2.91 µm as shown in Figure 3.

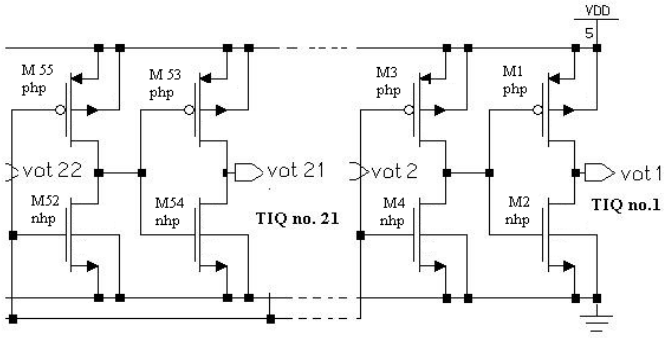

Figure 3. The TIQ Comparator (from no. 1 to no. 21)

Furthermore, to overcome the limitations of the L channel expansion due to the body effect influence according to Equation (3) as:

$$V_t = V_{to} + \gamma\left[\sqrt{2|\phi_F| + V_{SB}} - \sqrt{2|\phi_F|}\right] \quad (3)$$

Where, V_t is threshold voltage, V_{to} corresponds to the threshold voltage when V_{BS} = 0V, □□ is the body effect parameter and ϕ_F is the surface potential at strong inversion, hence the

comparator no. 22 to 63 one or two PMOS transistors were inserted as compensation in diode connection, to extend the achievement of the expected voltage input range to the lower side. The compensation transistor is inserted between VDD to the first inverter PMOS transistors as shown in Fig. 4. The circuit is designed and simulated by using the tools of the Mentor Graphics Design Architect (DA) CEDEC_KIT. This design and simulations are iterated to achieve a linear quantization.

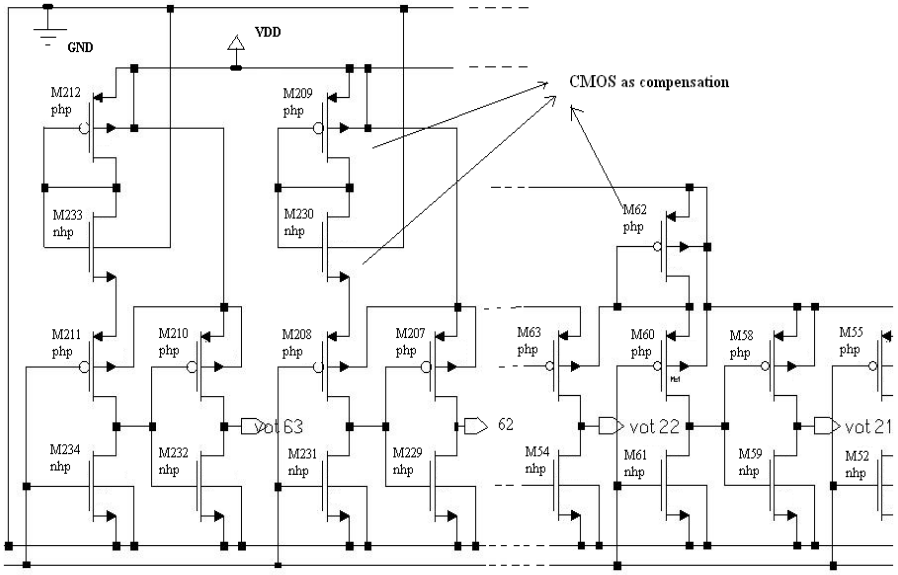

Figure 4. Comparator with CMOS Compensation

3. Results and Analysis

Based on the complete circuit design of 64 levels TIQ-comparator, executed the simulation schematic by providing a DC input of 0V to 0.61V. The graphic quantization output was shown in Figure 5. The quantization output is known thermometer code usually. From this graph we can see, that is, responding from 0.285V to 0.6V. If the DC input level is below 0.285V and above 0.6V the output quantization no response. The thermometer code is to change one level if the DC input 5mV changes up or down. In this simulation conditions are obtained 31.14µW power dissipation. These phenomena are convincing to quantify the analog data sensor within the range of 0.36 and 0.56V only.

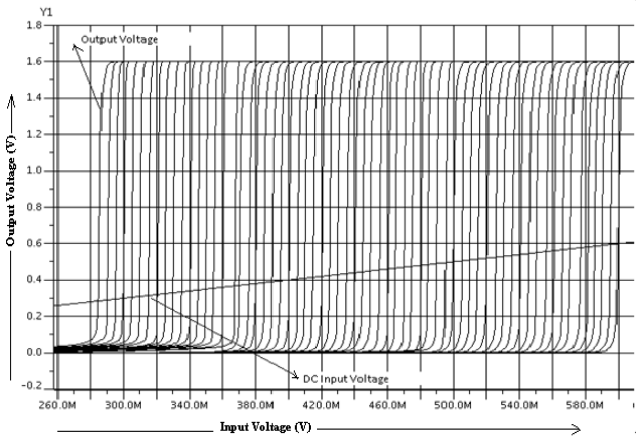

Figure 5. Quantization Output from the DC Input Voltage 0 to 0.61

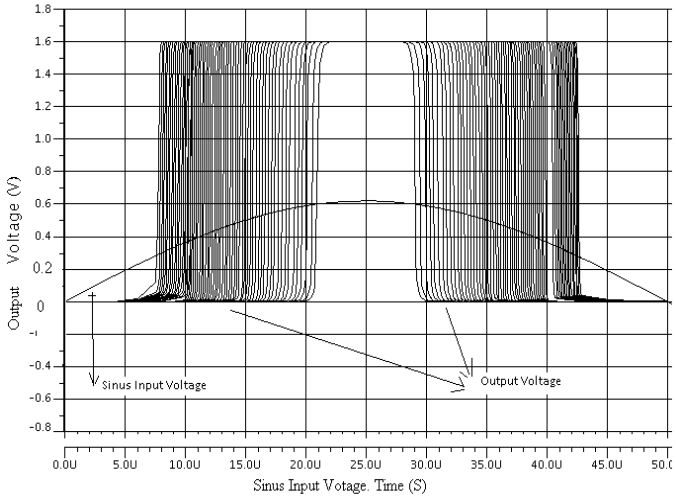

Figure 6. Quantization Output for the Sine Input Voltage 0.61V and 10KHz

Figure 6 illustrates the simulated result of the TIQ Comparator designed on 64 levels of quantization with the sinusoidal input voltage of 0V to 0.6 V-peak at the frequency of 10KHz and half wave positive transition. This graphical response exhibits a good linearity and sensitivity with linear rise and fall of the input signal. If the input signal 10KHz above to be given to the circuit, hence it was not capable to perform linearly data quantization, due increasing the length *L* of the CMOS transistor or body effect influence consequently increasing delay time, which means that this circuit has the ability to respond up to 10KHz only. Therefore, this circuit is suitable for use as a sensor signal processing which not required high speed such as a temperature sensor, humidity sensor and etc. In this simulation, conditions obtained 31.14µW power dissipation.

Finally, the layout of the circuit was designed by using Mentor Graphics IC CEDEC_KIT design as shown in Figure 7. This picture provides information that; proceeds layout design area of 150 x 71µm or 10650µm^2. This layout area has not been included of the other circuits in the flash ADC system.

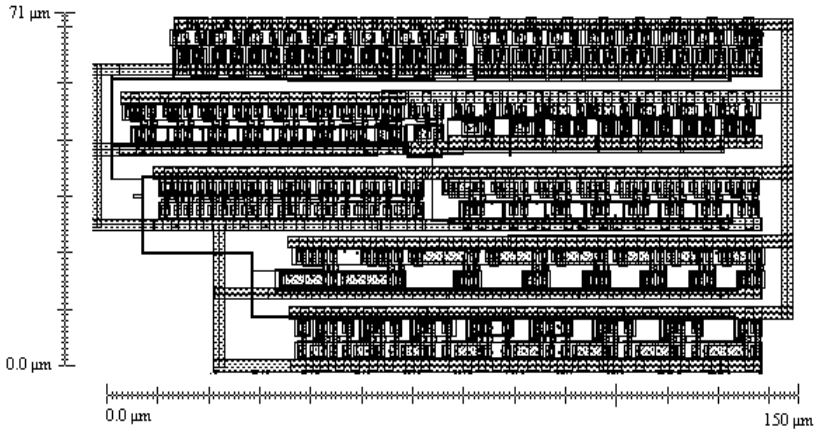

Figure 7. Layout Design of the TIQ-comparator Proposed

The comparisons of the TIQ-comparator for the flash ADC with related works are shown in Table 1. It is evident that the designed work achieved smaller chip area. Moreover, the power dissipation is also significantly lower than the previous works. Although their research has been in the form of a complete flash ADC, however, it is enough to provide an overview of significant

comparisons due the TIQ-comparator part occupies a space that exceeds 50% and power consumption was also as in the complete Flash ADC system. Thus the proposed design can be expected that the chip area of 16.4 times smaller than the Tangel A and Choi, K [6] works, and the power consumption of 14.3 times lower than the design of the SC Hsia and Lee WC [8].

This result is better because of the methods used by increasing the length *L* of the transistor channel. In addition the use of smaller CMOS technology such as [6] uses a larger CMOS technology, which is 2μm and supply voltage of 5V, so that he gained greater power dissipation (3350μW) and 35000μm^2 layout areas. In the other references it can be seen that the use of the CMOS technology is 0.18μm [1] and [2] with the supply voltage disparate are 1.8V and 2.5V respectively, they gain higher power dissipation as well.

Table 1. The Comparison Results with Eight other Comparators for flash ADCs

References	CMOS Technology (μm)	Type of Result	Input range (V)	Supply Voltage (V)	Power Dissipation (μW)	Layout area (μm^2)
[1]	0.18	Simulated	-	1.8	36980	-
[2]	0.18	Simulated	1.6	2.5	53000	-
[6]	2.00	Simulated & fabricated	1.72	5	3350	35000
[8]	0.35	Simulated & fabricated	0.4-2.4	3.3	895	-
[11]	0.35	Simulated & fabricated	0.785-2.092	3.3	-	-
[12]	0.35	Simulated & fabricated	3.8	5	4730000	650000
[13]	0.70	Simulated & fabricated	-	5.5	-	3996000
[14]	0.35	Simulated	1.6	3.3	12400	-
This Work	0.1 8	Simulated	0.315	1.6	31.14	1065

4. Conclusion

The TIQ Comparator is designed and verified by using the Mentor Graphics VLSI Design Software. It consists of 63 pairs of CMOS inverters. The design is able to quantize analog input from 285mV to 600mV, with 64 quantization levels that make use of the source voltage of 1.6V. The TIQ-Comparator is quantizing the input signal any 5mV increment comparable to an increase of 1 (one) level output in the thermometer code system.

Achieving low power dissipation of 31.14μW and a smaller chip size of 1065μm^2 make this design suitable for a sensor having the output in the range of quantization.

Acknowledgements

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